

TO PAGE -1 CPU

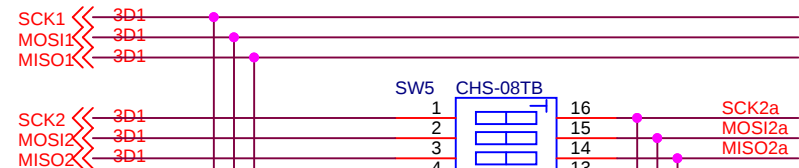
IRQ1 <- 3C1
IRQ2 <- 3C1
IRQ3 <- 3C1
IRQ4 <- 3C1

SHUT DN UART 6 <- 3C1
SHUT DN UART 7 <- 3C1
SHUT DN UART 8 <- 3C1
SHUT DN UART 9 <- 3C1
SHUT DN UART 10 <- 3C1
SHUT DN UART 11 <- 3C1
SHUT DN UART 12 <- 3C1
SHUT DN UART 13 <- 3C1

CS UART 6 <- 3C1
CS UART 7 <- 3C1
CS UART 8 <- 3C1
CS UART 9 <- 3C1
CS UART 10 <- 3C1
CS UART 11 <- 3C1
CS UART 12 <- 3C1
CS UART 13 <- 3C1

UARTS split on two SPIs
1, 2, 3 on
6, 7, 8 off

UARTS on SPI 1
1, 2, 3 off
6, 7, 8 on



UART SPI SELECT

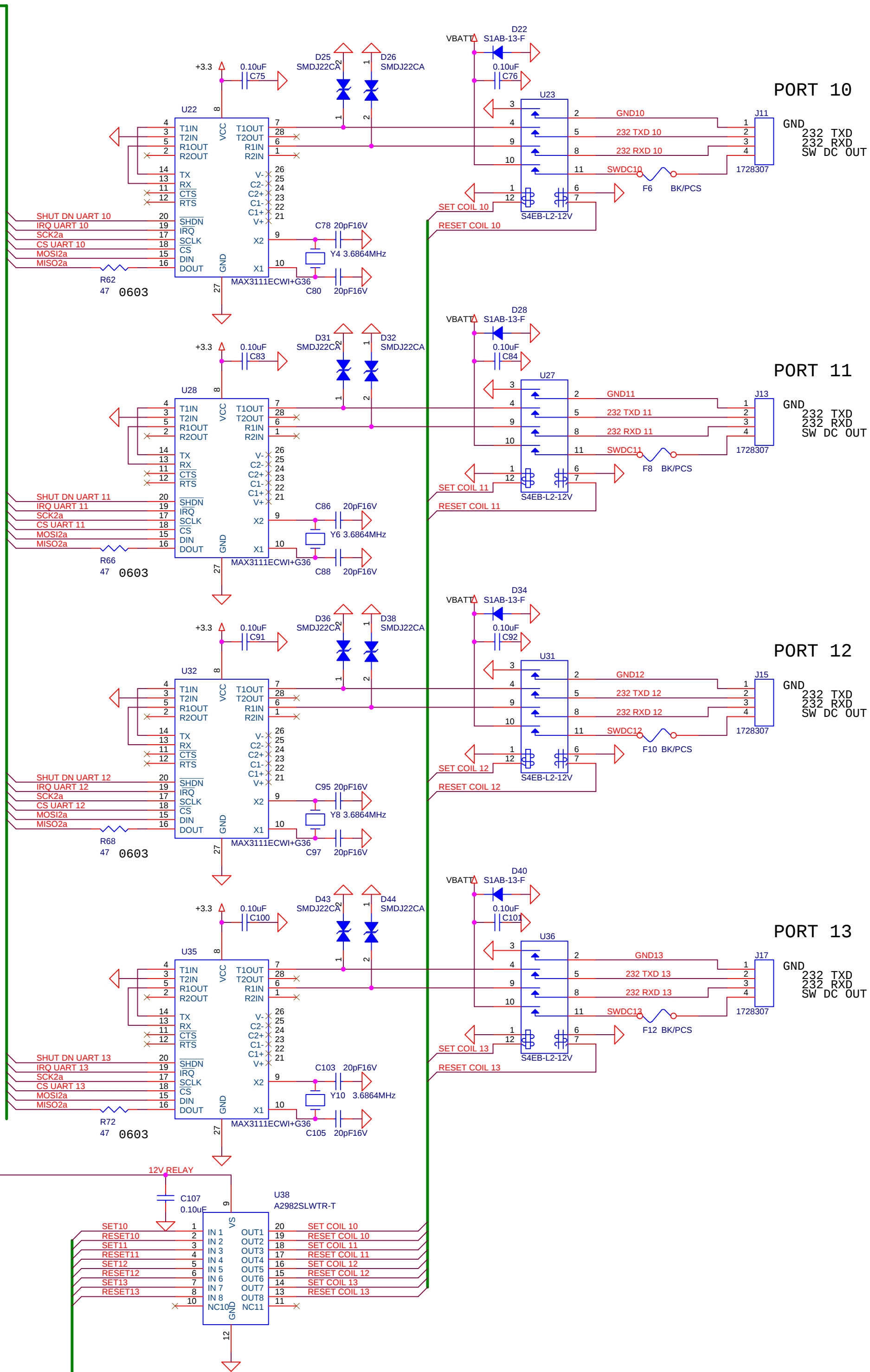
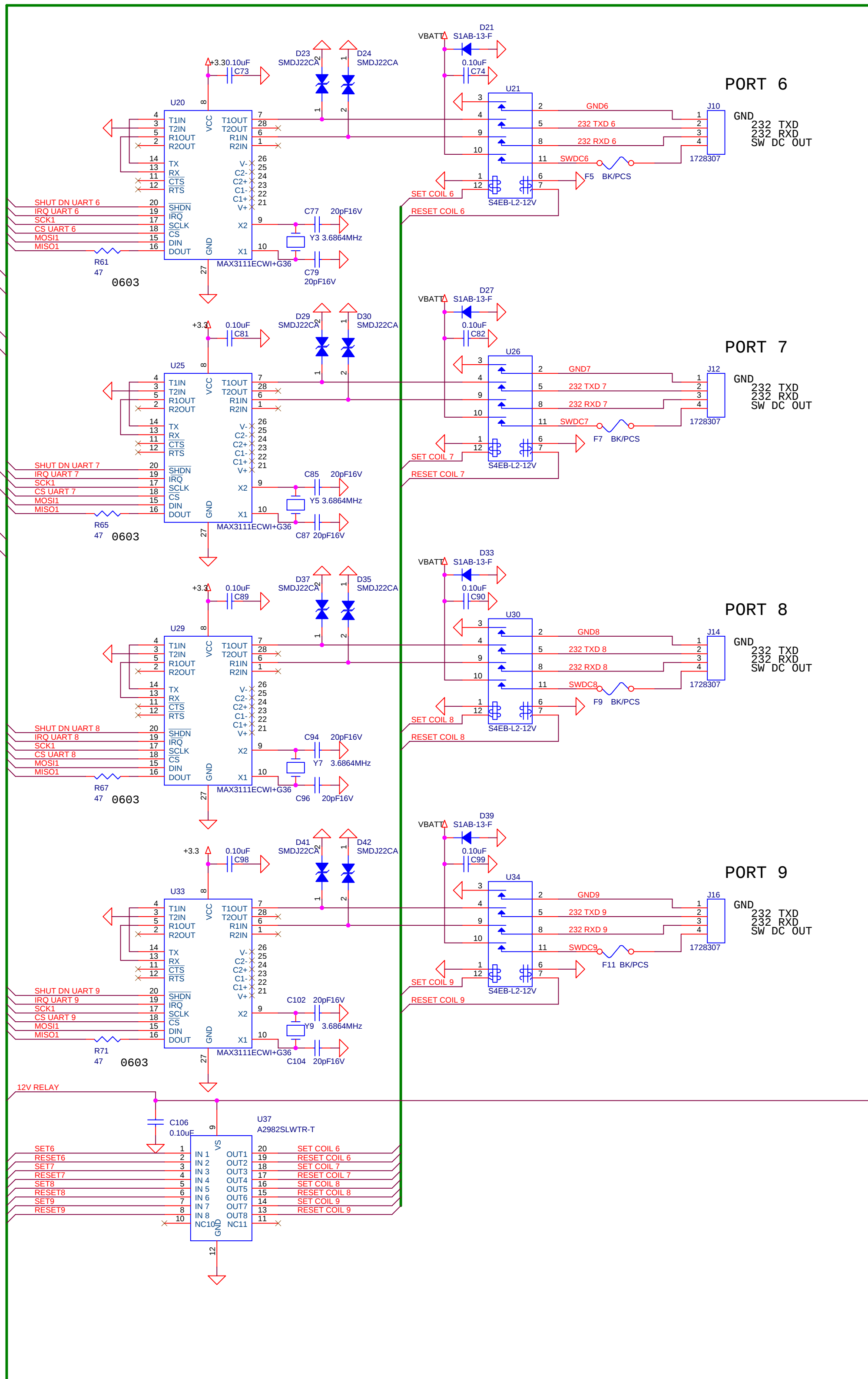
SET6 <- 3C1
RESET6 <- 3C1
SET7 <- 3C1
RESET7 <- 3C1
SET8 <- 3C1
RESET8 <- 3C1
SET9 <- 3C1
RESET9 <- 3C1
SET10 <- 3C1
RESET10 <- 3C1
SET11 <- 3C1
RESET11 <- 3C1
SET12 <- 3C1
RESET12 <- 3C1
SET13 <- 3C1
RESET13 <- 3C1

12V RELAY <- 3A1

VBATT <- VBATT 3C1

+3.3 <- +3.3 3C1

GND_SIGNAL <- 3C1



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