

Preliminary

KM616FV2000, KM616FS2000, KM616FR2000 Family CMOS SRAM

Document Title

128Kx16 Super Low Voltage Low Power Full CMOS SRAM Data Sheets

Revision History

<u>Rev No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
Rev 0.0	• Initial Draft	May. 3rd, 96	Advance Information
Rev 0.1	• First edition	Aug. 12th, 96	Preliminary
Rev 0.2	Second edition	Sep. 1st, 96	Preliminary
Rev 0.3	• Third edition - Edded KM616FV2000 family - Extended operating Vcc range of FS family from 2.3(min)~3.2V(max) to 2.3(min)~3.3V(max) - Deleted high power version : Isb1=5uA - Added low power version : Isb1=10uA - Added Super Low Power Version with Special Handling : Isb1=2.0uA(max) - Reduced Icc1 & Icc Write : 25mA ----> 20mA at Vcc=3.6V(max) - Deleted 70ns and added 85ns in KM616FS2000 family	Nov 21st, 96	Preliminary

Customer Approval

Please fill out the following table and send it to SEC branch office or Product Planning Team in Seoul Korea We will help your further requests and provide technical supports based on this material.	
Department	
Received Date	
Sent Date(to SEC)	
Approved by & Comments	
(Signature)	

The attached data sheets are prepared and approved by SAMSUNG Electronics. And SAMSUNG Electronics has the right to change all the specifications in data sheets. SAMSUNG Electronics will evaluate and reply to any dear customer's requests and questions on the parameters of this device. If dear customer has any questions, please contact the SAMSUNG branch office near your office or call or fax to the memory product planning team.

Tel : 82-2-760-6068 Fax : 82-2-760-7990

KM616FV2000, KM616FS2000, KM616FR2000 Family CMOS SRAM

128Kx16 bit Low Power CMOS Static RAM

FEATURE SUMMARY

- Process Technology : 0.4 um Full CMOS
- Organization : 128K x 16
- Power Supply Voltage
 - KM616FV2000 Family : 3.0(min)~3.6(max)
 - KM616FS2000 Family : 2.3(min)~3.3V(max)
 - KM616FR2000 Family : 1.8(min)~2.7(max)
- Low Data Retention Voltage : 1.5V(Min)
- Three state output status and TTL Compatible
- Package Type : JEDEC Standard
 - 44-TSOP(II)-Forward/Reverse

GENERAL DESCRIPTION

The KM616FV2000, KM616FS2000 and KM616FR2000 family are fabricated by SAMSUNG's advanced Full CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operations with low data retention current.

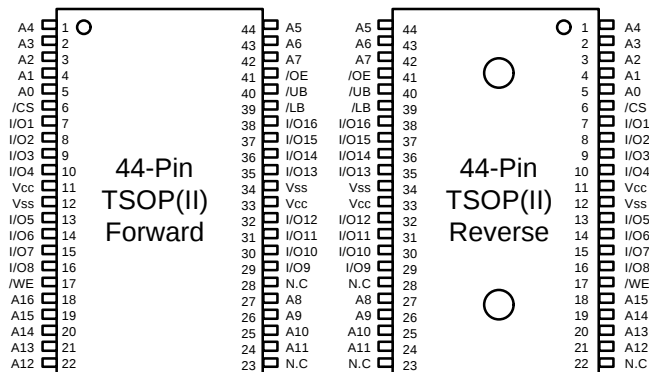
PRODUCT FAMILY

Product Family	Operating Temp Range	Vcc Range (min~max)	Speed(ns)	Power Dissipation		PKG Type
				Operating (Icc2)	Standby (Isb1)	
KM616FV2000	Commercial (0~70 °C)	3.0~3.6V	70*/85 @ Vcc=3.3 +/- 0.3V	80mA(max)	2uA*** /10uA** (max)	44-TSOP(II) Forward/ Reverse
KM616FS2000		2.3~3.3V	85 @ Vcc=3.0 +/- 0.3V 120*/150 @ Vcc=2.5 +/- 0.2V	80mA(max) 50mA(max)		
KM616FR2000		1.8~2.7V	300* @ Vcc=2.0 +/- 0.2V	25mA(max)		
KM616FV2000I	Industrial (-40~85 °C)	3.0~3.6V	70*/85 @ Vcc=3.3 +/- 0.3V	80mA(max)	2uA*** /10uA** (max)	44-TSOP(II) Forward/ Reverse
KM616FS2000I		2.3~3.3V	120*/150 @ Vcc=2.5 +/- 0.2V 85 @ Vcc=3.0 +/- 0.3V	80mA(max) 50mA(max)		
KM616FR2000I		1.8~2.7V	300* @ Vcc=2.0 +/- 0.2V	25mA(max)		

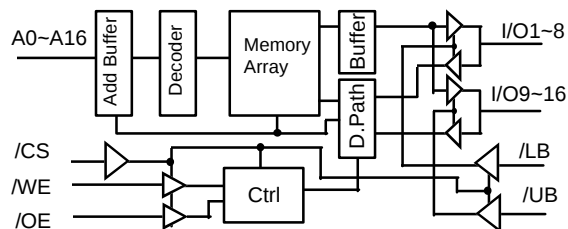
* measured with 30pF test load, ** low low power version

*** for super low power version with special handling

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



Name	Function	Name	Function
A0~A16	Address Inputs	/LB	Lower Byte(I/O1~8)
/WE	Write Enable Input	/UB	Upper Byte(I/O9~16)
/CS	Chip Select Input	Vcc	Power
/OE	Output Enable Input	Vss	Ground
I/O1~I/O16	Data Input/Output	N.C	No Connection

Preliminary

KM616FV2000, KM616FS2000, KM616FR2000 Family **CMOS SRAM**

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST FOR LOW LOW POWER CONSUMPTION

Commercial Temp Products (0~70 °C)		Industrial Temp Products (-40~85 °C)	
Part Name	Function	Part Name	Function
KM616FV2000T-7	44-TSOP F, 3.3V, 70ns, LL-pwr	KM616FV2000TI-7	44-TSOP F,3.3V,70ns,LL-pwr
KM616FV2000T-8	44-TSOP F,3.3V,85ns,LL-pwr	KM616FV2000TI-8	44-TSOP F,3.3V,85ns,LL-pwr
KM616FV2000R-7	44-TSOP R,3.3V,70ns,LL-pwr	KM616FV2000RI-7	44-TSOP R,3.3V,70ns,LL-pwr
KM616FV2000R-8	44-TSOP R,3.3V,85ns,LL-pwr	KM616FV2000RI-8	44-TSOP R,3.3V,85ns,LL-pwr
KM616FS2000T-12	44-TSOP F,2.5/3.0V,120/85ns,LL-pwr	KM616FS2000TI-12	44-TSOP F,2.5/3.0V,120/85ns,LL-pwr
KM616FS2000T-15	44-TSOP F,2.5/3.0V,150/85ns,LL-pwr	KM616FS2000TI-15	44-TSOP F,2.5/3.0V,150/85ns,LL-pwr
KM616FS2000R-12	44-TSOP R,2.5/3.0V,120/85ns,LL-pwr	KM616FS2000RI-12	44-TSOP R,2.5/3.0V,120/85ns,LL-pwr
KM616FS2000R-15	44-TSOP R,2.5/3.0V,150/85ns,LL-pwr	KM616FS2000RI-15	44-TSOP R,2.5/3.0V,150/85ns,LL-pwr
KM616FR2000T-30	44-TSOP,F, **2.0/2.5V,300ns,LL-pwr	KM616FR2000TI-30	44-TSOP,F, 2.0/2.5V,300ns,LL-pwr
KM616FR2000R-30	44-TSOP,R, 2.0/2.5V,300ns,LL-pwr	KM616FR2000RI-30	44-TSOP,R, 2.0/2.5V,300ns,LL-pwr

* The meaning of 2.5V/3.0V, 120/85ns is that the operating Vcc is ranged from 2.3V(min) to 3.3V(max) with speed 120ns @ 2.5V +/- 0.2 and 85ns @ 3.0V +/- 0.3. This type of meaning is applied to other notations like the example.

** But in case of KM616FR2000T-30, there is only one speed bin, 300ns though it supports wide range operating Vcc.

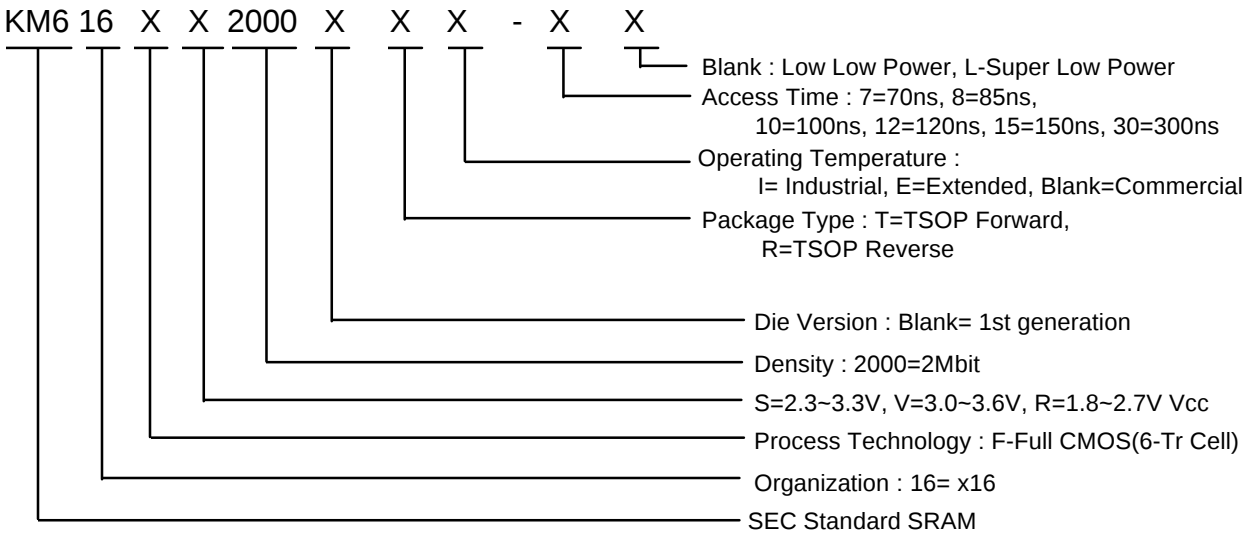
PRODUCT LIST FOR SUPER LOW POWER CONSUMPTION

The product names for super low power version has letter [L] at the end of product name of low low power version. The part name for 128Kx16 Super Low Power product operating at 2.3~3.3V with 85ns @ 3.0V and 120ns @ 2.5V access time will be KM616FS2000TI-12L

And if suppliment is required for those products, please contact Samsung Electronics Branch near your office. Samsung will support with special treatment.

KM616FV2000, KM616FS2000, KM616FR2000 Family CMOS SRAM

ORDERING INFORMATION



Preliminary

KM616FV2000, KM616FS2000, KM616FR2000 Family CMOS SRAM

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	Vin, Vout	- 0.2 to 3.6V**	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.2 to 4.0V**	V	-
Power Dissipation	Pd	1.0	W	-
Storage temperature	Tstg	-55 to 150	°C	-
Operating Temperature	Ta	0 to 70	°C	KM616FV2000 KM616FS2000 KM616FR2000
		-40 to 85	°C	KM616FV2000I KM616FS2000I KM616FR2000I
Soldering temperature and time	Tsolder	260 °C, 5sec(Lead Only)	-	-

* Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

** 1) Vin, Vout for KM616FV2000 family ; -0.2 to 3.9V

2) Maximum Vcc range for KM616FV2000 family ; -0.2 to 4.6V

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol			Min	Typ**	Max	Unit
Supply voltage	Vcc	KM616FV2000 Family		3.0	3.3	3.6	V
		KM616FS2000 Family		2.3	2.5/3.0	3.3	V
		KM616FR2000 Family		1.8	2.0/2.5	2.7	V
Ground	Vss			0	0	0	V
Input high voltage	Vih	KM616FV2000 Family	Vcc=3.3+/- 0.3V	2.2	-	Vcc+0.2	V
		KM616FS2000 Family	Vcc=3.0+/- 0.3V	2.2	-	Vcc+0.2	V
			Vcc=2.5 +/- 0.2V	2.0		Vcc+0.2	V
		KM616FR2000 Family	Vcc=2.5 +/- 0.2V	2.0		Vcc+0.2	V
			Vcc=2.0 +/- 0.2V	1.6		Vcc+0.2	V
Input low voltage	Vil			-0.2***		0.4	V

* 1) Commercial Product : Ta=0 to 70 °C , unless otherwise specified

2) Industrial Product : Ta=-40 to 85 °C, unless otherwise specified

** Ta=25 °C

*** Vil(min)=-1.5V for $t_i \geq 30$ ns pulse

CAPACITANCE * (f=1MHz, Ta=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	Cin	Vin=0V	-	8	pF
Input/Output capacitance	Cio	Vio=0V	-	10	pF

* Capacitance is sampled not 100% tested

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KM616FV2000, KM616FS2000, KM616FR2000 Family CMOS SRAM

DC AND OPERATING CHARACTERISTICS

Item		Symbol	Test Conditions ¹⁾		Min	Typ	Max	Unit		
Input leakage current		Ili	Vin=Vss to Vcc		-1	-	1	uA		
Output leakage current		Ilo	/CS=Vih or /WE=Vil, Vio=Vss to Vcc		-1	-	1	uA		
Operating power supply current		Icc	/CS=Vil Vin=Vih or Vil, Iio=0mA		Read	-	-	15 ⁵⁾	mA	
					Write		-	20 ⁵⁾		
Average operating current		Icc1	Cycle time=1uS 100% duty /CSi 0.2V,		Read	-	-	15 ⁵⁾	mA	
					Write		-	20 ⁵⁾		
		Icc2	Iio=0mA,/CS=Vih Min cycle, 100% duty		Vcc=3.3V @ 85ns		-	-	80 ⁴⁾	mA
					Vcc=2.7V @ 100ns				60	
Vcc=2.2V @ 300ns							25			
Output low voltage		Vol	Iol	Vcc=3.0/3.3V	2.1mA	-	-	0.4	V	
				Vcc=2.5V	0.5mA			0.4		
				Vcc=2.0V	0.33mA			0.4		
Output high voltage		Voh	Ioh	Vcc=3.0/3.3V	-1.0mA	2.4	-	-	V	
				Vcc=2.5V	-0.5mA	2.0	-	-		
				Vcc=2.0V	-0.44mA	1.6	-	-		
Standby Current(TTL)		Isb	/CS=Vih		-	-	0.3	mA		
Standby Current (CMOS)	KM616FV2000	Isb1	/CSi Vcc-0.2V Other inputs =0~Vcc		Super Low Power		-	0.05 ³⁾	2 ²⁾	uA
	Low Low Power				-	-	10 ²⁾			
	KM616FS2000				Super Low Power		-	0.05 ³⁾	2 ²⁾	uA
	KM616FR2000				Low Low Power		-	-	10 ²⁾	
	KM616FV2000I									
KM616FS2000I										
	KM616FR2000I									

1) - Commercial Product

T_a=0 to 70 °C, V_{cc}=3.3 +/- 0.3V for 616FV2000 Family, V_{cc}=2.3(min)~3.3(max)V for 616FS2000 Family,
V_{cc}=1.8(min)~2.7(max)V for 616FR2000 Family

- Industrial Product

T_a=-40 to 85 °C, V_{cc}= 3.3 +/- 0.3V for 616FV2000I Family, V_{cc}=2.3(min)~3.3V(max)V for 616FS2000I Family
V_{cc}=1.8(min)~2.7(max)V for 616FR2000I Family

2) The value has difference by +/- 1uA

Measured at V_{cc}=3.3V

3) The value is not 100% tested but obtained statistically at Temp= 25 °C

4) - The value is measured at V_{cc}=3.0V +/-0.3

- I_{cc2}=70mA with 70ns at V_{cc}=3.3V +/- 0.3, but this value is not 100% tested but obtained statistically.

- I_{cc2}=40mA with 100ns cycle at V_{cc}=2.5V +/- 0.2, but this value is not 100% tested but obtained statistically.

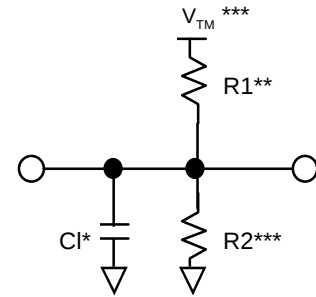
- I_{cc2}=20mA with 150ns cycle at V_{cc}=2.0V +/- 0.2, but this value is not 100% tested but obtained statistically.

5) The value is measured at V_{cc}=3.0V +/- 0.3. The value measured at V_{cc}=2.5/2.0V is under the value of V_{cc}=3.0V +/- 0.3

A.C CHARACTERISTICS

TEST CONDITIONS (1. Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	Vcc=3.3V, 3.0V, 2.5V
	0.4 to 1.8V	Vcc=2.0V
Input rise fall time	5ns	-
Input and output reference voltage	1.5V	Vcc=3.3V, 3.0V
	1.1V	Vcc=2.5V
	0.9V	Vcc=2.0V
Output load (See right)	Cl=100pF	See Test Condition #2
	Cl=30pF	



* Including scope and jig capacitance
 ** R1=3070 Ω , R2=3150 Ω
 ***V_{TM}=2.8V for Vcc=3.0/3.3V
 2.3V for Vcc=2.5V
 1.8V for Vcc=2.0V

* See test condition of DC and Operating characteristics

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Vcc Range	Typical Supply Vcc	Speed	Comments
KM616FR2000	0~70 °C	1.8(min)~ 2.7(max)	2.0 +/- 0.2V Operation	300*ns	Commercial
KM616FS2000	0~70 °C	2.3(min)~ 3.3V(max)	2.5 +/- 0.2V Operation	120*/150ns	
			3.0 +/- 0.3V Operation	85ns	
KM616FV2000	0~70 °C	3.0(min)~ 3.6V(max)	3.3 +/- 0.3V Operation	70*/85ns	Industrial
KM616FR2000I	-40~85 °C	1.8(min)~ 2.7(max)	2.0 +/- 0.2V Operation	300*ns	
			2.5 +/- 0.2V Operation	120*/150ns	
KM616FS2000I	-40~85 °C	2.3(min)~ 3.3V(max)	3.0 +/- 0.3V Operation	85ns	
			3.3 +/- 0.3V Operation	70*/85ns	
KM616FV2000I	-40~85 °C	3.0(min)~ 3.6V(max)			

* Parameters are measured with 30pF test load

Preliminary

KM616FV2000, KM616FS2000, KM616FR2000 Family CMOS SRAM

PARAMETER LIST FOR EACH SPEED BIN

Parameter List		Sym -bol	Speed Bins												Un-its
			70ns		85ns		100ns*		120ns		150ns		300ns		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	120	-	150	-	300	-	ns
	Address access time	tAA	-	70	-	85	-	100	-	120	-	150	-	300	ns
	Chip select to output	tCO1, tCO2	-	70	-	85	-	100	-	120	-	150	-	300	ns
	Output enable to valid output	tOE	-	35	-	45	-	50	-	60	-	75	-	150	ns
	/UB, /LB Access Time	tBA	-	35	-	45	-	50	-	60	-	75	-	150	ns
	Chip select to low-Z output	tLZ1, tLZ2	10	-	10	-	10	-	20	-	20	-	50	-	ns
	/OE & /LB,/UB to low-Z output	tOLZ tBLZ	5	-	5	-	5	-	20	-	20	-	30	-	ns
	Chip disable to high-Z output	tHZ1, tHZ2	0	25	0	25	0	30	0	35	0	40	0	60	ns
	/OE & /UB,/LB disable to high-Z	tOHZ tBHZ	0	25	0	25	0	30	0	35	0	40	0	60	ns
	Output hold from address change	tOH	10	-	15	-	15	-	15	-	15	-	30	-	ns
Write	Write cycle time	tWC	70	-	85	-	100	-	120	-	150	-	300	-	ns
	Chip select to end of write	tCW	65	-	70	-	80	-	100	-	120	-	300	-	ns ns
	Address set-up time	tAS	0	-	0	-	0	-	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	65	-	70	-	80	-	100	-	120	-	300	-	ns
	Write pulse width	tWP	55	-	60	-	70	-	80	-	100	-	200	-	ns
	/UB, /LB Valid to End of Write	tBW	65	-	70	-	80	-	100	-	120	-	300	-	ns
	Write recovery	tWR	0	-	0	-	0	-	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	25	0	30	0	35	0	40	0	60	ns
	Data to write time overlap	tDW	30	-	35	-	40	-	50	-	60	-	120	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	0	-	0	-	0	-	ns
End write to output low-Z	tOW	5	-	5	-	5	-	5	-	5	-	20	-	ns	

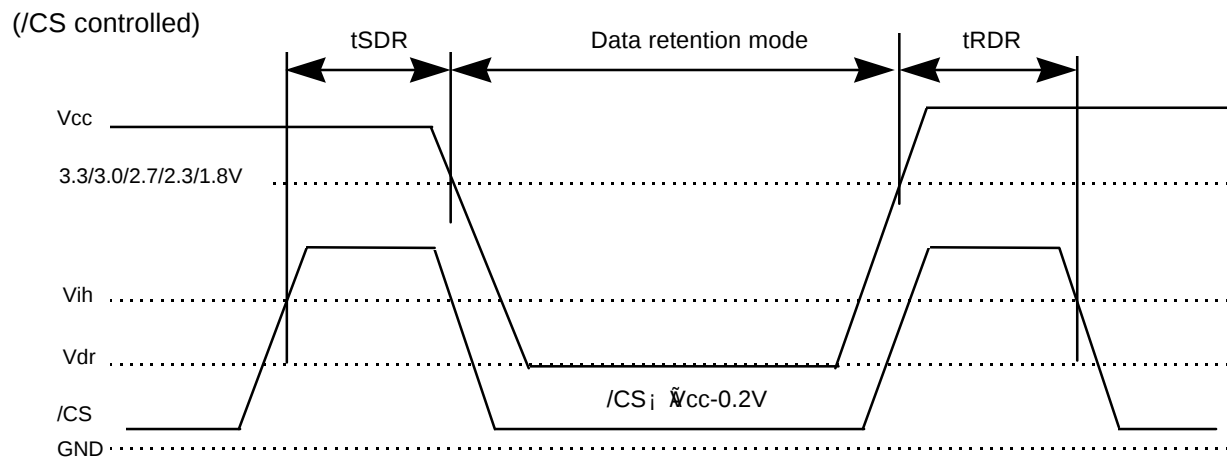
* not yet available, only for reserved speed bins

DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	Vdr	/CS _i $\bar{V}_{cc}-0.2V$		1.5	-	3.6	V
Data retention current	I _{dr}	Vcc=3.0V /CS _i $\bar{V}_{cc}-0.2V$	Super Low Power	***	**	2	uA
			Low Low Power	-	-	10	
Data retention set-up time	tSDR	See data retention waveform		0	-	-	ns
Recovery time	tRDR			tRC	-	-	

* 1) Commercial Product : Ta=0 to 70 °C, unless otherwise specified
 2) Industrial Product : Ta=-40 to 85 °C, unless otherwise specified
 ** Ta=25 °C, the value is too small to detect by test machine, 0.01uA statistically
 *** The min value is almost 0nA statistically

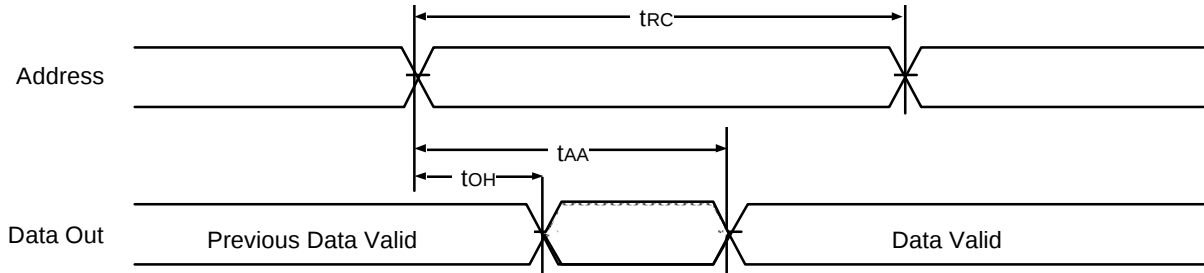
DATA RETENTION TIMING DIAGRAM



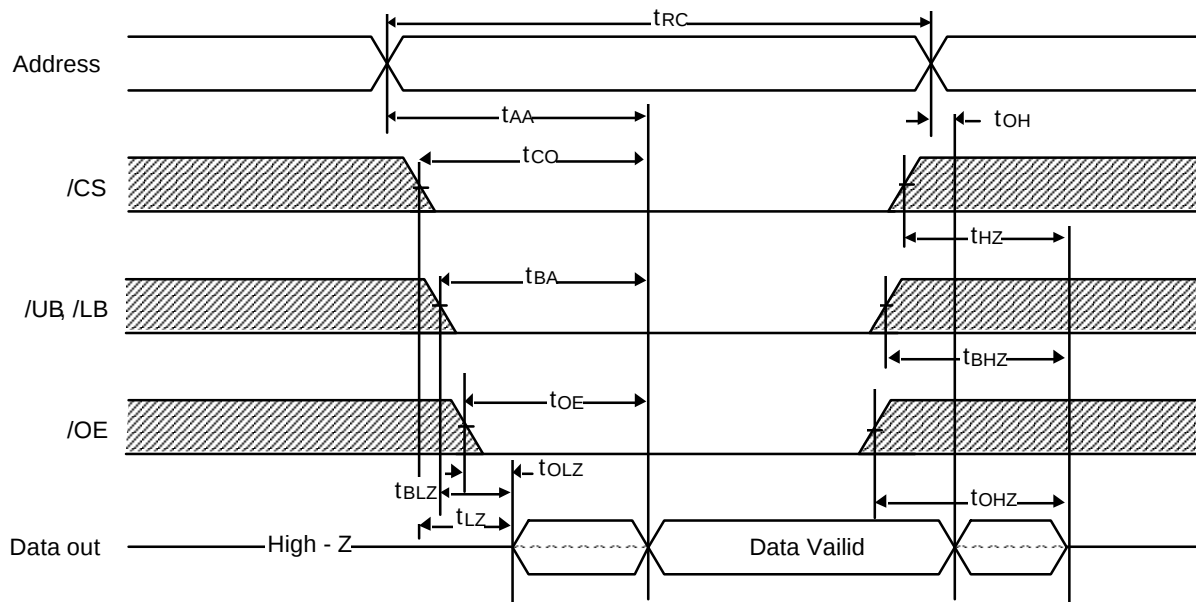
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

(/CS=/OE=Vil, /WE=Vih, /UB or, and /LB=Vil)



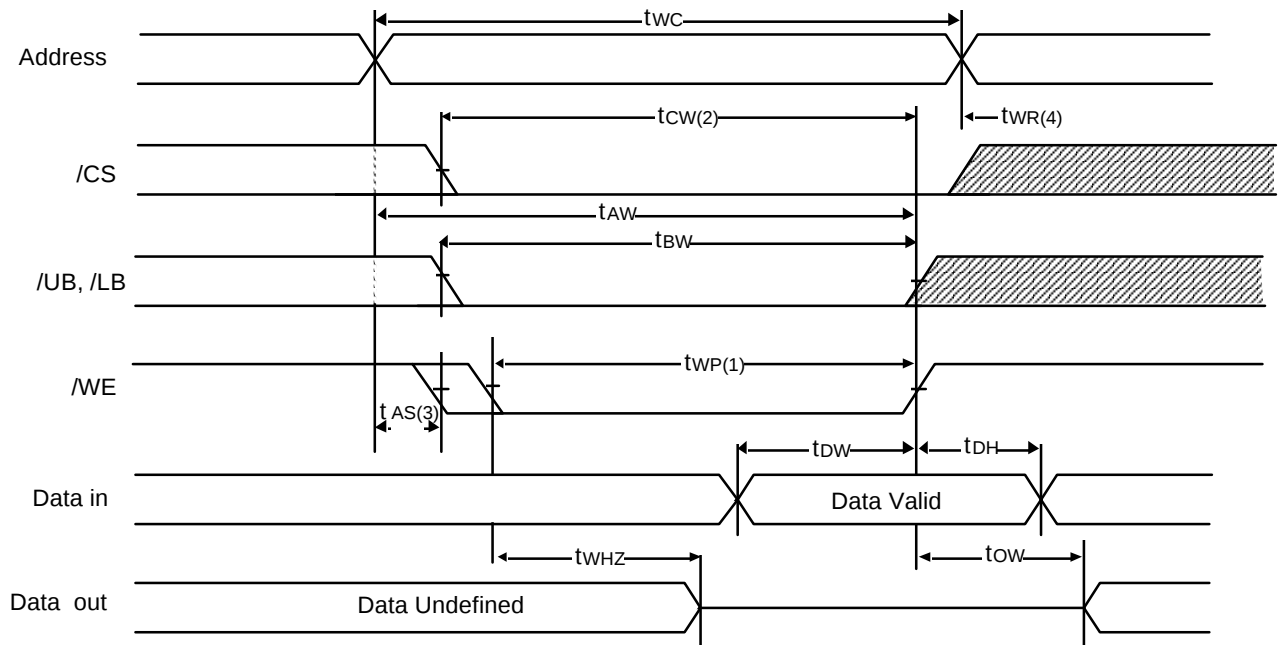
TIMING WAVEFORM OF READ CYCLE (/WE= V_{IH})



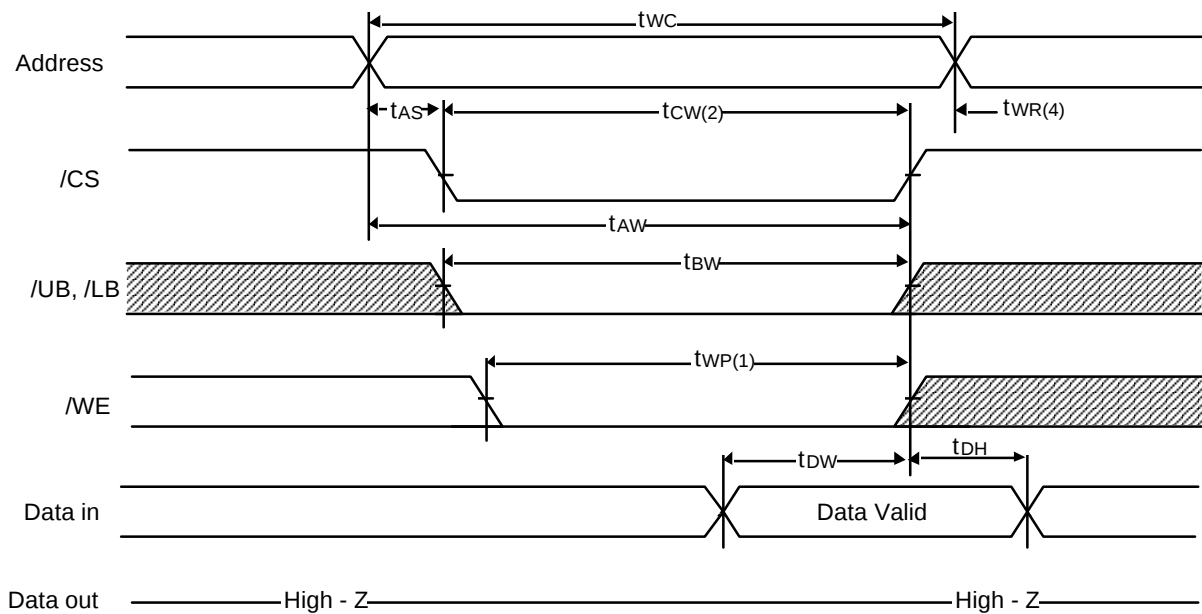
Notes (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{max.})$ is less than $t_{LZ}(\text{min.})$ both for a given device and from device to device.

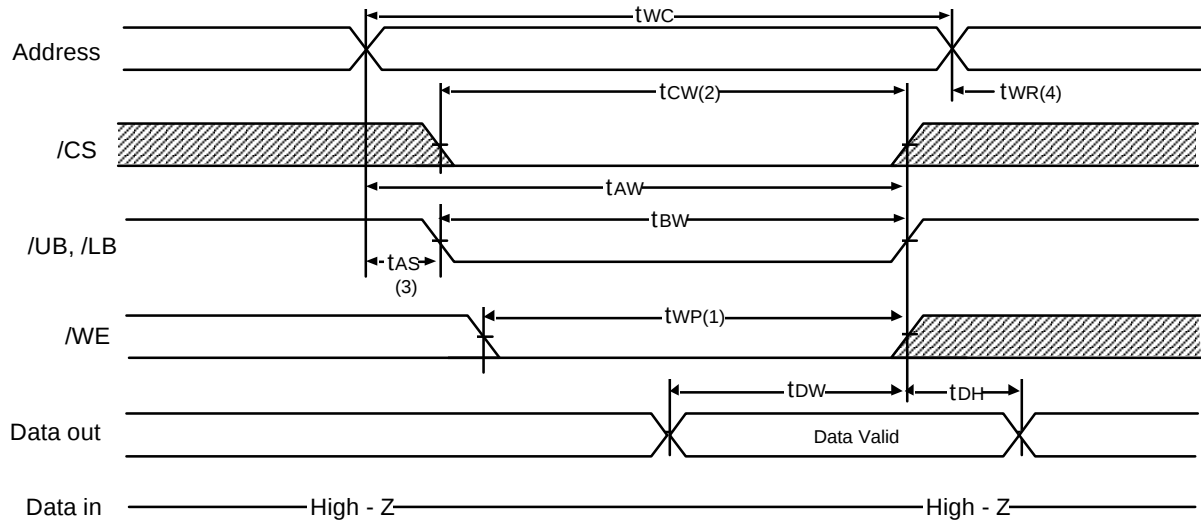
TIMING WAVEFORM OF WRITE CYCLE (/WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE (/CS Controlled)



TIMING WAVEFORM OF WRITE CYCLE (/UB,/ LB Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of a low $/CS$ and low $/WE$. A write begins at the latest transition among $/CS$ going low and $/WE$ going low : A write end at the earliest transition among $/CS$ going high and $/WE$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $/CS$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $/CS$, or $/WE$ going high.

FUNCTIONAL DESCRIPTION

$/CS$	$/LB$	$/UB$	$/WE$	$/OE$	Mode	I/O1~8	I/O 9~16	Current Mode
H	X	X	X	X	Not Select	High-Z	High-Z	Isb1
L	X	X	H	H	Output	High-Z	High-Z	Icc
L	H	H	X	X	Disable	High-Z	High-Z	
L	L	H	H	L	Read	Dout	High-Z	Icc
L	H	L	H	L	Read	High-Z	Dout	
L	L	L	H	L	Read	Dout	Dout	
L	L	H	L	X	Write	Din	High-Z	Icc
L	H	L	L	X	Write	High-Z	Din	
L	L	L	L	X	Write	Din	Din	

* X means don't care(Must be in high or low state)

44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400F)

Unit : Millimeters (Inches)

