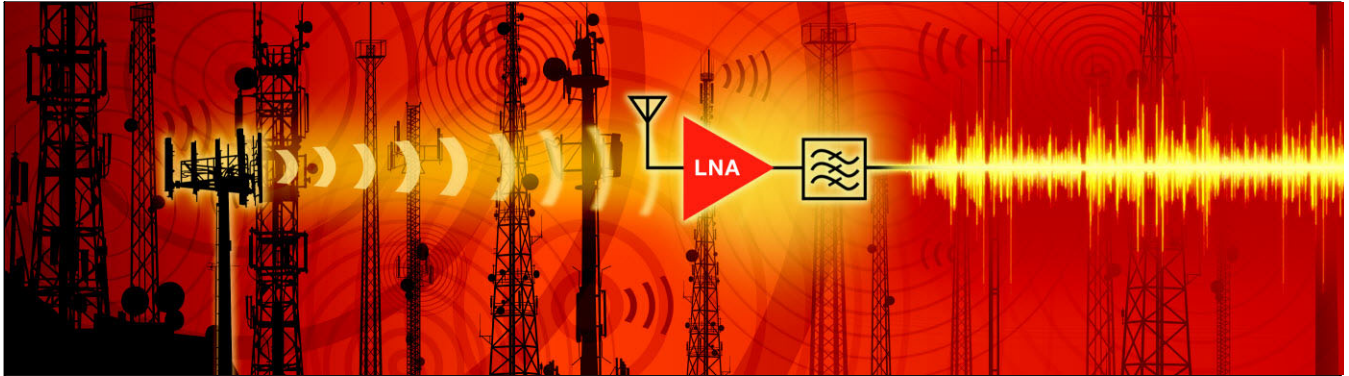




Practical Considerations for Low Noise Amplifier Design

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INTRODUCTION

Low noise amplifiers (LNAs) play a key role in radio receiver performance. The success of a receiver's design is measured in multiple dimensions: receiver sensitivity, selectivity, and proclivity to reception errors. The RF design engineer works to optimize receiver front-end performance with a special focus on the first active device.

This paper considers device- and board-level variables that affect LNA performance and confront the engineer at each level of design in accommodating the various requirements of specific applications. To illustrate the practical challenges, performance trade-offs for three popular LNA topologies and two process technology implementations are examined. Each of the topics covered can easily be expanded into individual chapters, but the purpose of this paper is to provide a concise summary of the most salient considerations affecting LNA performance and implementation.

All receivers require an LNA with sufficient sensitivity to discern the residual signal from the surrounding noise and interference in order to reliably extract the embedded information. Five characteristics of LNA design are under the designer's control and directly affect receiver sensitivity: noise figure, gain, bandwidth, linearity, and dynamic range. Controlling these characteristics, however, requires an understanding of the active device, impedance matching, and details of fabrication and assembly to create an amplifier that achieves optimal performance with the fewest trade-offs.

Figure 1 shows the set of variables that affect LNA performance at the device and board design levels. It is up to the designer to mitigate the impact of environmental variables, while finding the most appropriate trade-off between competing characteristics to optimize receiver sensitivity and selectivity, and maintaining information integrity.

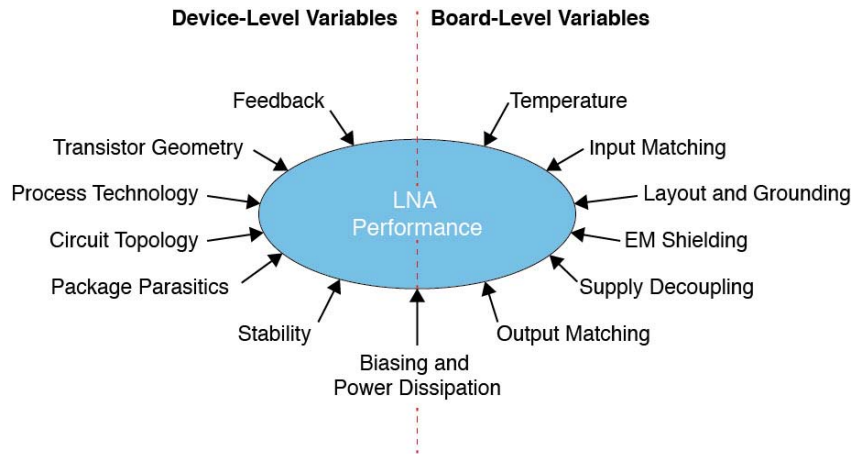


Figure 1. LNA Performance Variables

LNA Parameters

Preliminary to any discussion of LNA performance optimization, it is worthwhile to define the noise parameters associated with LNAs and briefly point out the importance of considering measurement uncertainty, particularly for sub-1 dB noise figures. Agilent Technologies Inc. offers an excellent library of application notes that describe in detail noise figure measurements and methods. Agilent's online "NF Uncertainty Calculator" identifies the factors that contribute to noise figure uncertainty and can facilitate design work by estimating the measurement uncertainty associated with a device under test (DUT) based on its characteristics and the measurement system specifications. For instance, when measuring sub-1 dB noise figures, careful vector calibration of the measurement reference plane and mismatch correction between the noise source and DUT become critical to measurement precision.

The process of adjusting LNA source admittance and mapping its characteristics is called "source pulling." Noise parameters map the relationship between source admittance (Y_{source}) and noise characteristics as described in the following equation for noise figure NF:

$$\text{NF} = 10 \cdot \log \left(F_{\min} + \frac{R_n}{\text{Re}(Y_{\text{source}})} \cdot |Y_{\text{source}} - Y_{\text{opt}}|^2 \right) \quad (1)^1$$

The following noise parameters are used in this paper to describe LNA performance at a given frequency, temperature, and bias level:

- $Y_{\text{opt}}(S)$ — The unique value of the normalized input admittance at which the noise factor is at a minimum ($F_{\min}$). The complex conjugate of Y_{opt} must be presented to the LNA input for the best possible noise performance (or Γ_{opt} when expressed in terms of reflection coefficients).
- $F_{\min}$ — The minimum achievable noise factor when $Y_{\text{source}}^* = Y_{\text{opt}}$; also minimum noise figure, $\text{NF}_{\min} = 10 \log(F_{\min})$

- R_n (Ω) — The equivalent noise resistance (the NF sensitivity to the deviation between Y_{source} and Y_{opt})
- Y_{in} (S) — The normalized input admittance for maximum power transfer
- Y_{source} (S) — The normalized admittance presented to the LNA input

Figure 2 defines the reference plane and admittances used here to describe LNA performance. Unless otherwise stated, each admittance is normalized to $Y_0 = 0.02 \text{ S} = (50 \Omega)^{-1}$ at the input or output of the LNA, including impedance matching networks. A reference plane is a specific point within an RF system that is set to a specific impedance (either by calibration or definition) to enable side-by-side comparisons of the same parameter. Side-by-side parametric comparisons are invalid if the reference plane impedance is unknown or significantly different.

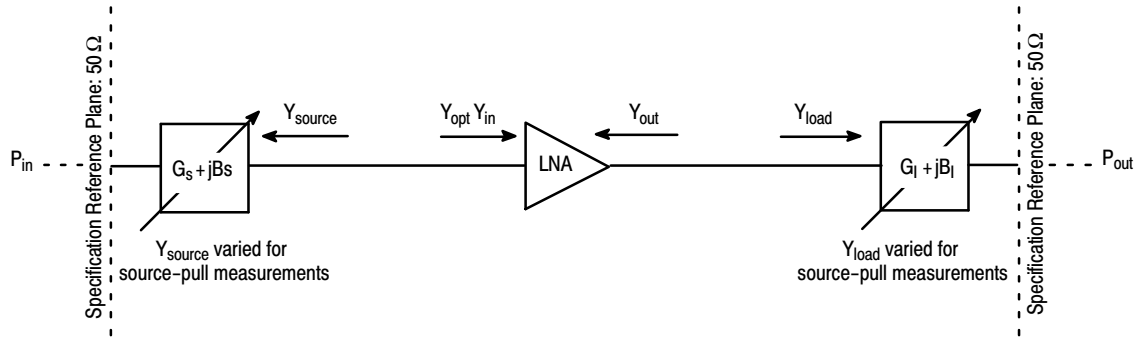


Figure 2. LNA Performance Reference Plane and Admittances

System-Level Requirements for Receiver Sensitivity

Although radio link budgeting is beyond the scope of this paper, it can be used to model the determinants of receiver sensitivity for LNA performance optimization as shown in Figure 3 and the following set of equations:

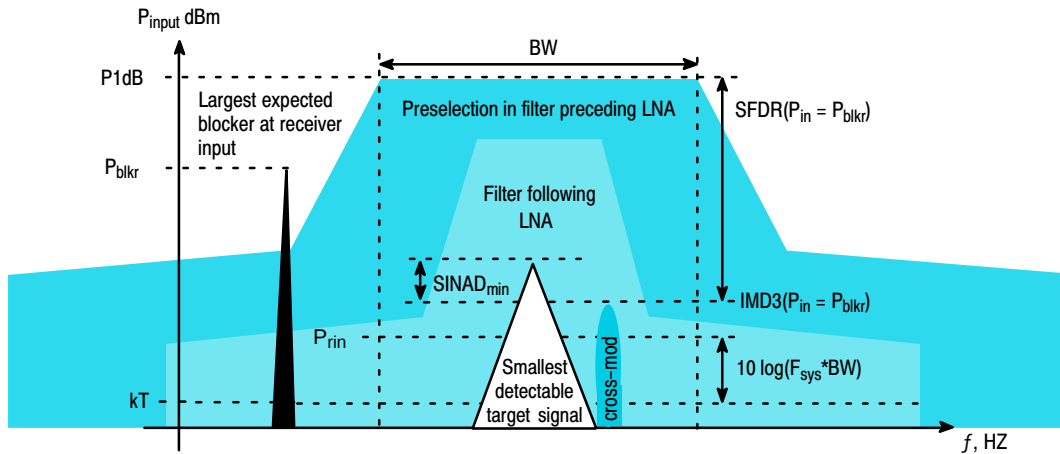


Figure 3. Receiver Input Sensitivity

$$NF_{sys} = 10 \log(F_{sys}) = 10 \log\left(F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \dots + \frac{F_n - 1}{G_1 G_2 \dots G_{n-1}}\right), \text{ dB} \quad (2)$$

$$P_{rin} = kT + 10 \log(BW) + NF_{sys}, \text{ dBm} \quad (3)$$

$$[P1dB]_{input} = [P1dB]_{output} - G_{sys} + 1, \text{ dBm} \quad (4)$$

$$SFDR(P_{in} = P_{blk}) = [P1dB]_{input} - IMD3(P_{in} = P_{blk}), \text{ dB} \quad (5)$$

Where:

- NF_{sys} is the cascaded noise figure of the system referred to the input (the Friis formula).
- F_n and G_n are the noise factor and linear gain, respectively, of each successive stage within the receiver signal chain.
- P_{rin} is the noise floor for receiver input sensitivity.
- kT is thermal noise density: -174 dBm/Hz at room temperature
- BW is the receiver signal pass bandwidth.
- $P1dB$ is the signal power at the input/output that corresponds to 1 dB gain compression.

- G_{sys} is the linear system gain.
- $SFDR(P_{in} = P_{blkr})$ is the input-referred, spurious-free, dynamic range with the largest expected blocker signal power (P_{blkr}) present at the receiver input.
- $IMD3(P_{in} = P_{blkr})$ is the third order cross-modulation product generated within the receiver when the largest expected blocker signal power (P_{blkr}) is present at the receiver input.

Both equations 2 and 4 indicate that the receiver signal gain must be set as a compromise between the system noise figure (NF_{sys}) and input dynamic range (P1dB). Although excessive LNA gain degrades the input dynamic range, it must be set high enough for the LNA noise figure to dominate the cascaded noise figure.

P_{rin} defines the noise floor for receiver sensitivity in equation 3. Based on this definition, the receiver bandwidth should be as narrow as possible without degrading the target signal. The receiver noise figure also should be minimized. It is worth considering, however, how low the noise figure actually needs to be in order to meet the application requirements. Improvements in the receiver noise figure can indeed translate into improved receiver performance and range, but it is up to the system designer to decide at what point further improvement in the noise figure results in diminishing returns in terms of improved receiver performance. For example, while a 0.2 dB improvement in noise figure for a satellite communication system might provide a worthwhile improvement to receiver performance, that same 0.2 dB noise figure improvement might not translate into significant benefits in other applications.

Consider the simplified Free Space Path Loss (FSPL) model for line-of-sight radio transmission:

$$FSPL = 20 \log(d) + 20 \log(f_c) - 147.55, \text{ dB} \quad (6)^2$$

Where:

- d is the distance between the transmitter and receiver in meters and f_c is the carrier frequency in Hz.

Although simplified, the FSPL model is useful in demonstrating how there can be diminishing returns with noise figure improvements when the receiver sensitivity is limited only by the receiver's noise floor, in this case, $\Delta FSPL = \Delta NF$. As shown in Table 1, a 0.2 dB improvement in the noise figure can provide up to 2.3% improvement in the receiver range.

Table 1. FSPL Improvement to Receiver Range via Improvements to NF

Improvement in Receiver Noise Figure, ΔNF	Potential Improvement in Receiver Range, Δd
0.1 dB	up to 1.1%
0.2 dB	up to 2.3%
0.5 dB	up to 5.6%
1.0 dB	up to 11%

Input dynamic range is particularly important when large interferers (blockers) close in frequency are present. These blockers can desensitize the receiver and must be either filtered or have their effects mitigated. Equations 4 and 5 (above) describe the input dynamic range of an LNA with gain compression limiting the top-end and cross-modulation distortion limiting receiver sensitivity in the presence of a large blocker. The LNA must be sufficiently linear to mitigate cross-modulation, and the smallest detectable target signal must have sufficient signal power to overcome resultant in-band noise and interference ($SINAD_{min}$). The designer can improve receiver sensitivity by improving LNA linearity when the receiver operates in the midst of blocking signals. LNA linearity is most often specified as a third order intercept point (IP3). A 1 dB improvement in LNA IP3 corresponds to a 2 dB reduction in third order cross-modulation products.

For applications such as 3G/4G cellular base stations, it is important to choose an LNA technology and circuit topology capable of providing high linearity and low noise figures. Improvements to $SINAD_{min}$ require a focus on both receiver noise and linearity performance.

DEVICE-LEVEL CONSIDERATIONS

In this section, the device-level trade-offs for three LNA topologies and two process technologies are addressed. Beyond the choice of technologies, transistor geometry and package parasitics also significantly affect LNA noise figure performance and should be considered when implementing a design.

LNA Topologies

Common-source, common-gate, and cascode are three prevailing LNA topologies. Table 2 provides a concise comparison based on the most relevant considerations for LNA design.

Table 2. Comparison of Three LNA Topologies

Characteristic	Common-Source	Common-Gate	Cascode
Noise Figure	Lowest	Rises rapidly with frequency	Slightly higher than CS
Gain	Moderate	Lowest	Highest
Linearity	Moderate	High	Potentially Highest
Bandwidth	Narrow	Fairly broad	Broad
Stability	Often requires compensation	Higher	Higher
Reverse Isolation	Low	High	High
Sensitivity to Process Variation, Temperature, Power Supply, Component Tolerance	Greater	Lesser	Lesser

The cascode amplifier is the most versatile of the three topologies. It provides the most stable signal gain over the widest bandwidth with only a slight sacrifice in noise figure performance and design complexity.

The common-source transistor is sized to deliver the best possible noise figure, but that advantage often comes at the cost of greater sensitivity to bias, temperature, and component tolerances. The raw transistor rarely has its Y_{opt} coincide with Y_{in} or the system's characteristic admittance, Y_o .

To minimize the need for external noise matching circuit components, the LNA designer manipulates transistor construction (gate finger multiples, finger dimension, interconnects, and layout), RF feedback, and package parasitics to have Y_{opt} simultaneously converge on Y_{in} and the system's characteristic admittance (see Figures 4 and 5). Careful insertion of source degeneration feedback also improves amplifier stability and linearity at the expense of gain, especially at higher frequencies. Too much or too little feedback, however, degrades stability and performance; therefore, the LNA designer seeks the optimal value. This design feature allows the user to find a much better trade-off between amplifier noise figure, gain, and input return loss.

The trade-off between noise figure and gain can be shown more clearly using gain and noise circles on a Smith chart. Maximum gain and minimum noise figure rarely occur at the same impedance state. The circuit designer, therefore, must decide on matches that provide the desired gain and noise figure. The choice of impedance must also take into consideration the location of input and output stability circles so that a potentially unstable circuit is avoided. The stability circles, however, often lie outside the Smith chart, so any choice of impedance results in unconditional stability.

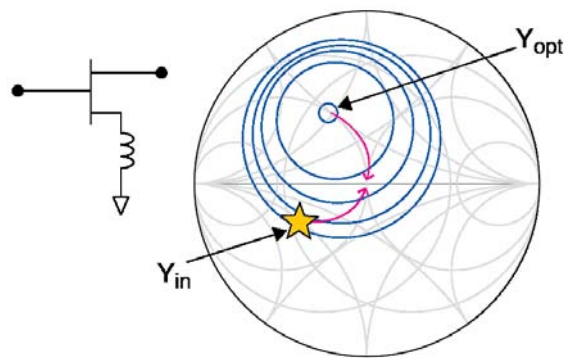


Figure 4. Source Degeneration Feedback on Common-Source Configuration

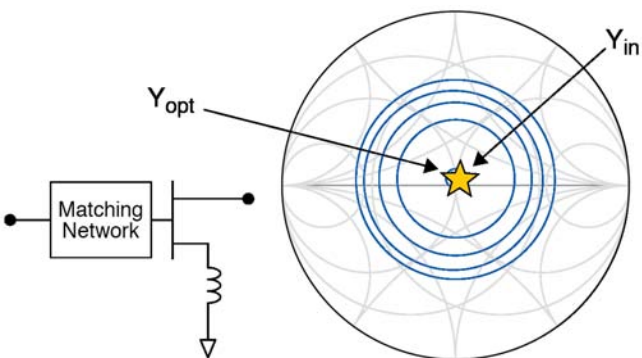


Figure 5. Input Match with Good Input Impedance and Optimal NF Performance

The common-gate amplifier also has a low noise figure (particularly at lower frequencies), but the noise figure increases rapidly with signal frequency. The high drain-source capacitance in common-gate implementations requires inductive feedback, which serves to improve noise figure, gain, and stability at higher frequencies.

The cascode amplifier combines the common-source stage previously described with a common-gate transistor designed for optimal linearity. The cascode amplifier, however, becomes greater than the sum of its parts when the common-source transistor is also designed to pre-distort the common-gate transistor's AM-PM characteristics. These design features greatly ease LNA implementation and improve stability, bandwidth, and linearity.

Process Technologies

The most popular active devices used in LNAs are based on GaAs pHEMTs and SiGe BiCMOS process technologies. Performance differences between the two technologies are shown in Table 3.

Table 3. Comparison of Device Technologies for L- and S-Band LNAs

Typical Performance	GaAs pHEMT	SiGe BiCMOS
Noise Figure (dB)	≥ 0.4	≥ 0.9
Gain (dB)	12 to 21	10 to 17
OIP3 (dBm)	≥ 41	≥ 31
Breakdown Voltage (Vdc)	15	much less than 15 V
Inductor Q-factor	15	5 to 10
Strengths	High P1dB and OIP3, very low noise figure	Higher integration, lower cost, ESD immunity
f_T/f_{MAX}	Similar	

GaAs pHEMT devices generate very little noise due to the heterojunction between the doped AlGaAs layer and the extremely thin undoped GaAs layer, but the real advantage of GaAs is in gain linearity. Today's SiGe process technology is comparable to GaAs devices in terms of usable frequency range, but the relatively low breakdown voltage of SiGe devices limits dynamic range. GaAs pHEMT has clear advantages over SiGe implementations in terms of noise figure and linearity performance, whereas SiGe can operate much more efficiently and has cost advantages due to higher levels of integration. As with any device technology, the relative advantages and disadvantages of each must be evaluated within the context of a specific application.

To understand how process technologies differ in practice, consider the attributes of 30 commercially available LNAs MMICs produced by various manufacturers. All 30 devices operate within the 1400–2200 MHz frequency range, but each device does not share a common application. As a result, each design differs in performance optimization and trade-offs. That difference prevents direct comparisons between devices. Observations, however, limited to general characteristics of SiGe and GaAs designs are still relevant.

Figures 6 and 7 illustrate the performance trade-offs between OIP3 versus noise figure and OIP3 versus power consumption, respectively. Figure 6 illustrates that GaAs pHEMT devices generally have a higher OIP3 and lower noise figure than SiGe BiCMOS devices because they are designed to operate at higher power consumption levels. Figure 7 illustrates the clear distinction between how the technologies are used for mobile applications, where power budgets are very low, and other applications, where higher power consumption affords the opportunity to achieve LNAs with higher linearity.

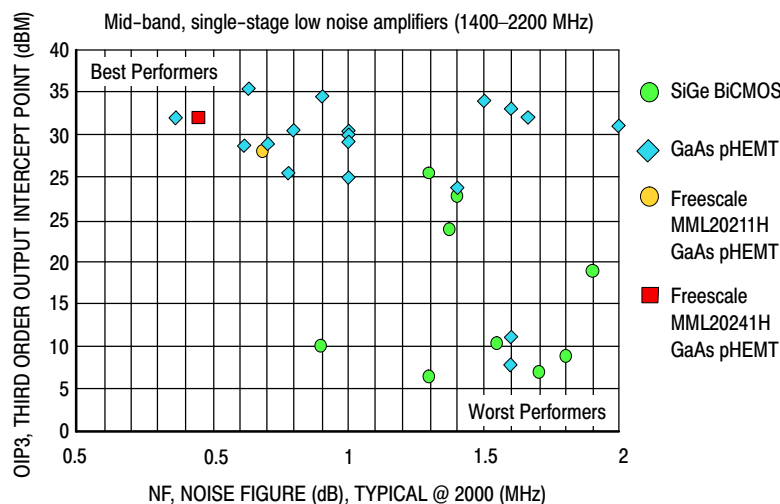


Figure 6. Third Order Output Intercept Point versus Noise Figure

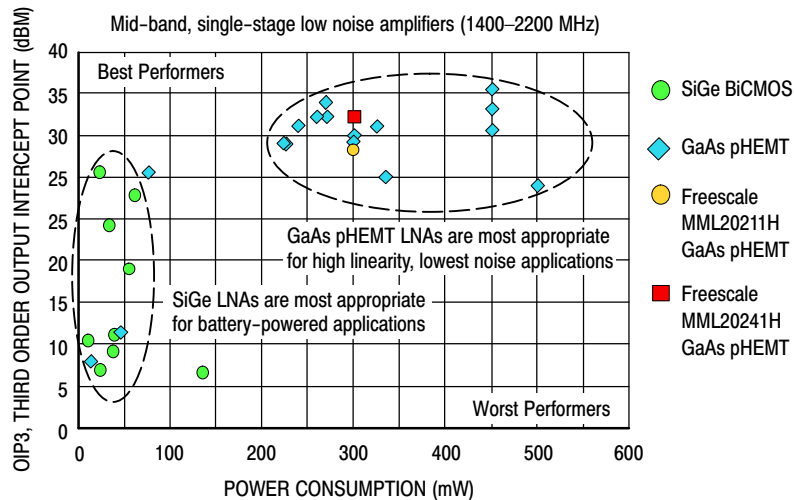


Figure 7. Third Order Output Intercept Point versus Power Consumption

GaAs pHEMT LNAs generally exhibit a much more optimal combination of high linearity and low noise when compared to SiGe implementations. GaAs pHEMT devices vary widely in power consumption compared to SiGe devices, which consume much less. GaAs pHEMT technology is best suited to applications in which optimization of receiver sensitivity is the foremost concern, such as in cellular base stations. SiGe LNAs, on the other hand, are best suited to applications in which sensitivities to power consumption and cost figure more prominently.

Transistor Geometry and Package Parasitics

Beyond the choice of process technology, LNA noise figure performance is significantly affected by transistor design and package parasitics. Although a transistor can be constructed for a perfect $50\ \Omega$ match, a specific transistor design also exists at which Y_{opt} is closer to Y_{in} while minimizing R_n . Shrinking transistor sizing improves power consumption, but often at the expense of degraded NF_{min} and IP3 performance. Alternative dimensioning, such as narrower and shorter gate fingers on a field effect transistor (FET), can sometimes improve the noise figure by lowering gate resistance and high-frequency gain; stability also improves. Wider gate width or gate finger multiples increase transistor transconductance. As transistor aspect ratios take advantage of newer process technology nodes, however, these intrinsic relationships between electrical characteristics and transistor construction start to become muddled as device parasitics become more significant.

Package parasitics grow as frequency increases. Physical structures, such as bond-wires and bond-pads along with package capacitance, often dominate package parasitics and have a direct effect on the noise figure, input-impedance matching, and transistor transconductance. The designer must mitigate the effects of each of these elements; some tight process controls can even turn these structures into constructive design elements. Carefully controlled bond-wire placement and length can be used as input-matching elements or to provide source degeneration.

BOARD-LEVEL CONSIDERATIONS

The RF circuit designer must also consider board level variables when designing with an LNA. Designing an LNA on a printed circuit board (PCB) requires balancing a different set of variables that can have a significant effect on LNA performance: PCB layout, bias setting, input/output (impedance) matching, EM shielding, and supply decoupling.

Starting with PCB layout, the designer should take care in designing the printed structures between the antenna and the LNA input. Some good reference guides are available for the layout of low-noise circuits.³ Some noteworthy low-noise PCB layout practices are the following:

- Maintain controlled RF impedances along shielded signal traces. Coplanar waveguides are recommended over microstrip transmission lines.
- Isolate noisy circuits from sensitive circuits with separate ground planes and signals routed on separate shielded layers.
- Minimize parasitic inductance for currents passing along/across planar voids and copper islands with low-inductance ties to the RF ground plane.
- Avoid lossy elements along the signal path up to the LNA input.
- Dampen digital/noisy signal lines with series resistance.
- Avoid routing low-noise and sensitive signals across planar voids.
- Decouple dc supplies with a network of two or three capacitors with the smallest value nearest the device lead.
- Tie the N.C. pins to ground, unless otherwise directed by the data sheet.

Bias Setting

Setting the LNA bias is the first most critical step in implementation. Most LNA MMICs have an integrated active-bias circuit that regulates bias currents over variations in supply voltage, temperature, and FET threshold voltage. Careful selection of a bias point, however, is still required to find the best compromise between gain, NF, and linearity for any given application.

Consider the biasing characteristics of Freescale's MML09211H LNA shown in Figure 8. The optimal noise figure for this LNA is 9% of $I_{D(max)}$, with the maximum gain occurring at approximately 31% of the $I_{D(max)}$. OIP3 performance approaches optimality near 27% of $I_{D(max)}$. It is up to the designer to find the most appropriate balance between OIP3, gain, and noise figure performance. A designer of a cellular base station receiver would probably choose a bias point favoring the highest levels of linearity: a drain current somewhere between 20% and 25% of $I_{D(max)}$.

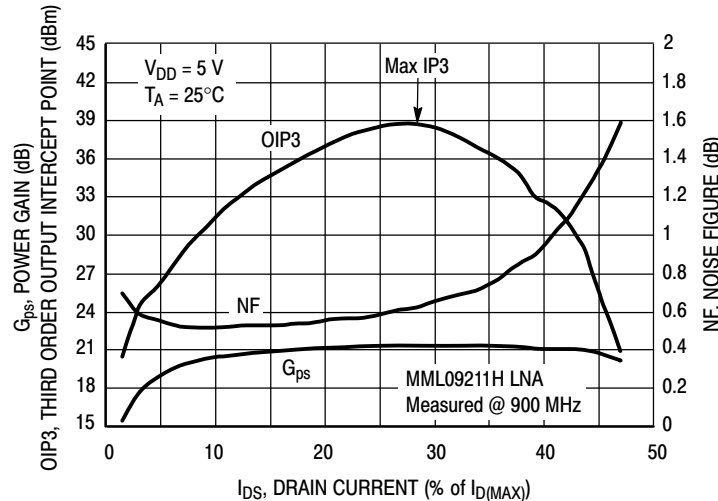


Figure 8. Power Gain, Third Order Output Intercept Point, and Noise Figure versus Drain Current

Input and Output Matching

The LNA designer tries to provide a versatile solution that delivers optimal levels of performance with little fuss. Careful design produces a device with well-controlled input and output impedances at which the optima of various important performance characteristics come close to coinciding. The MML series of Freescale LNAs are good examples.⁴

There are several important considerations when approaching the task of input matching. Noise figure degradation can be mitigated by limiting the number of elements between the antenna and LNA input. A high-Q input matching network provides an optimal noise figure and gain performance because of the minimal loss, but these networks are often quite sensitive to variations in process, voltage, temperature, and component value.

LNA noise parameters guide the designer to an optimal input match. Generally, the input match is a compromise between noise figure, gain, and input return loss. With a well-designed LNA, this should not require too much compromise.

On the output, optimal OIP3 and maximum gain do not usually coincide. Load-pull techniques are used to determine an output match that provides an appropriate trade-off between gain, OIP3, and P1dB in the same way as for a power amplifier.

An LNA with lesser reverse isolation ($S_{12} > -40$ dB) might require some iterative (back-and-forth) tuning between input and output. Greater reverse isolation eases the task of impedance matching and improves amplifier stability.

Stability

Radio receiver design that uses MMIC LNAs no longer requires the user to have the specialized knowledge, skills, or equipment that discrete LNA design once did. It is still up to the user, however, to verify the integrity of each design, and no design is ever complete without checking the amplifier stability over the full range of operating conditions. Designers are encouraged to use stability circles to verify chosen source and load impedances well beyond the frequency band of interest and to check both large- and small-signal stability. Large-signal stability is verified by monitoring the LNA output at an input signal corresponding to 1 dB gain compression. Any spectral components that occur as spurs or humps in the noise floor that cannot be explained as signal distortion should be investigated.

Amplifier instability is most often traceable to one of the following causes:

- Insufficient RF isolation between supply lines of successive amplifier stages that provide a path for positive feedback
- Excessive parasitic inductance on ground connections
- Excessive in-band or out-of-band gain

- Insufficiently decoupled supply lines
- Electromagnetic coupling into the LNA (usually remedied by shielding)

Stability compensation is usually implemented with RF feedback to filter excessive out-of-band gain. Resistive damping also can be applied. It makes sense to use lossy stabilization techniques only after filtering and feedback techniques are applied. Resistance at the output is always preferable to resistance on the input. It also might be possible to use source (emitter) inductive loading to improve stability. This option, however, presents additional trade-offs in gain and noise figure that can be undesirable.

CONCLUSION

At a system level, receiver sensitivity is dominated by noise figure and linearity. Receiver dynamic range is dependent on LNA dynamic range, linearity, and gain. Receivers operating amid strong interferers must either filter blockers or suppress the resultant cross-modulation products by optimizing receiver linearity, which comes at the expense of power consumption and degraded noise performance. LNA design requires a sophisticated understanding of both the transistor properties and realizable advantages of viable semiconductor process technologies. It is up to the LNA designer to balance the design trade-offs and mitigate sensitivities to operating conditions while providing an easily implementable device that can accommodate the varied requirements of the targeted applications. The LNA designer's challenge is to provide a MMIC solution that meets the application's requirements with as little fuss as possible.

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3. Arthur T. Bradley et al., "Reducing Printed Circuit Board Emissions with Low-Noise Design Practices," IEEE Conference Publications, pp. 613–616, 2012.
4. Freescale MML series of LNA data sheets and reference designs. (Technical documentation, including data sheets and application notes, for Freescale RF Low Power product can be found at: <http://freescale.com/RFlowpower>. Enter the applicable Document Number into "Keyword" search for quickest results. Reference designs can be found at <http://freescale.com/RFMMIC> > Design Support.)

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