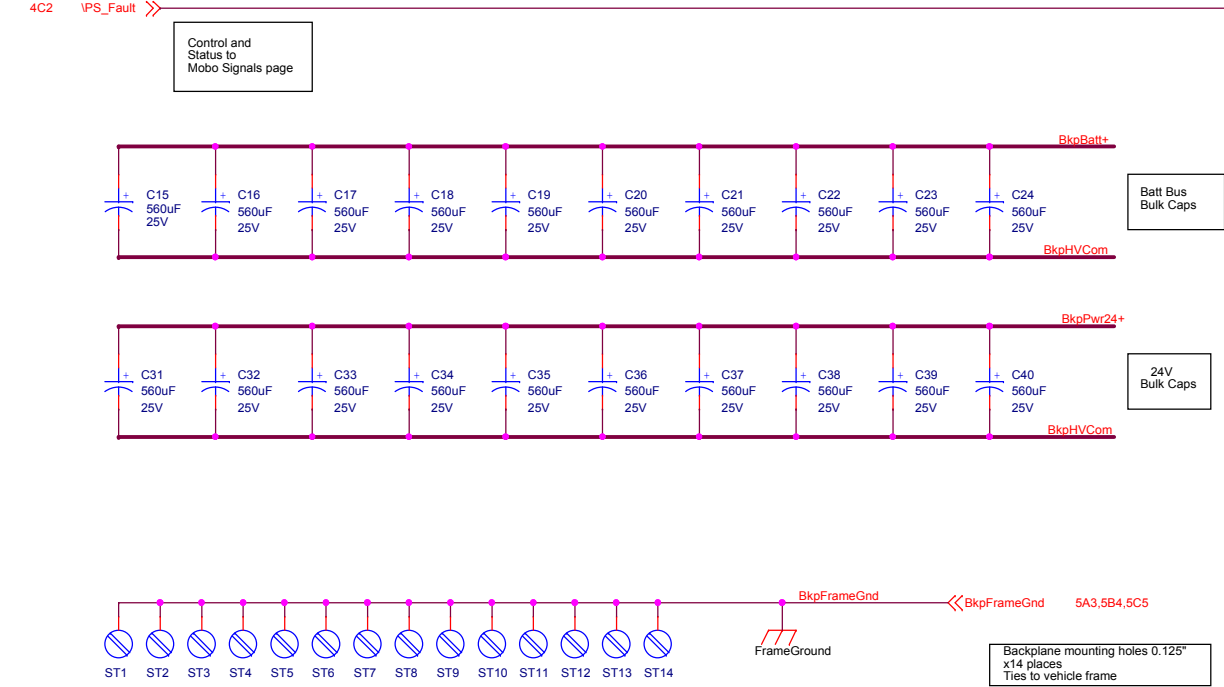
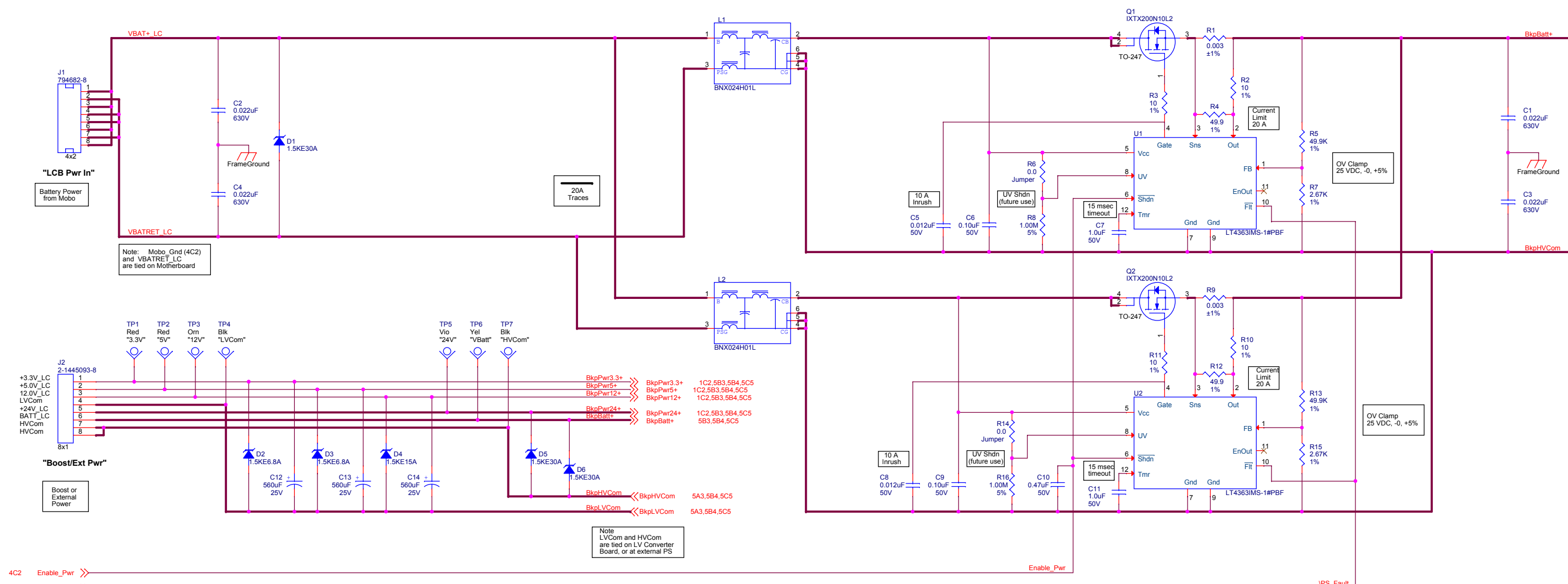






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Title		Document Number		Rev
Schematic, Power Input, Load Control Long Backplane		11021164		A
Size	Date	Engineer	Sheet	of
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Design File		Layout File		
Schematic Name		Page Name	Layout File	
11021164_LoadCtrlLongBackplane		01 Power Input	<Layout File>	

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Motherboard
signal names (ref)

LC_BOARD_SELECT_0
LC_BOARD_SELECT_1
LC_BOARD_SELECT_2
LC_BOARD_SELECT_3
LC_BOARD_SELECT_4
LC_BOARD_SELECT_5
LC_BOARD_SELECT_ENABLE
/RESOUT_LC
SPI2_MOSI
Mobo Gnd
SPI2_SCLK
Mobo Gnd
ENABLE_PWR_LC
/SPI2_MISO
/SPI2_INT_0
/SPI2_INT_1
/SPI2_INT_2
LC_PS_FAULT
CPU-B_3.15V
CPU-B_3.15V
Mobo Gnd
+3.3V_LC
+5.0V_LC

+12.0V_LC
+24V_LC
Mobo Gnd

Note
Ribbon Connector pin order
is reversed relative to CPU side
due to one-sided flat cable

52030-3029

"Mobo Signals"

+3.3V_LC
+5.0V_LC
+12.0V_LC
+24V_LC

Enable_Pwr_LC

LC_PS_Fault

Mobo Gnd
CPU-B_3.15V

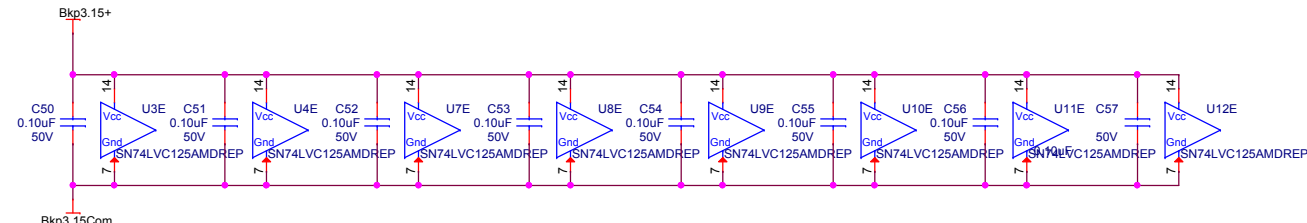
Note: Mobo_Gnd and
VBATRET_LC (5D1)
are tied on Motherboard

"Force On"

Install jumper to
power up for test.
Remove before dive.

Control and
Status to
Current Limiter

Logic Power to
Backplane and
Load Control PIC





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Title Schematic, Mobo Signals, Load Control Long Backplane		Document Number 11021164	Rev A
Size Custom	Date: Friday, July 17, 2015	Engineer Mellinger	Sheet 2 of 5
Design File X:\900739.L\RAUV\PROJECT.DRAWINGS\PROJECT.ESS\DWGS\LOADCONTROL\SUBSYSTEM\BACKPLANE\LONG2013\SCHEMATIC\11021164_LOAD_CONTROL_LONG_BACKPLANE.DWG		Page Name 02 Mobo Signals	Layout File <Layout File>

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