

HEF4104B

Quad low-to-high voltage translator with 3-state outputs

Rev. 9 — 29 March 2016

Product data sheet

1. General description

The HEF4104B is a quad low voltage-to-high voltage translator with 3-state outputs. It provides the capability of interfacing low voltage circuits to high voltage circuits. For example low voltage Local Oxidation Complementary MOS (LOCMOS) and Transistor-Transistor Logic (TTL) to high voltage LOCMOS. It has four data inputs (A0 to A3), an active HIGH output enable input (OE), four data outputs (B0 to B3) and their complements ($\overline{B0}$ to $\overline{B3}$).

With OE = HIGH, the outputs B0 to B3 and $\overline{B0}$ to $\overline{B3}$ are in the low impedance ON-state, either HIGH or LOW as determined by the inputs A0 to A3. With OE = LOW, the outputs B0 to B3 and $\overline{B0}$ to $\overline{B3}$ are in the high-impedance OFF-state.

It uses a common negative supply (V_{SS}) and separate positive supplies for the inputs ($V_{DD(A)}$) and the outputs ($V_{DD(B)}$). $V_{DD(A)}$ must always be less than or equal to $V_{DD(B)}$, even during power turn-on and turn-off. For the permissible operating range of $V_{DD(A)}$ and $V_{DD(B)}$ see [Figure 4](#).

Each input protection circuit is terminated between $V_{DD(B)}$ and V_{SS} . This allows the input signals to be driven from any potential between $V_{DD(B)}$ and V_{SS} , without regard to current limiting. When driving from potentials greater than $V_{DD(B)}$ or less than V_{SS} , the current at each input must be limited to 10 mA.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Inputs and outputs are protected against electrostatic effects
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B

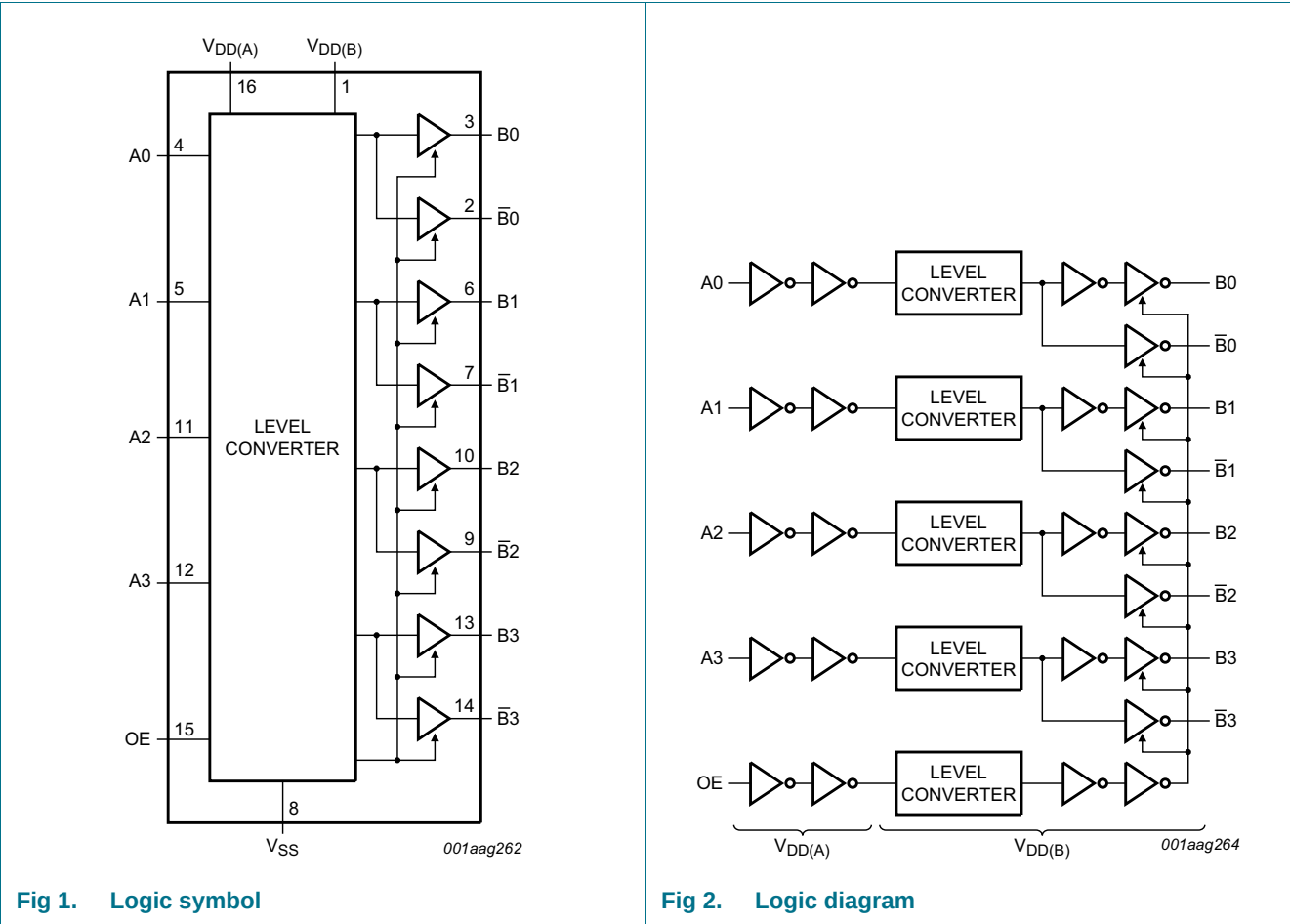
3. Ordering information

Table 1. Ordering information

All types operate from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$.

Type number	Package		
	Name	Description	Version
HEF4104BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

4. Functional diagram



The logic diagram shows the internal structure of the HEF4104B. It consists of four identical stages, one for each bit (0 to 3). Each stage takes an input A_i (A0, A1, A2, or A3) and produces two outputs: B_i and B̄_i. The input A_i is first inverted by a NOT gate. The output of the NOT gate is then connected to a "LEVEL CONVERTER" block. The output of the level converter is connected to a second NOT gate, which produces the final output B_i. The output B̄_i is the complement of B_i. The power supply pins VDD(A) and VDD(B) are shown at the bottom, with VDD(A) connected to the first NOT gate and VDD(B) connected to the second NOT gate. The identifier "001aag264" is located at the bottom right of the diagram.

5. Pinning information

5.1 Pinning

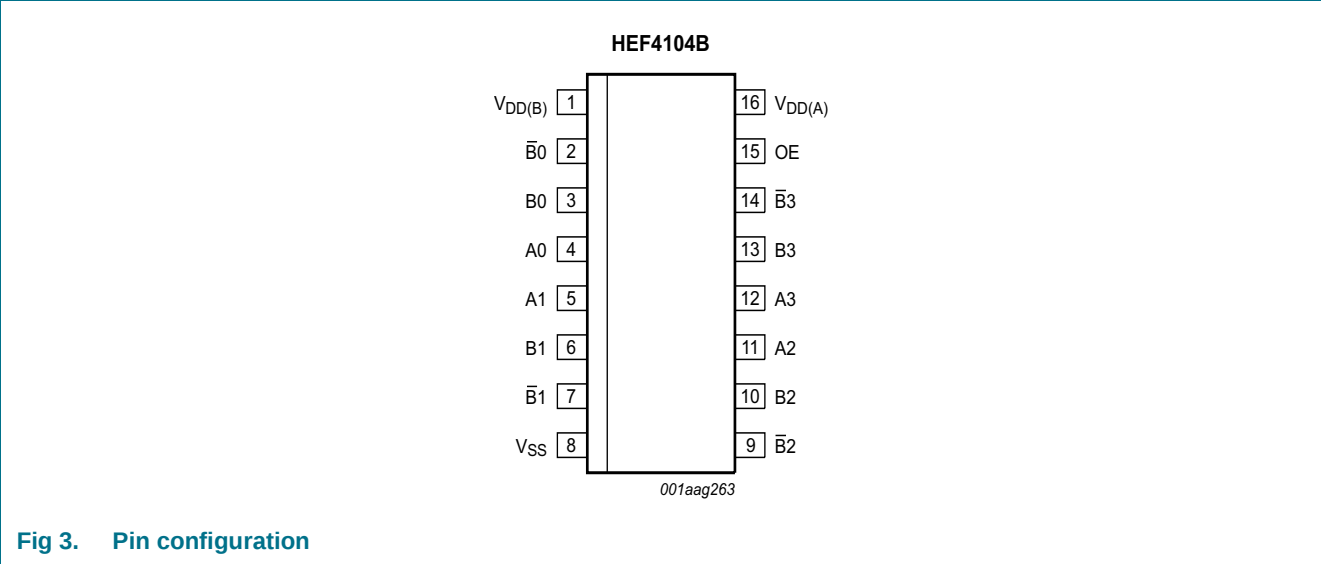


Fig 3. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$V_{DD(B)}$	1	supply voltage port B
$\overline{B0}$ to $\overline{B3}$	2, 7, 9, 14	complementary data output
B0 to B3	3, 6, 10, 13	data output
A0 to A3	4, 5, 11, 12	data input
V_{SS}	8	common negative supply voltage (0 V)
OE	15	output enable input
$V_{DD(A)}$	16	supply voltage port A

6. Functional description

Table 3. Function table^[1]

Control	Output	
OE	Bn	$\overline{Bn}$
H	An	$\overline{An}$
L	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to $V_{SS} = 0$ V (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(A)}$	supply voltage A	port A; $V_{DD(A)} \leq V_{DD(B)}$	-0.5	+18	V
$V_{DD(B)}$	supply voltage B	port B; $V_{DD(B)} \geq V_{DD(A)}$	-0.5	+18	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{DD(A)} + 0.5$ V	-	± 10	mA
V_I	input voltage		-0.5	$V_{DD(A)} + 0.5$	V
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{DD(B)} + 0.5$ V	-	± 10	mA
$I_{I/O}$	input/output current		-	± 10	mA
I_{DD}	supply current	[1]	-	50	mA
T_{stg}	storage temperature		-65	+150	°C
T_{amb}	ambient temperature		-40	+85	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +85 °C			
		SO16 [2]	-	500	mW
P	power dissipation	per output	-	100	mW

[1] I_{DD} is the combined current of $I_{DD(A)}$ and $I_{DD(B)}$.

[2] For SO16 packages: above $T_{amb} = 70$ °C, P_{tot} derates linearly at 8 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD(A)}$	supply voltage A		3	-	$\leq V_{DD(B)}$	V
$V_{DD(B)}$	supply voltage B		$\geq V_{DD(A)}$	-	15	V
V_I	input voltage		0	-	$V_{DD(A)}$	V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD(A)} = 5$ V	-	-	3.75	$\mu\text{s/V}$
		$V_{DD(A)} = 10$ V	-	-	0.5	$\mu\text{s/V}$
		$V_{DD(A)} = 15$ V	-	-	0.08	$\mu\text{s/V}$

9. Static characteristics

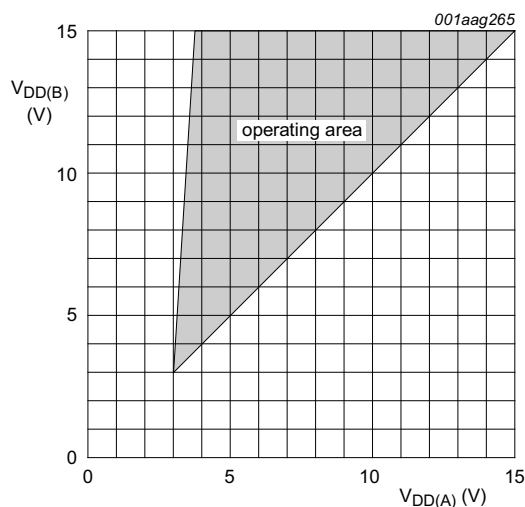
Table 6. Static characteristics

$V_{DD(A)} = V_{DD(B)}$; $V_{SS} = 0$ V; $V_I = V_{SS}$ or $V_{DD(A)}$; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD} ^[1]	$T_{amb} = -40$ °C		$T_{amb} = +25$ °C		$T_{amb} = +85$ °C		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$ I_O < 1$ μ A	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$ I_O < 1$ μ A	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$ I_O < 1$ μ A	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$ I_O < 1$ μ A	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	$V_O = 2.5$ V	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		$V_O = 4.6$ V	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		$V_O = 9.5$ V	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		$V_O = 13.5$ V	15 V	-	-3.6	-	-3.0	-	-2.4	mA
I_{OL}	LOW-level output current	$V_O = 0.4$ V	5 V	0.52	-	0.44	-	0.36	-	mA
		$V_O = 0.5$ V	10 V	1.3	-	1.1	-	0.9	-	mA
		$V_O = 1.5$ V	15 V	3.6	-	3.0	-	2.4	-	mA
I_I	input leakage current		15 V	-	± 0.3	-	± 0.3	-	± 1.0	μ A
I_{DD}	supply current	all valid input combinations; $I_O = 0$ A	5 V ^[2]	-	20	-	20	-	150	μ A
			10 V	-	40	-	40	-	300	μ A
			15 V	-	80	-	80	-	600	μ A
I_{OZ}	OFF-state output current	HIGH level; $V_O = V_{DD(B)}$	15 V	-	1.6	-	1.6	-	12.0	μ A
		LOW level; $V_O = V_{SS}$	15 V	-	-1.6	-	-1.6	-	-12.0	μ A
C_I	input capacitance	digital inputs	-	-	-	-	7.5	-	-	pF

[1] V_{DD} is the same as $V_{DD(A)}$ and $V_{DD(B)}$.

[2] I_{DD} is the combined current of $I_{DD(A)}$ and $I_{DD(B)}$.



The shaded area shows the permissible operating range.

Fig 4. $V_{DD(B)}$ as a function of $V_{DD(A)}$

10. Dynamic characteristics

Table 7. Dynamic characteristics

$T_{amb} = 25\text{ }^{\circ}\text{C}$; for test circuit see [Figure 7](#); unless otherwise specified.

Symbol	Parameter	Conditions	Extrapolation formula ^[1]	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	An to Bn, $\overline{Bn}$; see Figure 5					
		$V_{DD(A)} = V_{DD(B)} = 5\text{ V}$	$143\text{ ns} + (0.55\text{ ns/pF})C_L$	-	170	340	ns
		$V_{DD(A)} = V_{DD(B)} = 10\text{ V}$	$69\text{ ns} + (0.23\text{ ns/pF})C_L$	-	80	160	ns
		$V_{DD(A)} = V_{DD(B)} = 15\text{ V}$	$57\text{ ns} + (0.16\text{ ns/pF})C_L$	-	65	135	ns
t_{PLH}	LOW to HIGH propagation delay	An to Bn, $\overline{Bn}$; see Figure 5					
		$V_{DD(A)} = V_{DD(B)} = 5\text{ V}$	$143\text{ ns} + (0.55\text{ ns/pF})C_L$	-	170	340	ns
		$V_{DD(A)} = V_{DD(B)} = 10\text{ V}$	$69\text{ ns} + (0.23\text{ ns/pF})C_L$	-	80	160	ns
		$V_{DD(A)} = V_{DD(B)} = 15\text{ V}$	$62\text{ ns} + (0.16\text{ ns/pF})C_L$	-	70	140	ns
t_{THL}	HIGH to LOW output transition time	Bn or $\overline{Bn}$; see Figure 6					
		$V_{DD(A)} = V_{DD(B)} = 5\text{ V}$	$10\text{ ns} + (1.00\text{ ns/pF})C_L$	-	60	120	ns
		$V_{DD(A)} = V_{DD(B)} = 10\text{ V}$	$9\text{ ns} + (0.42\text{ ns/pF})C_L$	-	30	60	ns
		$V_{DD(A)} = V_{DD(B)} = 15\text{ V}$	$6\text{ ns} + (0.28\text{ ns/pF})C_L$	-	20	40	ns
t_{TLH}	LOW to HIGH output transition time	Bn or $\overline{Bn}$; see Figure 6					
		$V_{DD(A)} = V_{DD(B)} = 5\text{ V}$	$10\text{ ns} + (1.00\text{ ns/pF})C_L$	-	60	120	ns
		$V_{DD(A)} = V_{DD(B)} = 10\text{ V}$	$9\text{ ns} + (0.42\text{ ns/pF})C_L$	-	30	60	ns
		$V_{DD(A)} = V_{DD(B)} = 15\text{ V}$	$6\text{ ns} + (0.28\text{ ns/pF})C_L$	-	20	40	ns
t_{PHZ}	HIGH to OFF-state propagation delay	OE to Bn, $\overline{Bn}$; see Figure 6					
		$V_{DD(A)} = V_{DD(B)} = 5\text{ V}$		-	70	135	ns
		$V_{DD(A)} = V_{DD(B)} = 10\text{ V}$		-	55	110	ns
		$V_{DD(A)} = V_{DD(B)} = 15\text{ V}$		-	60	120	ns

Table 7. Dynamic characteristics ...continued $T_{amb} = 25\text{ }^{\circ}\text{C}$; for test circuit see [Figure 7](#); unless otherwise specified.

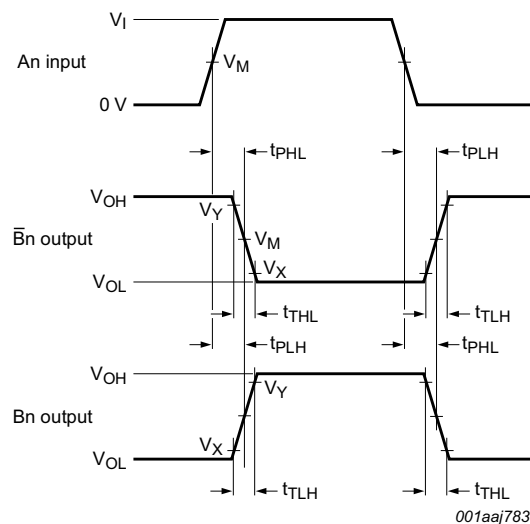
Symbol	Parameter	Conditions	Extrapolation formula ^[1]	Min	Typ	Max	Unit
t_{PLZ}	LOW to OFF-state propagation delay	OE to Bn, $\overline{Bn}$; see Figure 6					
		$V_{DD(A)} = V_{DD(B)} = 5\text{ V}$		-	70	135	ns
		$V_{DD(A)} = V_{DD(B)} = 10\text{ V}$		-	55	105	ns
		$V_{DD(A)} = V_{DD(B)} = 15\text{ V}$		-	55	110	ns
t_{PZH}	OFF-state to HIGH propagation delay	OE to Bn, $\overline{Bn}$; see Figure 6					
		$V_{DD(A)} = V_{DD(B)} = 5\text{ V}$		-	195	395	ns
		$V_{DD(A)} = V_{DD(B)} = 10\text{ V}$		-	95	195	ns
		$V_{DD(A)} = V_{DD(B)} = 15\text{ V}$		-	80	165	ns
t_{PZL}	OFF-state to LOW propagation delay	OE to Bn, $\overline{Bn}$; see Figure 6					
		$V_{DD(A)} = V_{DD(B)} = 5\text{ V}$		-	195	395	ns
		$V_{DD(A)} = V_{DD(B)} = 10\text{ V}$		-	95	190	ns
		$V_{DD(A)} = V_{DD(B)} = 15\text{ V}$		-	80	160	ns

[1] Typical value of the propagation delay and output transition time can be calculated with the extrapolation formula (C_L in pF).**Table 8. Dynamic power dissipation** $V_{DD(A)} = V_{DD(B)}$; $V_{SS} = 0\text{ V}$; $t_r = t_f \leq 20\text{ ns}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Symbol	Parameter	V_{DD} ^[1]	Typical formula (μW)	where
P_D	dynamic power dissipation	5 V	$P_D = 3000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF; $\Sigma(f_o \times C_L)$ = sum of the outputs; V_{DD} = supply voltage in V.
		10 V	$P_D = 12200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 31000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	

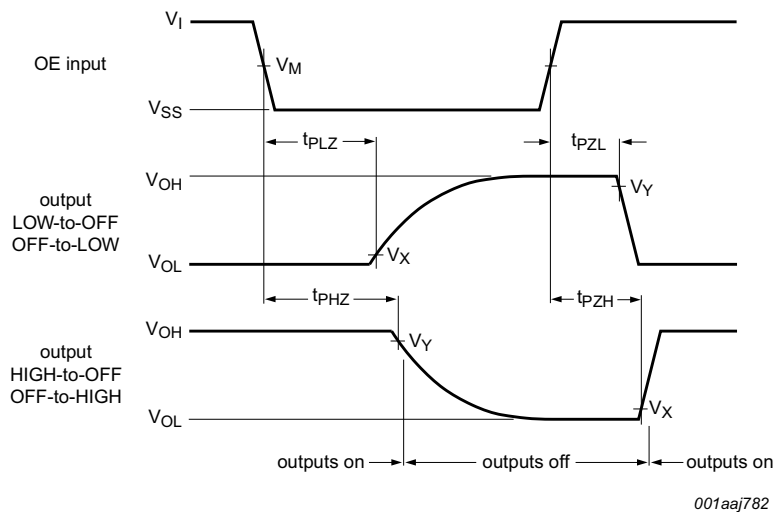
[1] V_{DD} is the same as $V_{DD(A)}$ and $V_{DD(B)}$.

11. Waveforms



Measurement points are given in [Table 9](#).
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 5. Data input (An) to data output (Bn, B̄n) propagation delays and output transition times

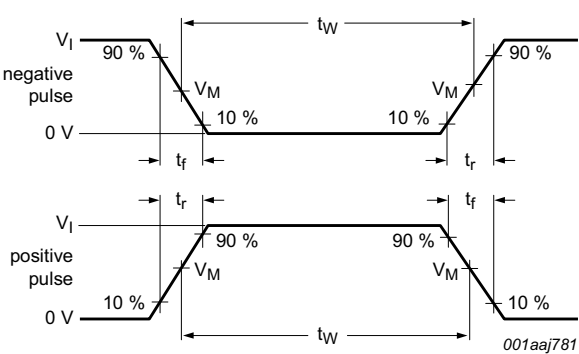


Measurement points are given in [Table 9](#).
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

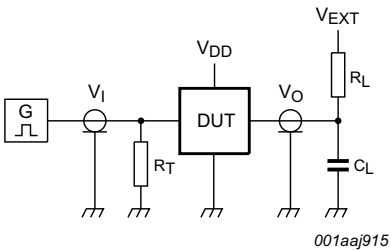
Fig 6. Enable and disable times

Table 9. Measurement points

Input		Output		
V _I	V _M	V _M	V _X	V _Y
V _{SS} or V _{DD(A)}	0.5V _{DD(A)}	0.5V _{DD(B)}	0.1V _{DD(B)}	0.9V _{DD(B)}



a. Input waveforms



b. Test circuit

Test data given in [Table 10](#).
Definitions for test circuit:
DUT = Device Under Test.
 C_L = load capacitance including jig and probe capacitance.
 R_L = load resistance.
 R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig 7. Test circuit for measuring switching times

Table 10. Test data

Supplies	Input	Load		V_{EXT}		
$V_{DD(A)} = V_{DD(B)}$	t_r, t_f	R_L	C_L	t_{PHL}, t_{PLH}	t_{PZL}, t_{PLZ}	t_{PZH}, t_{PHZ}
5 V to 15 V	≤ 20 ns	1 k Ω	50 pF	open	$V_{DD(B)}$	V_{SS}

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

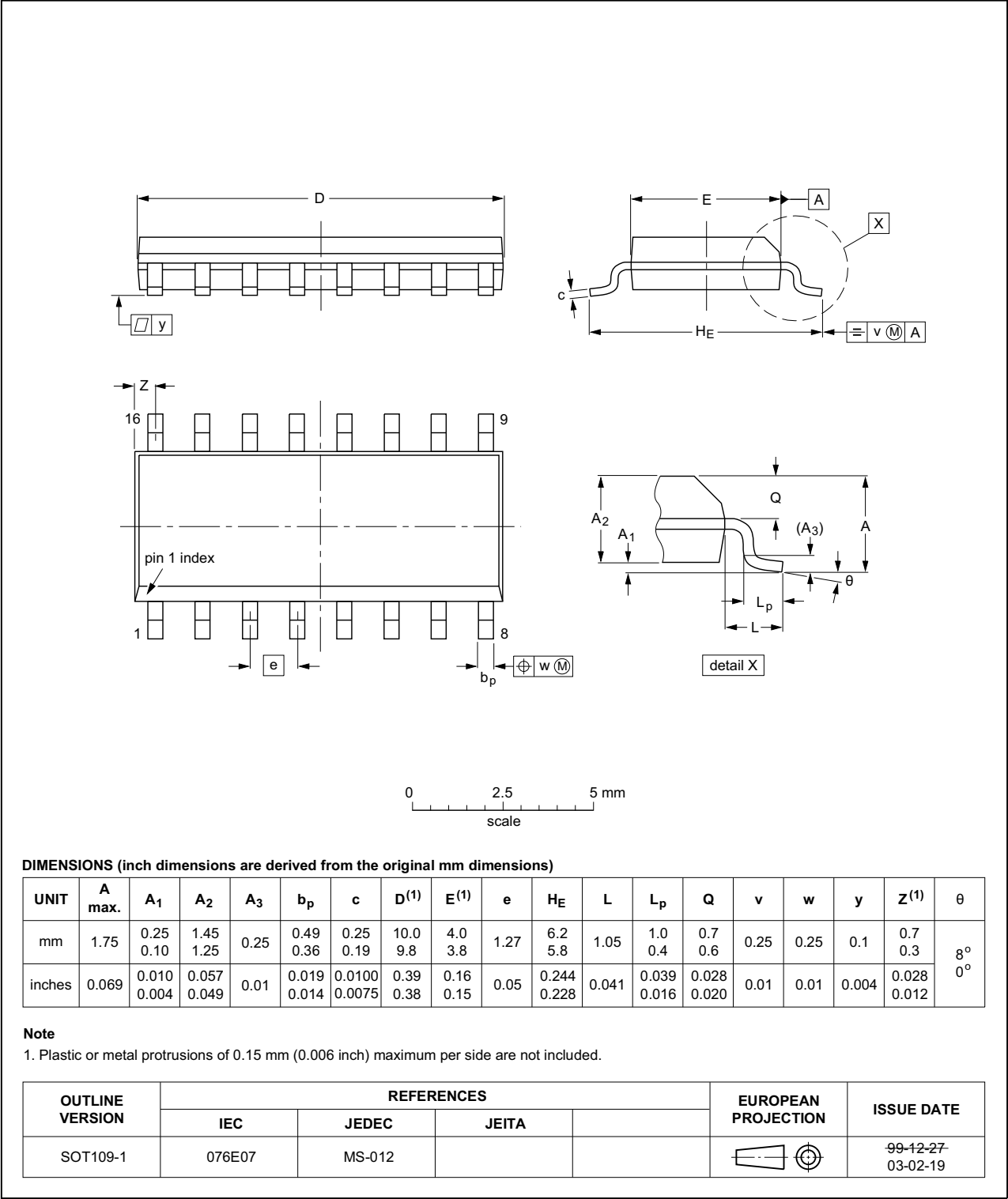


Fig 8. Package outline SOT109-1 (SO16)

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4104B v.9	20160329	Product data sheet	-	HEF4104B v.8
Modifications:	Type number HEF4104BP (SOT38-4) removed.			
HEF4104B v.8	20111111	Product data sheet	-	HEF4104B v.7
Modifications:	- Section Applications removed Table 6: I_{OH} minimum values changed to maximum			
HEF4104B v.7	20091216	Product data sheet	-	HEF4104B v.6
HEF4104B v.6	20091102	Product data sheet	-	HEF4104B v.5
HEF4104B v.5	20090728	Product data sheet	-	HEF4104B v.4
HEF4104B v.4	20090305	Product data sheet	-	HEF4104B_CNV v.3
HEF4104B_CNV v.3	19950101	Product specification	-	HEF4104B_CNV v.2
HEF4104B_CNV v.2	19950101	Product specification	-	-

14. Legal information

14.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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16. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	1
4	Functional diagram	2
5	Pinning information	3
5.1	Pinning	3
5.2	Pin description	3
6	Functional description	3
7	Limiting values	4
8	Recommended operating conditions	4
9	Static characteristics	5
10	Dynamic characteristics	6
11	Waveforms	8
12	Package outline	10
13	Revision history	11
14	Legal information	12
14.1	Data sheet status	12
14.2	Definitions	12
14.3	Disclaimers	12
14.4	Trademarks	13
15	Contact information	13
16	Contents	14