Zimbra **klimov@mbari.org**

Re: timing of daughter card

From : Elecia White <elecia@logicalelegance.com> Wed, Nov 06, 2019 03:02 PM
Subject : Re: timing of daughter card
To : Denis Klimov <klimov@mbari.org>
Cc : Brian Kieft <bkieft@mbari.org>

Hi Denis,

The CS goes to the processor on the IMU dev board. I changed that processor's code to listen to the CN1 connector and modify DB_CS. (See "Why Was IMU More Difficult than Expected?" slide.) There was no direct connection so I had to work around it.

As for INT2
* ICM-20948 pin 19 INT2 to INT_IMU to RD1 on PIC is **used**
* ICM-20948 pin 12 INT1 to IMU_IO1 to RA15 on PIC is **not used**

The the INT1 and INT2 lines also go through the IMU dev board's processor so they can be mirrored on the connector. That is why you can't trace them on the board. The three lines used by the IMU deb board's processor are CS, INT1 and INT2.

INT2 (RD1 on the pic) is functional, if I disconnect the system, IMU data is no longer received.

Unless we need IMU_IO1 for something else, I'd like to keep it attached to the INT1 so that we might use it in the future.

Thanks,
Elecia

On 11/5/19 5:25 PM, Denis Klimov wrote:

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From: "Denis Klimov" <klimov@mbari.org>
To: "Elecia White" <elecia@logicalelegance.com>
Cc: "Brian Kieft" <bkieft@mbari.org>
Sent: Monday, November 4, 2019 1:23:12 PM
Subject: Re: timing of daughter card

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From : Brian Kieft <bkieft@mbari.org> Tue, Nov 05, 2019 02:03 PM
Subject : Re: timing of daughter card
To : Denis Klimov <klimov@mbari.org>

Cc : Elecia White <elecia@logicalelegance.com>
Reply To : Brian Kieft <bkieft@mbari.org>

I'm happy to pick it up any day this week if it works out.

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To: "Elecia White" <elecia@logicalelegance.com>
Cc: "bkieft" <bkieft@mbari.org>
Sent: Tuesday, November 5, 2019 1:57:26 PM
Subject: Re: timing of daughter card

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Denis Klimov

From: "Elecia White" <elecia@logicalelegance.com>
To: "Denis Klimov" <klimov@mbari.org>
Cc: "Brian Kieft" <bkieft@mbari.org>
Sent: Tuesday, October 29, 2019 02:08:56 PM
Subject: Re: timing of daughter card

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Sent: Monday, October 28, 2019 05:34:36 PM
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From : Denis Klimov <klimov@mbari.org> Mon, Nov 04, 2019 04:18 PM
Subject : Re: timing of daughter card 2 attachments
To : Elecia White <elecia@logicalelegance.com>
Cc : Brian Kieft <bkieft@mbari.org>
Reply To : Denis Klimov <klimov@mbari.org>

Hi Elecia,
could you clarify something. The interrupt INT2 signal (pin 19 of ICM-20948) that you are supposedly have wired to /IMU_INT (U23.76 PIC processor on Mother Board) is specified as RESV (Reserved, do not connect) on ICM-20948 datasheet (page 19 of attached file). This is datasheet from DigiKey and it seems to be actual; as TDK website has the same datasheet for this part.

And yet, DK-20948 development board schematic shows this pin as INT2_1V8, which is connected to level shifter, but then going nowhere from there. See attached frame grab of page 6 of schematic. The net name connection is shown in blue line. Perhaps, it is really connected to CN5.1, then by the jumper , to CN5.2 which is signal DB_INT2, connected to CN1.6 where it could be connected to Mother Board by the wire. But i do not see a jumper on CN5 header on your photo either .

So are you sure this INT2 signal is wired on your prototype and operational?

thanks!

Denis Klimov

From: "Denis Klimov" <klimov@mbari.org>
To: "Elecia White" <elecia@logicalelegance.com>
Cc: "Brian Kieft" <bkieft@mbari.org>
Sent: Monday, November 4, 2019 1:23:12 PM
Subject: Re: timing of daughter card

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Sent: Monday, November 4, 2019 11:27:21 AM
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2019-11-03-DK-20948-Page-6-Commented.jpg
1 MB

DS-000189-ICM-20948-v1.3-1385562-Commented.pdf
2 MB

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> **To:** "Denis Klimov" <klimov@mbari.org>
> **Cc:** "Brian Kieft" <bkieft@mbari.org>
> **Sent:** Tuesday, October 29, 2019 02:08:56 PM
> **Subject:** Re: timing of daughter card
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To: "Brian Kieft" <bkieft@mbari.org>, "Denis Klimov" <klimov@mbari.org>
Sent: Monday, October 28, 2019 05:34:36 PM
Subject: timing of daughter card

Hello Brian and Denis,

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From : Denis Klimov <klimov@mbari.org> Mon, Nov 04, 2019 10:45 AM
Subject : Re: timing of daughter card 1 attachment
To : Elecia White <elecia@logicalelegance.com>
Cc : Brian Kieft <bkieft@mbari.org>
Reply To : Denis Klimov <klimov@mbari.org>

Elecia,
(1) - sounds good!
In regards to (2), I am not quite getting what did you mean by this: " as booting the IMU shouldn't be done after deployment."
The way I understood your comment on slide 2 "...No reset so FW control of VDD would be nice..." is that IMU could possibly be frozen or non-responsive occasionally. As you noted, it does not have a reset input, so we could implement VDD control by the processor on the Mother Board, where you could remove the power from IMU and then power it again, thus resetting internal registers of IMU. At least for me, that makes sense. This was exactly done on the old Persistor-based configuration with MPU-6050 bridge board. See page 3 of attached schematic 10020895-MOB1. The power to bridge board pin U18A.10 was applied thru FET pair U15A, B, controlled by signal TPU2 from U14C.23.
So you could have a watchdog with timer or something, and if IMU is not responsive, then reboot it.
I am going to use 3.3V to 1.8V linear regulator to power IMU, so wiring its enable input to /IMU_ENBL would be easy way to achieve this power-reboot.

In regards to (4), I like your idea of using IMU_IO2 for independent control of level shifters. That way you would have more control of power- reboot process.

thanks,

Denis Klimov

From: "Elecia White" <elecia@logicalelegance.com>
To: "Denis Klimov" <klimov@mbari.org>
Cc: "Brian Kieft" <bkieft@mbari.org>
Sent: Monday, November 4, 2019 9:00:19 AM
Subject: Re: timing of daughter card

Hi Denis,

1) Yes, 8 wires.

2) I am not currently using IMU_ENABLE so this is ok. However, it may be better to just control the level shifters as booting the IMU shouldn't be done after deployment.

4) We don't need the other signals, perhaps IMU_IO2 should control the level shifters while IMU_ENABLE controls the VDD to the IMU chip?

Thanks,
Elecia

On 11/1/19 2:12 PM, Denis Klimov wrote:

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Sent: Tuesday, October 29, 2019 3:39:56 PM
Subject: Re: timing of daughter card

It was not one of the original action items, no.

As with file compression, I have worked on it because it was requested, it seems like I have enough budget, and it seemed like it may be of good benefit. However, while working on it I considered that without a motherboard spin, there are only two unfixed channels (the temperature channels) and those can be handled in the code without adding the complexity of a reading in a config file. The complexity really comes in when you consider misspelling a sensor in the file and not being able to record it to sysrec because it wasn't identified correctly. There are too many things that can go wrong and not enough benefit to the system to correct them, particularly as the data is saved in ADC counts and gets set to engineering units in the PC-side program anyway. It is a lot of code for something that saves humans a minute with a calculator.

There are other, more critical things that I should use the time on (like making it so the zmodem settings are not fixed to inappropriate values and making a test plan that reduces risk).

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10020895-MOB1-2013-05-16.Rev1.pdf
86 KB

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