Zimbra **klimov@mbari.org**

Re: timing of daughter card

From : Elecia White <elecia@logicalelegance.com> Thu, Nov 21, 2019 11:07 AM
Subject : Re: timing of daughter card
To : Denis Klimov <klimov@mbari.org>, Brian Kieft <bkieft@mbari.org>

I plan to review the schematics tomorrow morning. I am not good with mechanical drawings so I'm not sure I'll have any comments on that though I will review it.

The IMU is in 9-axis mode. We could opt to sleep with the accels on only to decrease power usage as needed, only running gyros and mags when an event happens.

Yes, I can get the temperature on the IMU.

Thanks,
Elecia

On 11/21/19 10:50 AM, Denis Klimov wrote:

> Hi Elecia,
> couple of questions:
> - you are running IMU in 9-axis mode, correct? (The mode affects power consumption, that is why I am asking)
> - ICM-20948 is specified to have embedded digital temperature sensor, do you know if you can query it?
>
> Denis Klimov
>
> ---
>
> **From:** "Denis Klimov" <klimov@mbari.org>
> **To:** "Elecia White" <elecia@logicalelegance.com>
> **Cc:** "Brian Kieft" <bkieft@mbari.org>
> **Sent:** Wednesday, November 20, 2019 4:52:51 PM
> **Subject:** Re: timing of daughter card
>
> Elecia,
> please see the draft of schematic and mechanical drawing. We should have footprints and parts symbols with properties done tomorrow.
>
> Outstanding:
> - Decide if we go with simple control logic where we control /Tri-state and /IMU_ENBL separately, or use some sort of logic to control /Tri-state signal automatically based on available 1.8V power.
> - Power budget/ power draw summary. One issue, is level shifters are drawing quite a bit of power, and would do it continously in this design (no power down).
> - Make sure signals are correct voltage, connectivity, and logic (straight/ inverted)
> - Associate passives with the ones from database
> - Design rules check
> - Transfer to layout.
>
> Denis Klimov
>
> ---
>
> **From:** "Denis Klimov" <klimov@mbari.org>
> **To:** "Elecia White" <elecia@logicalelegance.com>
> **Cc:** "Brian Kieft" <bkieft@mbari.org>
> **Sent:** Tuesday, November 19, 2019 9:45:04 AM
> **Subject:** Re: timing of daughter card

Elecia,
thank you sending the detailed explanation how those 3 signals are making it between 2 boards. Exactly the thing I was not sure of.
Since I have a prototype here, here is a sketch of the connectivity between boards attached. Some wires fell of during transporting/ handinlg, I did restored connectvity and hope it is correct.
I will mount the loose board and you could have a prototype back tomorrow.

Denis Klimov

From: "Elecia White" <elecia@logicalelegance.com>
To: "Denis Klimov" <klimov@mbari.org>
Cc: "Brian Kieft" <bkieft@mbari.org>
Sent: Wednesday, November 6, 2019 3:02:09 PM
Subject: Re: timing of daughter card

Hi Denis,

The CS goes to the processor on the IMU dev board. I changed that processor's code to listen to the CN1 connector and modify DB_CS. (See "Why Was IMU More Difficult than Expected?" slide.) There was no direct connection so I had to work around it.

As for INT2
* ICM-20948 pin 19 INT2 to INT_IMU to RD1 on PIC is **used**
* ICM-20948 pin 12 INT1 to IMU_IO1 to RA15 on PIC is **not used**

The the INT1 and INT2 lines also go through the IMU dev board's processor so they can be mirrored on the connector. That is why you can't trace them on the board. The three lines used by the IMU deb board's processor are CS, INT1 and INT2.

INT2 (RD1 on the pic) is functional, if I disconnect the system, IMU data is no longer received.

Unless we need IMU_IO1 for something else, I'd like to keep it attached to the INT1 so that we might use it in the future.

Thanks,
Elecia

On 11/5/19 5:25 PM, Denis Klimov wrote:

> It would be soo cool if you Brian could bring it!
> I have issue with one more signal (/CS_1V8; SN_CS); just have no idea how it gets to conenctor CN1 and becomes DB_CS. Yet, this is where it mostlikely connected to Mother Board /IMU_CS signal. And it got to be there since it is hard to imagine how the SPI interface could work without Chip Select.
> So the prototype here would be very helpful in nailing the Bridge Board from first try.
>
> thanks,
>
> Denis Klimov
>
> ---
>
> **From:** "Elecia White" <elecia@logicalelegance.com>
> **To:** "Brian Kieft" <bkieft@mbari.org>
> **Cc:** "Denis Klimov" <klimov@mbari.org>
> **Sent:** Tuesday, November 5, 2019 3:19:16 PM
> **Subject:** Re: timing of daughter card

Sure! This week is open. Text me (408)839-8479 but I'll likely be here.

On Nov 5, 2019, at 2:04 PM, Brian Kieft <bkieft@mbari.org> wrote:

I'm happy to pick it up any day this week if it works out.

From: "Denis Klimov" <klimov@mbari.org>
To: "Elecia White" <elecia@logicalelegance.com>
Cc: "bkieft" <bkieft@mbari.org>
Sent: Tuesday, November 5, 2019 1:57:26 PM
Subject: Re: timing of daughter card

Hi Elecia
I had being thinking, if we could borrow your prototype for several days, it would be easier for me to figure out the connectivity and make sure footprints are correct. Do not need it working here. Just a hardware with wires in a last working configuration.
Brian said he could swing by your place to pick it up.

Would it be possible this week?

thanks!

Denis Klimov

From: "Denis Klimov" <klimov@mbari.org>
To: "Elecia White" <elecia@logicalelegance.com>
Cc: "Brian Kieft" <bkieft@mbari.org>
Sent: Monday, November 4, 2019 4:18:17 PM
Subject: Re: timing of daughter card

Hi Elecia,
could you clarify something. The interrupt INT2 signal (pin 19 of ICM-20948) that you are supposedly have wired to /IMU_INT (U23.76 PIC processor on Mother Board) is specified as RESV (Reserved, do not connect) on ICM-20948 datasheet (page 19 of attached file). This is datasheet from DigiKey and it seems to be actual; as TDK website has the same datasheet for this part.

And yet, DK-20948 development board schematic shows this pin as INT2_1V8, which is connected to level shifter, but then going nowhere from there. See attached frame grab of page 6 of schematic. The net name connection is shown in blue line. Perhaps, it is really connected to CN5.1, then by the jumper , to CN5.2 which is signal DB_INT2, connected to CN1.6 where it could be connected to Mother Board by the wire. But i do not see a jumper on CN5 header on your photo either .

So are you sure this INT2 signal is wired on your prototype and operational?

thanks!

Denis Klimov

From: "Denis Klimov" <klimov@mbari.org>

To: "Elecia White" <elecia@logicalelegance.com>
Cc: "Brian Kieft" <bkieft@mbari.org>
Sent: Monday, November 4, 2019 1:23:12 PM
Subject: Re: timing of daughter card

ok sounds good - let me play with logic and see how to implement a reliable reboot without bogging down the comms on SPI bus. I will keep separate control of tri-state input of level shifters still open for now. If a good reset controller or power supervisor is used, then I might as well use automatic logic control of tri-state input without the need for you to control those 2 inputs separately with some requirements for timing between application of those signals...

thanks,

Denis Klimov

From: "Elecia White" <elecia@logicalelegance.com>
To: "Denis Klimov" <klimov@mbari.org>
Cc: "Brian Kieft" <bkieft@mbari.org>
Sent: Monday, November 4, 2019 11:27:21 AM
Subject: Re: timing of daughter card

Hi Denis,

Ahh, yes, I did want reset to deal with catastrophic issues.

Sounds good, thanks,
Elecia

On 11/4/19 10:45 AM, Denis Klimov wrote:

> Elecia,
> (1) - sounds good!
> In regards to (2), I am not quite getting what did you mean by this: " as booting the IMU shouldn't be done after deployment."
> The way I understood your comment on slide 2 "...No reset so FW control of VDD would be nice..." is that IMU could possibly be frozen or non-responsive occasionally. As you noted, it does not have a reset input, so we could implement VDD control by the processor on the Mother Board, where you could remove the power from IMU and then power it again, thus resetting internal registers of IMU. At least for me, that makes sense. This was exactly done on the old Persistor-based configuration with MPU-6050 bridge board. See page 3 of attached schematic 10020895-MOB1. The power to bridge board pin U18A.10 was applied thru FET pair U15A, B, controlled by signal TPU2 from U14C.23.
> So you could have a watchdog with timer or something, and if IMU is not responsive, then reboot it.
> I am going to use 3.3V to 1.8V linear regulator to power IMU, so wiring its enable input to /IMU_ENBL would be easy way to achieve this power-reboot.
>
> In regards to (4), I like your idea of using IMU_IO2 for independent control of level shifters. That way you would have more control of power- reboot process.
>
> thanks,

Denis Klimov

From: "Elecia White" <elecia@logicalelegance.com>
To: "Denis Klimov" <klimov@mbari.org>
Cc: "Brian Kieft" <bkieft@mbari.org>
Sent: Monday, November 4, 2019 9:00:19 AM
Subject: Re: timing of daughter card

Hi Denis,

1) Yes, 8 wires.

2) I am not currently using IMU_ENABLE so this is ok. However, it may be better to just control the level shifters as booting the IMU shouldn't be done after deployment.

4) We don't need the other signals, perhaps IMU_IO2 should control the level shifters while IMU_ENABLE controls the VDD to the IMU chip?

Thanks,
Elecia

On 11/1/19 2:12 PM, Denis Klimov wrote:

> Hi Elecia,
> several questions:
> (1) Please confirm if there are 8 wires connected to DK-20948 development board on your prototype? Two wires are +5V and GND, and 6 are signals. Please see Slide 7 on attached file "20191007 IMU Daughter Design Notes-Commented-2019-11-01-DK.pptx". I could not quite tell from the photo you sent earlier (also attached) if my wire count is correct.
> (2) I am proposing to use U18A.A6 /IMU_ENBL signal on the Mother Board to enable VDD (1.8V) to IMU chip, and also to control Tri-State status of level shifter(s) so when /IMU_ENBL is not active and VDD(1.8V) is not active, the processor lines that go to IMU are not pulled down disrupting SPI Bus 1 that is shared between IMU and RTC on Mother Board
> (3) If (1) and (2) and good, we would have one more signal, IMU_IO2, available on the Mother Board connector U18A where a Bridge Board would be plugged.
> (4) We could leave IMU_IO2 in reserve, or control something else on Bridge Board. There are some pins on ICM-20948 that you are not using presumably: AUXDA, AUXCL; FSYNC; would you benefit from having access to those?
>
> thanks!
>
> Denis Klimov
>
> ---
>
> **From:** "Elecia White" <elecia@logicalelegance.com>
> **To:** "Denis Klimov" <klimov@mbari.org>
> **Cc:** "Brian Kieft" <bkieft@mbari.org>

Sent: Tuesday, October 29, 2019 3:39:56 PM
Subject: Re: timing of daughter card

It was not one of the original action items, no.

As with file compression, I have worked on it because it was requested, it seems like I have enough budget, and it seemed like it may be of good benefit. However, while working on it I considered that without a motherboard spin, there are only two unfixed channels (the temperature channels) and those can be handled in the code without adding the complexity of a reading in a config file. The complexity really comes in when you consider misspelling a sensor in the file and not being able to record it to sysrec because it wasn't identified correctly. There are too many things that can go wrong and not enough benefit to the system to correct them, particularly as the data is saved in ADC counts and gets set to engineering units in the PC-side program anyway. It is a lot of code for something that saves humans a minute with a calculator.

There are other, more critical things that I should use the time on (like making it so the zmodem settings are not fixed to inappropriate values and making a test plan that reduces risk).

-Elecia

On 10/29/19 3:01 PM, Denis Klimov wrote:

> Was not moving ADC sensor config data from code to configuration file, one of action items?
>
> Denis Klimov
>
> ---
>
> **From:** "Elecia White" <elecia@logicalelegance.com>
> **To:** "Denis Klimov" <klimov@mbari.org>
> **Cc:** "Brian Kieft" <bkieft@mbari.org>
> **Sent:** Tuesday, October 29, 2019 02:08:56 PM
> **Subject:** Re: timing of daughter card
>
> Hi Denis,
>
> I hope your father is doing well, I sympathize with the difficulty of parents getting older.
>
> I think you should do reflow soldering. The extra time is worth it to avoid questioning the reliability.
>
> The ADC config will be part of the code (instead of the filesystem) and the two additional channels will be available. It will do what you need.
>
> -Elecia

On 10/29/19 9:48 AM, Denis Klimov wrote:

> Hi Elecia,
> I started working on schematic 2 weeks ago and then our father got into hospital so that is a big distraction. Now I am back to it and should have the schematic for a review in several days. The board itself is rather simple but I am contemplating on assembly. Technically, we just need one bridge board for now, and manual assembly is quick, but I am not sure how sensitive those IMU chips are to hand soldering. Reflow soldering is reliable but that is 3 extra weeks. May be we should try to assemble couple of boards manually.
>
> I think it is better to implement ADC config. We should be able to use 2 existing MOB3 boards for testing and even deployments. Adding external temperature sensor can be done by soldering to test points. The sensor itself would sit remotely on tiny board connected by 3 wires. (5V, AGND, and 0-2.5V signal). All those available on test points.
>
> That being said, I am configuring the board I have here like this, with external temperature sensor and Bridge Board and we will exchange them with the one you have. So please treat those 2 last ADC inputs as actual signals (although you would read them at 0V on your board). Sounds ok?
>
> Thanks!
>
> Denis Klimov
>
> ---
>
> **From:** "Elecia White" <elecia@logicalelegance.com>
> **To:** "Brian Kieft" <bkieft@mbari.org>, "Denis Klimov" <klimov@mbari.org>
> **Sent:** Monday, October 28, 2019 05:34:36 PM
> **Subject:** timing of daughter card
>
> Hello Brian and Denis,
>
> When will the IMU daughter card be in?

I want to make sure I have plenty of time available to integrate and test it. I have about 50% of my initial budget remaining so there is currently enough to do it but I worry. I don't want to fritter away the hours bugging you for updates.

Also, I was working on the ADC config file and realized it is of no use until the motherboard is spun. That being the case, it adds unnecessary complexity. I'm going to stash my modifications so they are available but I don't think it should go into a BEDS release that doesn't include the ability to use the changes.

That said, my next tasks are to focus on testing and documentation, until the IMU daughter card is ready. I plan to make some headway on that this week and then I'll wait for the board to test.

Thanks,
Elecia

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Elecia White

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