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OrCAD 16.2: What's New

Product Version 16.2
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What’s New in OrCAD Capture 16.2

This chapter contains the following sections describing the OrCAD Capture 16.2 (henceforth referred to as Capture) release.

- New Features and Enhancements on page 8
- Fixed CCRs on page 23

New Features and Enhancements

Capture 16.2 release brings you the following new features and enhancements:

- Usability Enhancements on page 8
- Enhanced OrCAD Capture and PCB Editor Integration on page 18
- Improved FPGA Functionality on page 18
- New Annotation Type Option on page 19
- DRC Enhancements on page 19
- Netlist Enhancements on page 19
- L2A Integration in Capture on page 20
- User Interface Updates on page 20

Usability Enhancements

In OrCAD 16.2, OrCAD Capture and OrCAD Capture CIS comes with many enhancements to provide an improved usability experience to users. Starting from new ways of managing multiple windows to the ability to place wires and parts using a crosshair cursor; all enhancements are created to increase ease of use.

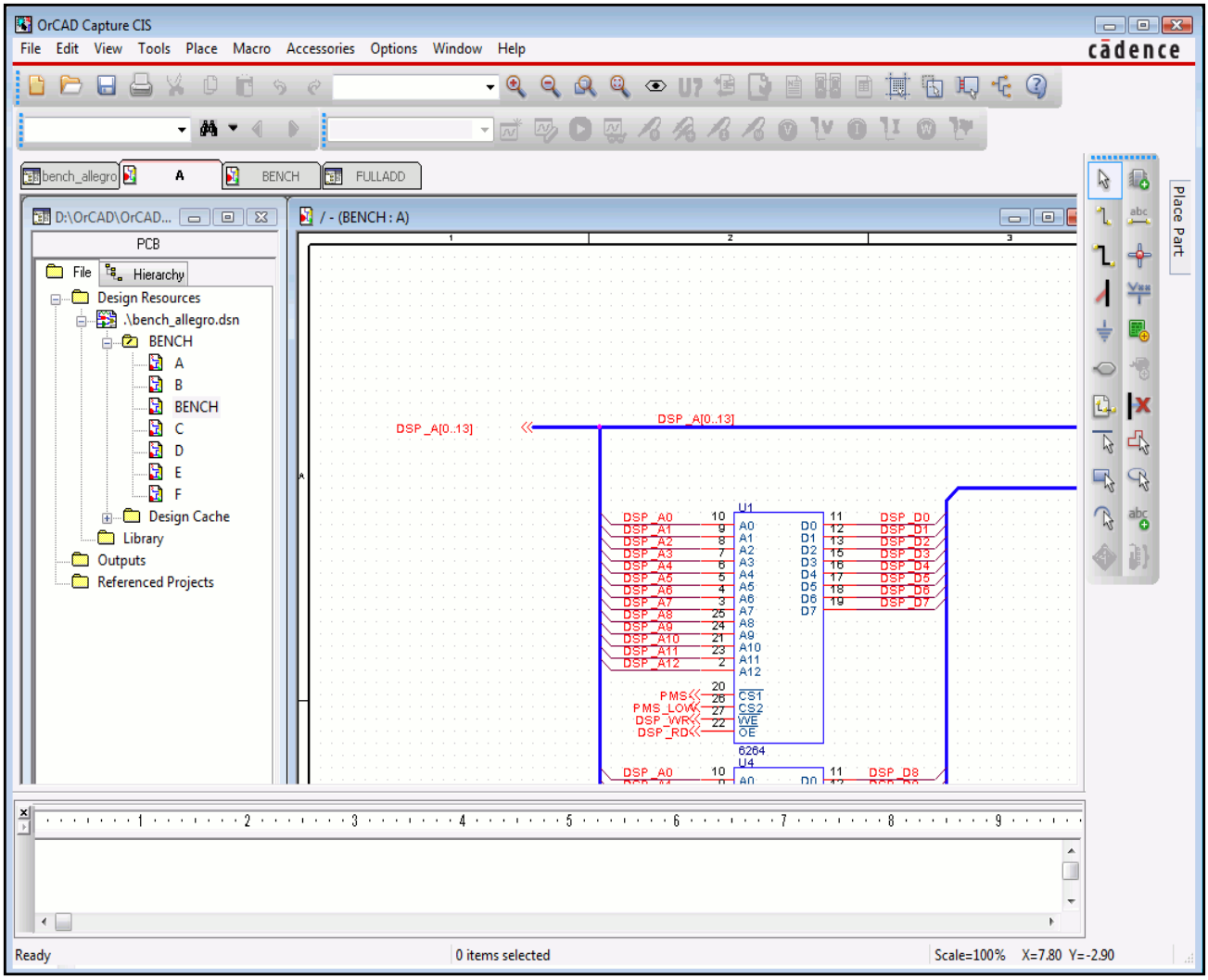
Following are some of the usability enhancements in 16.2:

- Tabbed windows with docking, floating, and MDI Child capabilities on page 9
- "New Dockable Place Part dialog" on page 11
- Incremental Package Placement on page 11
- Ability to close all open windows on page 11
- Display of net names for selected nets on the status bar on page 12
- Increased choices for lines on page 12
- Enhanced Search functionality - Find toolbar & Find window on page 12
- Non-Linear Editor (Fisheye) on page 13
- Resizable Split Part window on page 14
- Junction Dot Size on page 14

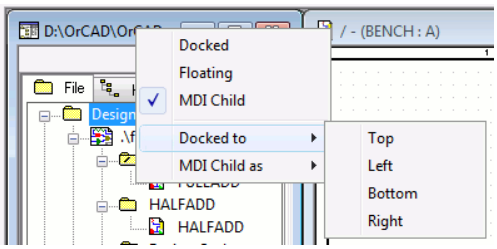
- Fullscreen Mode on page 14
- Enhanced Navigation using Zoom and Pan features on page 14
- Customizable Toolbars on page 15
- New Project Manager Shortcuts on page 16
- "Property Editor Enhancements" on page 16
- "Cross Hair mode" on page 17

Tabbed windows with docking, floating, and MDI Child capabilities

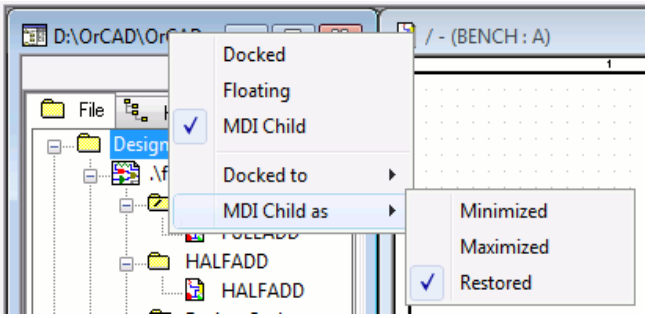
Now it is easier to manage multiple open windows through tabs that show tooltips with window names when pointed. You can click a tab to activate the associated window or press `CTRL+TAB` to navigate through different open windows from right to left. And press `CTRL+SHIFT+TAB` to navigate in the reverse order.



The Session Log and Project Manager windows give you the flexibility to dock them or keep them as floating. You can right-click the title bar of these windows to get options to dock the windows to the top, bottom, left, or right of the main window.

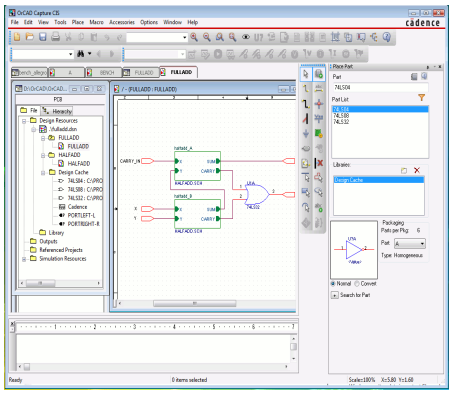


You can also specify to open these windows as MDI child windows in the maximized, minimized, or restored states.



New Dockable Place Part dialog

The modal Place Part dialog can now be made dockable. Allowing you to place the window anywhere within the Capture window and also work in a modaless manner. Giving you the flexibility to move between the different docked windows you have positioned in your Capture window.



Incremental Package Placement

When you place instances of hetrogeneous parts containing multiple packages, OrCAD Capture Place Part command now ensures that the reference designator for the part is auto-incremented. This feature was available only for homogeneous parts in previous releases of Capture.

Ability to close all open windows

You can close all open windows with a single action by choosing *Windows - Close All Windows*.

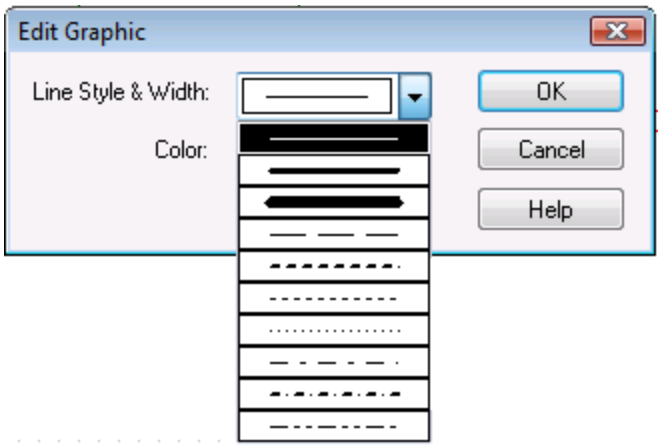
Display of net names for selected nets on the status bar

You can check the name & ID of a net by simply selecting the net or a wire in the net. The status bar displays the name & ID of the net when it is selected.

The name and ID is also displayed in a tooltip that can be viewed if you place the mouse pointer over the net.

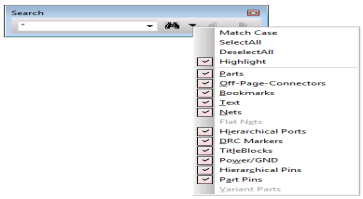
Increased choices for lines

With OrCAD 16.2, you can have additional choices for line style. Two new line styles have been added to provide thicker line choices. This also enhances printability of the designs.

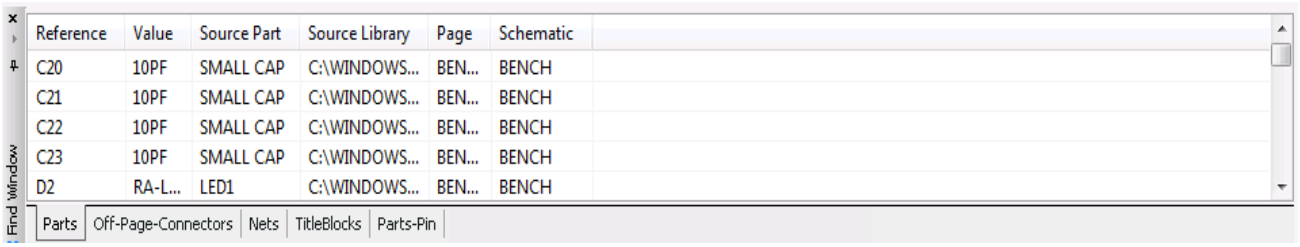


Enhanced Search functionality - Find toolbar & Find window

Search functionality is enhanced to include a new Find toolbar. This includes a new Search options button that allows you to narrow down or expand your search to the types of objects on the canvas.

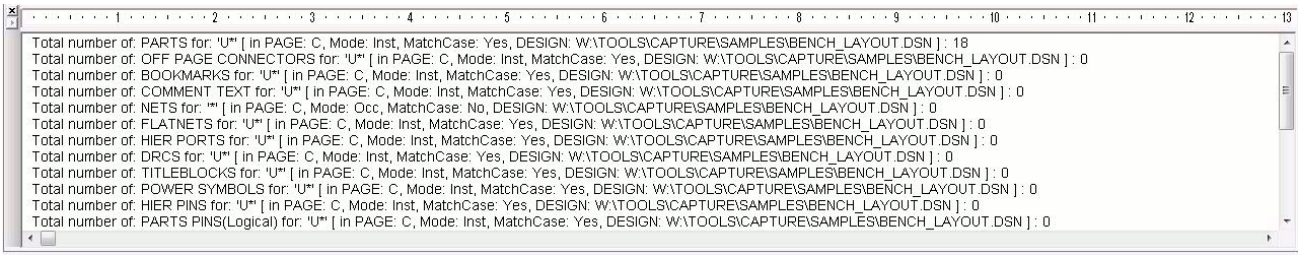


Once the search is complete, the new Find window groups the search results by object type making it easier for you to track down your result. You also have the option of saving the search results to an HTML.

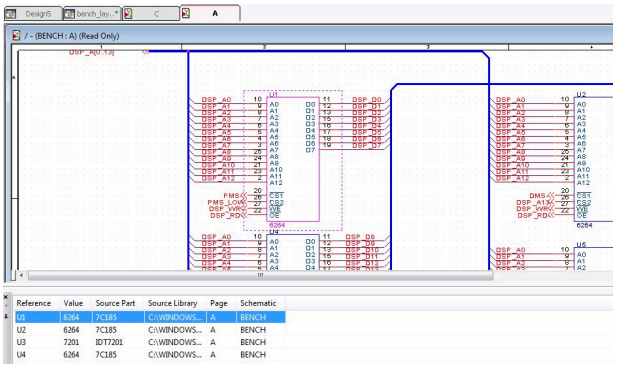


The new Find window is dockable, allowing you to conveniently position the window.

You can search at the design or page level. While the search results display in the Find window, the Session log shows details of the search like the total number of that object type found and the result page where the object was found.



You can zoom directly to the items found by double-clicking them in the Find wiindow.



Non-Linear Editor (Fisheye)

OrCAD 16.2 now includes a new Fisheye feature that provides an enhanced method to navigate and zoom into your design.

In the Fisheye view, you can focus and zoom into on one or more objects on your page. This causes all other viewable objects on the page to be demagnified allowing you to view in detail only objects of interest.

You can also set up a dynamic view that zooms into objects as you pan across the page. This bring into focus (and magnifies) any object that the mouse pointer hovers over. This dynamic zoom feature can be used with the selective zoom feature. You can even decide the zoom factor when working in this mode using the Eye Magnification feature.

Fisheye can be used completely in conjuction with all the current Capture features like place part, edit part or routing. So you can work on a schematic as before but with these features of selective and dynamic zoom.

Resizable Split Part window

The Split Part window has become easier to use. You can now resize the window to adjust the number of pins visible.

Junction Dot Size

Now you can choose the size of the junction dot that appears when two wires are connected to be Small, Medium, Large, or Very Large. You can set the junction dot size by choosing the option from the Junction Dot Size drop down list in the Miscellaneous tab of the Preferences dialog box.

Fullscreen Mode

You can change to fullscreen mode by pressing `CTRL+F8`. You can then exit the fullscreen mode by clicking the *Close Fullcreen* button or by pressing the `Escape` key.

Enhanced Navigation using Zoom and Pan features

OrCAD Capture 16.2 now includes an improved zoom functinality and a new panning feature to help you navigate and work with dense designs.

- To zoom into a specific section of you schematic you just need to hold the right mouse button down and drag it over the portion you want to zoom into. The portion will be zoomed as soon as you release the mouse button.
- When navigating a dense design and large design you would either need to zoom out of the design and zoom into a specific section or use the scroll bars to move around the parts of the design that were outside the viewable area. You can now use the panning feature to move around the design as you move the cursor without needing to use the

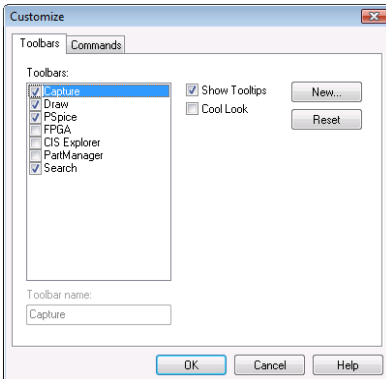
scrollbars. You need to simply click the scroll mouse button. The pan cursor & pointer appear, and the page pans as you move the mouse..

Customizable Toolbars

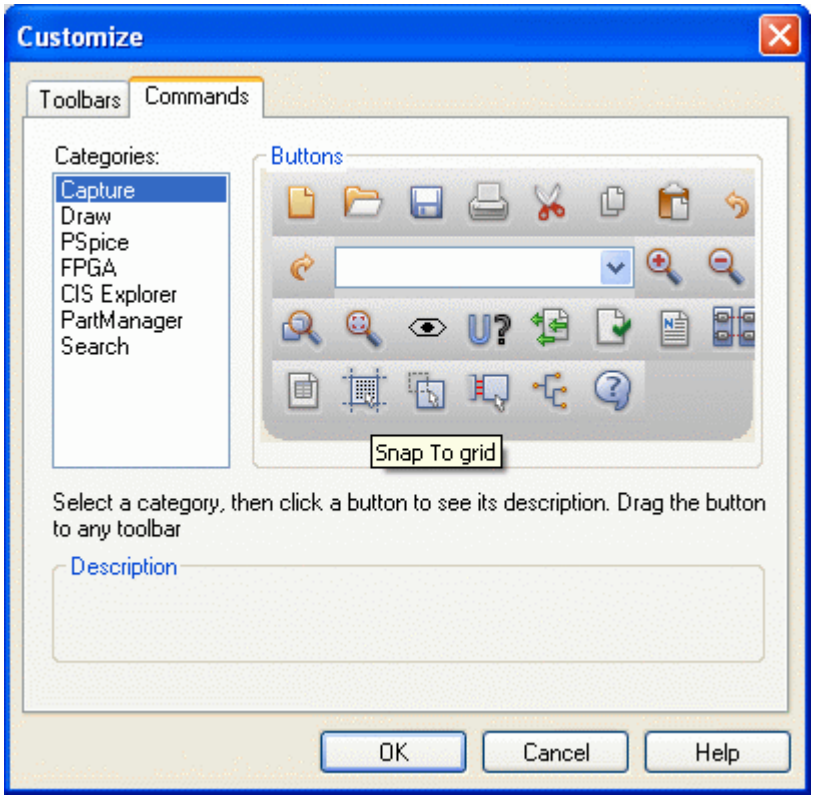
OrCAD Capture 16.2 now provides highly customizable toolbars. You can now pick and choose the toolbars you want to view or hide. And the state of the toolbars is maintained when you close and open Capture.

The new Customize dialogs includes two tabs Toolbars and Commands.

- The Toolbars tab allows you to add and remove toolbars. It also allows you to create new toolbars. You can decide whether or not you want to view tooltips.



- Use the Commands tab to add or remove buttons from the toolbars. Also, clicking on each button in the tab dispalys a short description of the button.



New Project Manager Shortcuts

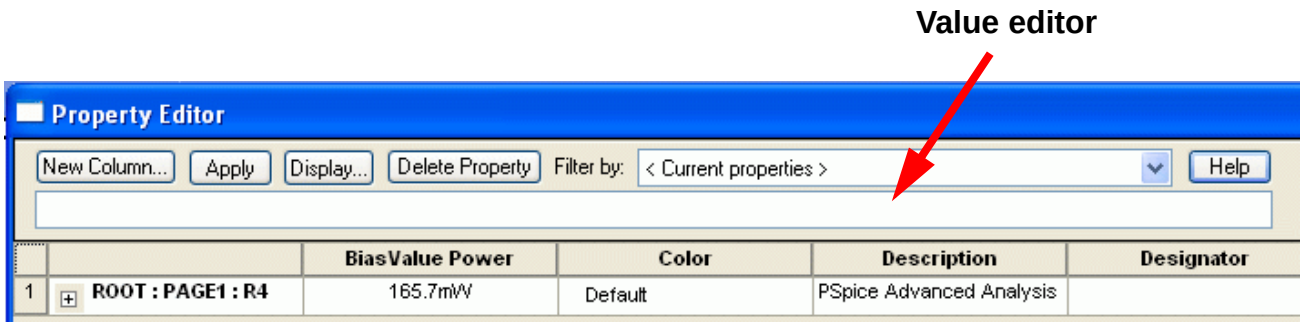
The right mouse button shortcut menu in the Project Manger includes some new useful options.

- **Annotate**: You can now choose to annotate a design or selected parts of a design by selecting the Annotate menu item from context menu in the Project Manager. You will see this option either at the design or page level.
- **Cut / Copy & Paste**: The Project Manager context menu also includes the new Cut / Copy & Paste options. You can cut or copy a page from one design folder and paste into another folder. Note, while you can perform the copy operation at any time, you can do a cut operation only if that particullar object is not current open, You can even cut or copy a design folder from one design and paste it into another deslgn.

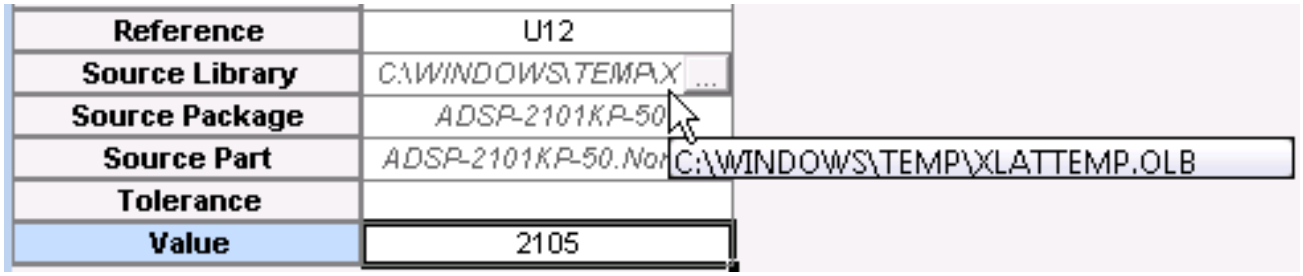
Property Editor Enhancements

In OrCAD 16.2, the OrCAD Capture Property Editor is enhanced to:

- Include value editor that allows you to edit property values without having to resize the spreadsheet columns.



- Immediately refresh property editor when a property is deleted.
- Include a tooltip for cell values. So, if you do not want to increase the column width, you can point to a cell whose value is large than the column width.



- Retain the order of properties columns or rows. So if you rearrange the propery columns or rows, the order is maintained within your current session.

Cross Hair mode

When placing a part on a very dense design, it is often not easy to find your way around the design. To make this task more manageable, you can turning on the Cross Hair mode. This will place a Cross Hair at the edge of the mouse pointer. As you move your cursor across the page the cross hair will make it easier to locate objects like pin and nets or very small parts in your design.

Use the F6 key to toggle this mode on and off.

Elliptical Arcs

You can now draw arcs that are part of an ellipse. This means the arcs do not need to be circular, they can be drawn as part of an ellipse.

Enhanced OrCAD Capture and PCB Editor Integration

OrCAD Capture 16.2 comes with better integration with PCB Editor. The following cross probing and cross placement features enhances flow between Capture and PCB Editor:

- Now you can place one or all component in a page by just selecting the component in Capture, provided PCB Editor is in the Place Manual mode
- When design and board are out of sync and when you try and highlight a part/pin/signal in PCB Editor that has been deleted in Capture design then for such components an appropriate warning message is printed into the session log.
- While doing cross-probing from Capture, you no longer need to do Allegro Select. All you need to do is to turn on the highlight mode in PCB editor and select the component in Capture and it will get highlighted in PCB Editor.

Improved FPGA Functionality

In 16.2, OrCAD Capture has improved support for FPGA flow with the following enhancements and new features:

- Support for split part: With an ever-increasing pin count and complexity for FPGA parts, the easy to use GUI based options of Capture that can be used to create single section and multi-section FPGA parts based on I/O bank will simplify the task of users.
- Power Pin visibility options: Users can now make power and ground pins invisible by checking a single option.
- More Pin defaults and pin shapes: Users can configure pin-shapes and pin-directions in FPGA Setup before doing Generate Part.
- Specifying pin groups: Users can specify pin groups based on I/O Banks or I/O standard.
- Modifying Pin defaults: Users can modify the direction and shape of pins in FPGA parts from GUI options.
- Exporting FPGA: Users can export FPGA components by using the Export FPGA dialog box. The export FPGA completes the bi-directional link between FPGA Designers and PCB Designers to pass the constraints information not available in previous releases.
- Reserve Pins: Users can now reserve Input, Ouput and Bidirectional pins in an FPGA component using the Reserve Pins dialog box from within the FPGA Export dialog box.

OrCAD Capture now comes with a new *FPGA Options* dialog box that enables users to specify FPGA settings while creating a FPGA part. This dialog box can be opened from the Generate Part dialog box.

Capture includes a FPGA toolbar for quick access to some of the important FPGA commands.

New Annotation Type Option

The annotation dialog box now includes a new Annotation type list. When annotation your design you can now choose from three sequence options:

- **Default**: This options annotates you design in the same sequence and manner as previous versions of OrCAD Capture.
- **Left - Right**: Use this option if you want the objects in your design to be annotated in the left to right order in which they are placed on the page grid.
- **Top - Bottom**: You can annotate the objects in your design from top to bottom order on the page grid using this option.

For a detailed description of this feature see Annotation Sequence in the Capture User Guide.

DRC Enhancements

The Design Rule's Check in Capture is enhanced to improve permformance on very large design and to include some new design checks.

- In OrCAD 16.2, DRC will now check for unconnected Global nets across schematics in a design.
- The "**Report misleading tap connections**" check is enhanced to report missing bus taps as well.
- When working with very large FPGAs, designer may accidentally route a signal of the same name from two different pins using two separate module ports/pins of the same name. The "**Check hierarchical port connections**" option is enhanced to include a check that identifies two identical module ports/pins within a schematic.

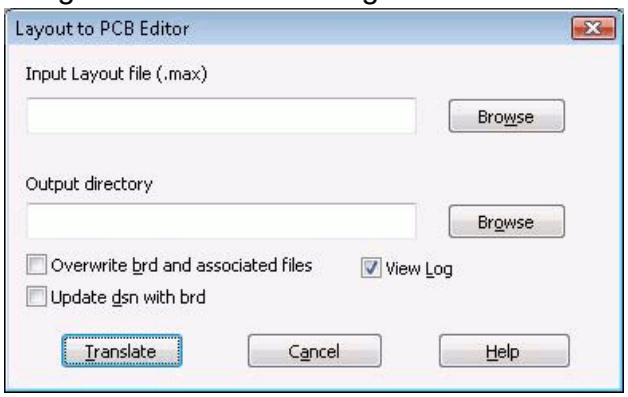
Netlist Enhancements

- OrCAD Capture 16.2 includes a new **PACK_SHORT** property used to short pins on a part. The PACK_SHORT property specifies the shorting of pins of a part. Multiple groups of pins, each group having two or more pins, can be shorted.

- The correct net names are updated in the netlist for invisible power pins if there is a global net short and POWER_GROUP is not specified. As a result, users need not manually update invisible pins.
- You can now specify the location where the netlister will search for the Allegro.cfg file by creating an environment variable **CDS_SITE** to point to the path of the .cfg file. So you can now create a common custom cfg file for all users.

L2A Integration in Capture

The Layout to PCB Editor Translator converts PCB designs created in OrCAD® Layout to Allegro® PCB Editor designs.



- You can translate PCB design databases created in any version of Layout and prepare them for use within PCB Editor.
- The Layout to PCB Editor Translator converts designs (.MAX files) created in Layout to design databases (.BRD files) that can be read by PCB Editor.
- You can also specify the option Overwrite existing files if you want to overwrite the existing files such as the design fie.
- The Layout to PCB Editor now also allows you to choose to synchronize the the Capture design and PCB Editor board files.
- During the translation process, the footprint names are changed. If you select the Synchronize dsn with brd option the footprint names are synchronized with the Capture design.

User Interface Updates

The enhancements made in OrCAD 16.2 within the display canvas of OrCAD Capture include:

- New Icons on page 21
- Tabbed windows with docking, floating, and MDI Child capabilities on page 9
- Branding Changes on page 22

Pink Gradation & Images in Menus

A pink coloring gradation appears when you move the mouse pointer over a menu item, bringing the menu item into focus and easier to differentiate from other items in the menu.

Besides this, if any menu item has a corresponding toolbar button, the toolbar button icon will appear alongside the item text. This makes it easier to correlate the item with the menu button. Further making it easier to use menu buttons when you are familiar with them after using the menu items.

New Icons

In OrCAD 16.2, OrCAD Capture and OrCAD Capture CIS have been upgraded with new, softer looking icons. This upgrade brings uniformity across many of the generic icon styles in different Cadence products. Several new icons have also been added across many of the functional groups.

This upgrade brings uniformity across many generic icon styles. Several new icons have also been added across many functional groups.

Note: For a quick introduction to the new-look icons in OrCAD Capture 16.2, view the following multimedia demonstration:

New-Look Icons in OrCAD Capture 16.2

There are seven toolbars in OrCAD Capture and OrCAD Capture CIS. For a detailed description of the Capture toolbars click: Toolbars in OrCAD Capture 16.2

A description of the new CIS toolbar is available at: Toolbars in OrCAD Capture CIS 16.2

Toolbar Customization

A total change in the Capture toolbars includes a standard Windows application style customization of toolbars. This allows you to select the toolbars you want to see.

Further it also allows you to choose the icons that appear in each toolbar

You can even create your own completely customized toolbar, give it a name of your choise and put whichever toolbar icons you want.

Branding Changes

The corporate logo of Cadence now appears in the upper right corner of the main application window of OrCAD Capture and OrCAD Capture CIS. The corporate logo and a red line under the top-level menus are common across all products.

Fixed CCRs

The following lists the problems reported and fixed in Capture16.2. For detailed information about a fixed problem, contact your customer support.

CCR ID	Description
11554 (PCR 322742)	Elliptical arcs - and method change
13669 (PCR 337376)	No warning when crossprobing deleted part in Capture
15426 (PCR 352911)	Customer suggests improvements in Property Editor
25297 (PCR 421669)	Doing a SAVE AS should point to CURRENT directory
25842 (PCR 425237)	Enhance Capture, Allow use of heavy dashed lines
26953 (PCR 431677)	Request for - close all windows, or pages option
30842 (PCR 453347)	Select multiple component with a single function for place in Alg
54304 (PCR 556980)	Unconnected net DRC error if GND/PWR instantiated on Diff sch
58025 (PCR 563054)	drc 0004 error not shown for pins conflicts on a design
82682 (PCR 605060)	Lack of consistency with DRC report.
105258 (PCR 652814)	Junction dots management issue
116119 (PCR 665275)	Add pack_short property under capture
130755 (PCR 688677)	Improve crossprobe and selection between Capture and Allegro
141959 (PCR 701679)	Edit >Find to have an option for searching Pin Names
148804 (PCR 709224)	Property Editor Spreadsheet will not update until closed
157713 (PCR 719345)	Random Junction Points added in Version 15.1 & 10.0 SP1.1
178827 (PCR 743859)	Save As directory different than Open directory

CCR ID	Description
191253 (PCR 757550)	Printing E and F pin names overlaps pin making unreadable
194902 (PCR 761534)	Generate part should include pin types and styles functions
200160 (PCR 767162)	Option to change size of Connection Dot
201550 (PCR 768594)	filled rectangle overrides line and text visibility
227082 (PCR 794463)	Old path use in save or save as operations
229057 (PCR 796446)	Increase in size of Connection Dots
233231 (PCR 800634)	Capture Find filter should have pins in scope section
234578 (PCR 801991)	Capture Allegro Select not required while placing the part
243112 (PCR 810602)	Property editor does not retain the user settings
295372 (PCR 870462)	Hetrogenous device enhancement
298766 (PCR 873945)	Maximise button for Browse Spreadsheet
298870 (PCR 874052)	Printing cross hatch area loses wires
331188 (PCR 899142)	Need new feature Find Pin or Find Pinname
335395 (PCR 902989)	LT1369/SO in the OPAMP.OLB library is incorrect
342217 (PCR 909537)	Improve crossprobe and selection between Capture and Allegro
352261 (PCR 918475)	Custom pin proporties are not modifiable
355852 (PCR 400183)	ability to re-size captures annotation control field
366847 (PCR 2366847)	Annotation not keeping correct order
373773 (PCR 2373773)	Unnecessary junctions are formed on many operations
381638 (PCR 2381638)	Allow for multiple parts to be selected for Allegro placement
384316 (PCR 2384316)	Capture Find filter should have pins in scope section
387660 (PCR 2387660)	Add shortcuts to tool palette
390674 (PCR 2390674)	Export part properties

CCR ID	Description
390923 (PCR 2390923)	error message is meaningless 53 DDB_ERROR: Null object id specified in call to ddbStopGen
395189 (PCR 2395189)	Hetrogenous device enhancement place U?A then U?B and so on
401133 (PCR 2401133)	drc 0004 error not shown for pins conflicts on a design
406572 (PCR 2406572)	Annotaion problem : Ref Des are incorrectly assigned.
412113 (PCR 2412113)	Enhacnement: Ability to enlarge the annotation window
419009 (PCR 2419009)	Printing cross hatch area loses wires
432731 (PCR 2432731)	Enhancement: Elliptical Arc drawing tool in Symbol Editor
439004 (PCR 2439004)	Pin number 0 for pspice parts overrules pspice_only property
444745 (PCR 2444745)	Design must be saved before the root can be changed
445237 (PCR 2445237)	ERROR [NET0011] Netlist failed or may be unusable while creating a PSpice net list
453628 (PCR 2453628)	Enhancement: Need user selectable junction sizes
454795 (PCR 2454795)	Allow usage of pin number 0 in Capture Allegro
456889(PCR 4026007)	Unable to import pin type property from edited file
468563(PCR 2468563)	some pins are missing while generate a part using Quartus II Version 5.1 pin file.
468586(PCR 2468586)	Enhancement for renaming of duplicate pinnames while generating a part through pinfile.
470808 (PCR 2470808)	Map 4 capture pins to 1 allegro Pin
480171 (PCR 2480171)	VDC Part gives ALG0032 Error
480795 (PCR 2480795)	Error ALG0050 even if common named pins are connected to single net.
481201 (PCR 2481201)	DRC Enhancements

CCR ID	Description
482028 (PCR 2482028)	pack_short property not working properly in capture
483983 (PCR 2483983)	Capture is checking DRC for option "Report off-grid objects" with respect to the initial grid setting
487232 (PCR 2487232)	Find Pin of selected part
489048 (PCR 2489048)	Enhancement: Maximize icon in Browse Spreadsheet window
490242 (PCR 2490242)	Error in Documentation under the section "Creating a Verilog model from a hierarchical block"
490315 (PCR 2490315)	Tabs on schematic page for changing the page
492458 (PCR 2492458)	Resizing of split part window in capture
494194 (PCR 2494194)	Capture to Allegro netlisting erorr
494228 (PCR 2494228)	Capture.ini file gets Reset with Part Selector and Symbol Selector Configured Libraries sections lost
496910 (PCR 2496910)	Inconsistent netlist creation
498276 (PCR 2498276)	Enable position lock on Capture windows
500683 (PCR 2500683)	Option to change connection dot size
501730 (PCR 2501730)	list Netname in status bar when in wire mode
501822 (PCR 2501822)	Doc Error Capture user guide page 507
504664 (PCR 2504664)	File format useful for Alteras Quartus FPGA design tool
504969 (PCR 2504969)	Maximise button for Browse Spreadsheet
511102 (PCR 2511102)	Section of the ini file is getting reset on cancel to the product selection dialog
511322 (PCR 2511322)	net name coming wrong for Power pin in PCB
516159 (PCR 2516159)	Default location for Allegro.CFG
516899 (PCR 2516899)	PCB Editor FlowTutorial doc
517465 (PCR 2517465)	printing E and F pin names overlaps pin making unreadable
519927 (PCR 2519927)	DRC does not consider global connected power pins
520440 (PCR 2520440)	Resizing the column widths in Property editor

CCR ID	Description
521588 (PCR 2521588)	DRC does not consider global connected power pins
523216 (PCR 2523216)	Annotation not keeping correct order
524028 (PCR 2524028)	Adding net properties for flat design results change in annotation mode
524552 (PCR 2524552)	Capture crashes while cleaning up the cache
525349 (PCR 2525349)	Enhancement: Warning message if design name is miss-matching while Allegro netlist
530140 (PCR 2530140)	RPD : Delta Value should be positive numeric value
530610 (PCR 2530610)	Enhancement: Capture should allow making differential pairs for bus >> bits using AutoSetup.
533685 (PCR 2533685)	EMI : SPCODD-413 error generating a netlist
534456 (PCR 4044329)	Change small upper-case (caps) letters in pin name to caps for NC pins in Capture schematic while netrev
535331 (PCR 2535331)	Enhancement for placing a heterogeneous part
535523 (PCR 2535523)	Restore previous Help content
538193 (PCR 2538193)	EMI: invalid format/unable to change drive errors
538726 (PCR 2538726)	Auto rename duplicate pins during FPGA import
539664 (PCR 2539664)	Generate part using Lattice files
541560 (PCR 2541560)	Generate part should be able to process BGA text out and die text out formats from our APD SIP software
544401 (PCR 2544401)	Question regarding Differential pair and BOM variant
544896 (PCR 2544896)	VHDL Netlist Bus Name Issue
545321 (PCR 2545321)	part configuration library information missing from INI file while disconnecting from license
545362 (PCR 2545362)	DRC tool does not recognize two identical Module port in same page
547445 (PCR 2547445)	Export, modify and import properties on library parts not up
548625 (PCR 2548625)	Some flaws in design because of diffpair

CCR ID	Description
549068 (PCR 2549068)	Document for Macro Scripts
549075 (PCR 2549075)	enhancement for having a feature to calculate the total pins in design
550580 (PCR 2550580)	Allow usage of pin number 0 in Capture Allegro
551455 (PCR 2551455)	latency in spawning PCB Editor from Capture on mouse event
553210 (PCR 2553210)	DRC enhancement for multiple module port
555134 (PCR 2555134)	cross probing of pins is not working fine
556831 (PCR 2556831)	Wire invisible if covered by a slid filled shape
556867 (PCR 2556867)	Some parts are causing problem while Import Properties operation.
558642 (PCR 2558642)	Need pack short property in Design entry CIS
560919 (PCR 2560919)	MultiPin highlight is not working properly from Capture to Allegro
564460 (PCR 2564460)	Column width changes to default in Property Editor
564485 (PCR 2564485)	ANN0011 error message should point to the location of error
568360 (PCR 2568360)	Option to Export Pin List with details of a Component in Spreadsheet format
569639 (PCR 2569639)	Enhancement: DRC that should catch any missing bus bit in the design
569691 (PCR 2569691)	All the Package Part are replaced by the selected Part while linking multi package part to database
571384 (PCR 2571384)	Adding net properties for flat design results change in annotation mode
572671 (PCR 2572671)	DRC does not consider global connected power pins
573515 (PCR 2573515)	WARNING DRC0006 Net has fewer than two connections is false warning if on a global net in hierarchy
574259 (PCR 4055549)	Edif 200 issue about Capture(SPB 15.7)

CCR ID	Description
575196 (PCR 2575196)	Part configuration library information missing from INI file
575615 (PCR 2575615)	Why are suffixes added to the NAME Property?
579157 (PCR 2579157)	Use as default option in Cadence Product Choices not working
579601 (PCR 2579601)	DRC Enhancements
580382 (PCR 2580382)	Cannot change the value of user added property-Cap0007
580545 (PCR 2580545)	EMI: Cannot find primitive part for primitive instance
584118 (PCR 2584118)	capture crashing while drawing a circle using arc command in schematic editor
584148 (PCR 2584148)	Export property does not catch carriage return present in property value
585922 (PCR 2585922)	DRC for mismatch in bus width
587692 (PCR 2587692)	Enhancement: Warning message for illegal characters while generating PCB Editor netlist
591015 (PCR 2591015)	Design will not netlist
592248 (PCR 2592248)	Message for ALG0036 Error refers to a wrong Part as Problematic
592343 (PCR 2592343)	Moving text or property is causing duplicate reference designator
594239 (PCR 2594239)	Location of PSpice model libraries is wrong in Capture User Guide
598750 (PCR 4062919)	Auto rename duplicate pins during FPGA import
607559 (PCR 2607559)	Capture crashes while adding and deleting a Library to the Design from Project Manager
608220 (PCR 2608220)	Capture crashes after Generate Part
614659 (PCR 2614659)	CIS replacing heterogeneous parts

2

What’s New in OrCAD Capture CIS 16.2

This chapter contains the following sections describing the OrCAD Capture CIS 16.2 (henceforth referred as Capture CIS) release.

- New Features and Enhancements on page 32
- Fixed CCRs on page 36

New Features and Enhancements

Capture CIS 16.2 brings you the following new features and enhancements:

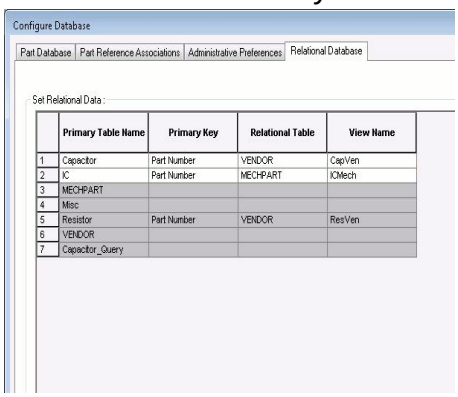
- CIS RDBMS Support on page 32
- CIS Configuration File in XML Format on page 34
- supplyframe Portal in ICA on page 34

CIS RDBMS Support

With 16.2, CIS allows you to create and use relational tables in your parts database. These tables must have a one-to-many relationship with your part information (primary) tables. The database may contain a Vendor table with multiple vendor / manufacture part numbers for one company part number in your electrical (e.g Resistor) table. This structure allows you to query for data across the primary and relational tables.

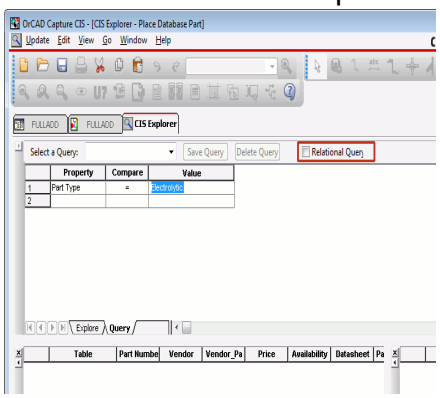
The CIS Configuration dialog

- The CIS Configuration dialog now includes a new Relational Database tab in which you define the Primary and Relational tables and a user-defined View Name.

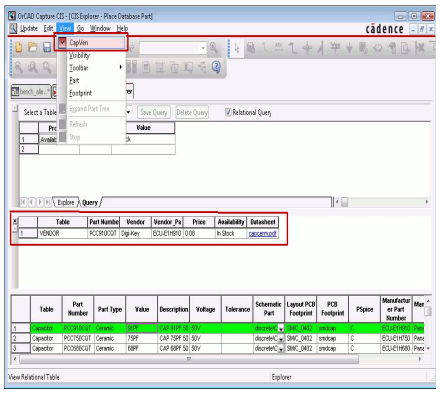


CIS Explorer

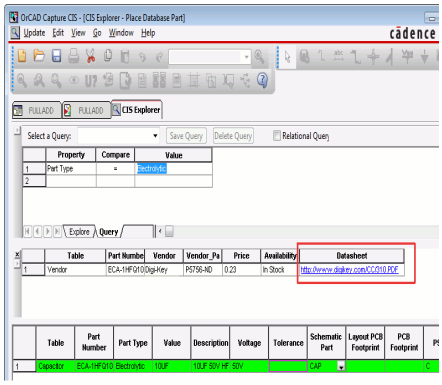
- The Search Query tab includes a **Relational Query checkbox** that you use to create and run relational queries on the basis of relations you set up in the CIS configuration.



- The CIS Explorer window now includes the new **Relational view**. This displays the related table data for the selected part in the primary table. For example, the relational view displays the vendor data for the selected electrical (Capacitor) item in the CapVen view.



- The Relational view has a Datasheet field that contains a hyperlink to the datasheet. You can now view the datasheet simply by clicking on this link.



CIS Configuration File in XML Format

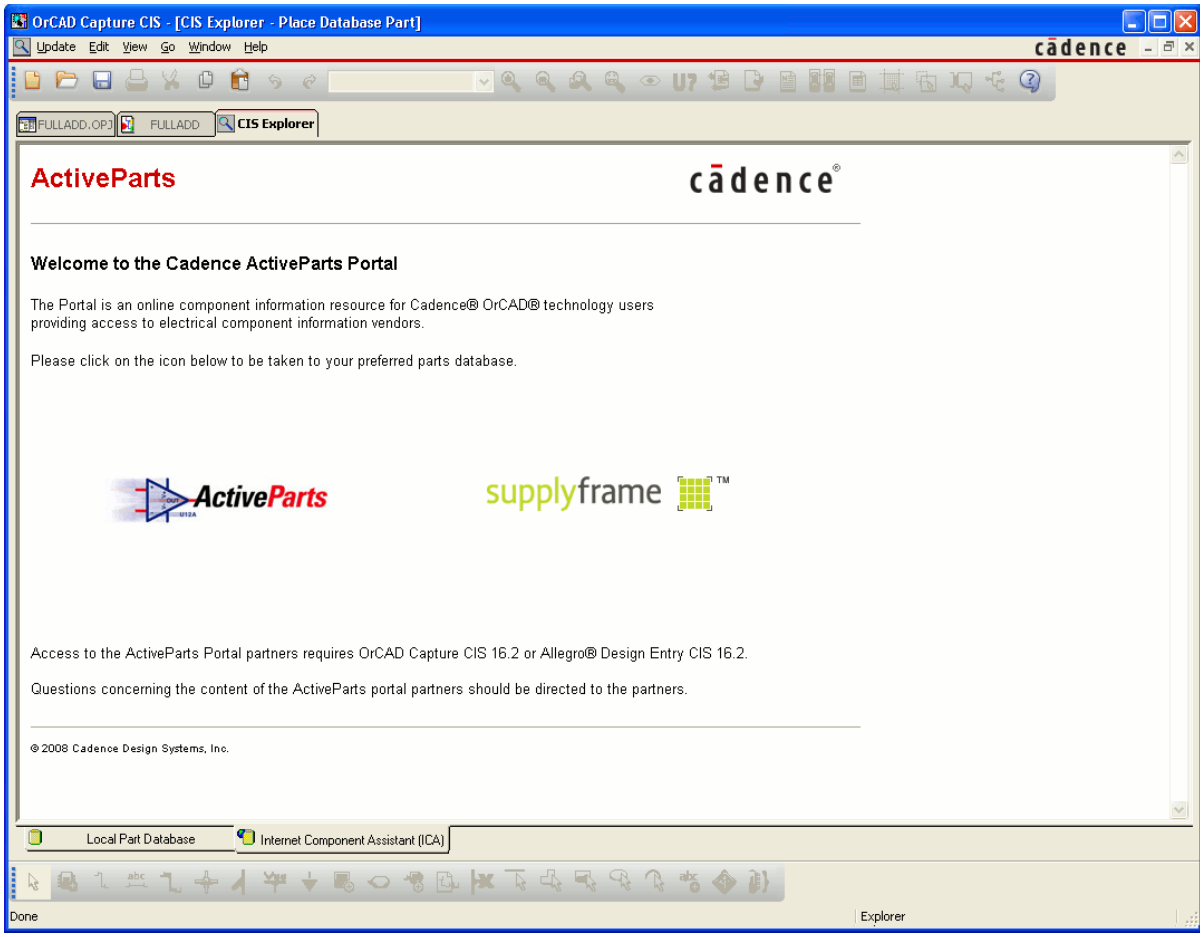
The16.2 CIS configuration file is in XML format. Giving you the flexibility to read and edit it in any text or XML editor.

If you use a CIS version 16.0 or earlier version configuration file with CIS 16.2, the file will be updated to the CIS 16.2 XML format.

When CIS 16.2 updates the configuration file to the new format, it creates a backup of the old configuration file with the extension .DBCBAK. You can use this file with CIS 16.0 or earlier versions.

supplyframe Portal in ICA

ICA now includes two Internet Component portals, ActiveParts & supplyframe. In addition, to ActiveParts, supplyframe provides you with more components available via its portal. You can now access both ActiveParts and supplyframe from the ICA home page in CIS.



Like ActiveParts, supplyframe allows you to search and place components on your schematic and add these parts (as temporary parts) to your preferred parts database.

Fixed CCRs

The following lists the problems reported and fixed in Capture CIS 16.2. For detailed information about a fixed problem, contact your customer support.

CCR ID	Description
452551 (PCR 2452551)	Expand Visibility Window button does not work, resizing view collapses that particular view
466488 (PCR 2466488)	up/down arrow keys and pgup/down not working in part manager window
474432 (PCR 2474432)	wrong variant.lst is generated from CIS Part Manager
475947 (PCR 2475947)	Keyboard does not work in part manager
494689 (PCR 2494689)	Footprints does not show up when PCB Footprint Property is not mapped in
498273 (PCR 2498273)	a strange beep comes while sorting in CIS explorer winodw
501631 (PCR 2501631)	Errors in the CIS User Guide
536558 (PCR 2536558)	Variants lost while replacing Titleblock
556865 (PCR 2556865)	Capture give System-Beep while sorting in CIS
560903 (PCR 2560903)	Symbol body still viewable when not fitted in variant view
560925 (PCR 2560925)	Symbol body does not change color in Variant mode
561504 (PCR 2561504)	varaint parts are being erased when populated from an external
561863 (PCR 2561863)	Error in VARIANT REPORT feature when comparing multiple BOMs
563296 (PCR 2563296)	a strange beep comes while sorting in CIS explorer winodw
565798 (PCR 2565798)	all the sections of mult part package are not coming as DNS in Variant
568737 (PCR 2568737)	All variant parts are not listed in variant report
578658 (PCR 2578658)	Export Variant List path should be relative to respective project

CCR ID	Description
583252 (PCR 2583252)	Some NM parts have grey bodies and others not
583781 (PCR 2583781)	Symbol body does not change color in Variant mode
592625 (PCR 2592625)	File Variant.lst is duplicated in the output folder
600459 (PCR 2600459)	CIS >> Part Pane window goes off after double-clicking at its window bar Variants lost while replacing Titleblock

3

What’s New in PSpice 16.2

This chapter describes the new features in the PSpice 16.2 release.

- New Features on page 40
- Fixed CCRs on page 53

New Features

PSpice 16.2 brings you the following new features and enhancements:

- New MOSFET Device Model BSIM4 Support in PSpice
- User Interface Updates
- New Supported Devices in Smoke Analysis
- Enhanced Performance for Large DAT files
- New Models
- CheckPoint Restart Support for Digital and Mixed Circuits
- Support for Split Part as a Single Component
- Displaying PSpice Names

New MOSFET Device Model BSIM4 Support in PSpice

The 16.2 release provides users with BSIM4 as a new MOSFET model as level=8, increasing the supported MOSFET device models to eight. BSIM4 offers several imrovements over BSIm3, not just in the traditional I-V modeling of the intrinsic transsitor, but also in the incorporation of extrinsic parasitics. BSIM4 provides robust and predictive simulations with increased accuracies in modeling various functions, such as tunneling and thermal noise. With BSIM4 support, PSpice now integrates the following models:

- IV model
- GIDL (gateinduced drain leakage) current model
- Bias-dependent source/drain resistance (Rds(V)) model
- Asymmetric source/drain junction diode model

Because of the support for the new model, many new parameters are included in PSpice that can be used to simulate the BSIM4 models. To know more about the parameters and equations refer to the `PSpice Reference Guide`.

User Interface Updates

The enhancements made in OrCAD 16.2 within the display canvas of OrCAD Capture include:

- New Icons
- Branding Changes
- Line Numbers in PSpice Text Editor
- Progress Indicator for Large Simulation Data File
- Convinient and Easy Method to Zoom In and Zoom Out in Probe Window
- Mouse Wheel Support for Scrolling in Probe Window

New Icons

In16.2, PSpice A/D has been upgraded with new, softer looking icons. This upgrade brings uniformity across many of the generic icon styles in different Cadence products.

There are six main toolbars in PSpice. Click a toolbar name in the following list to view the new-look icons on the toolbar:

- Cursor
- Edit
- File
- Probe
- Simulate
- View

Cursor

Icon	Name

	Cursor Peak
	Cursor Trough
	Cursor Slope
	Cursor Min
	Cursor Max
	Cursor Point
	Cursor Search
	Cursor Next Tran
	Cursor Prev Tran
	Mark Label

Edit

Icon	Name

	Cut
	copy
	Paste
	Undo
	Redo
	Toggle Bookmark
	Next Bookmark
	Previous Bookmark
	Clear Bookmarks

File

Icon	Name
	New

	Open
	Append File
	Save
	Print

Probe

Icon	Name
	Zoom In
	Zoom Out
	Zoom Area
	Zoom Fit
	Load Next Part
	Toggle Large Data File Mode

	Log Y Axis
	Fourier
	Performance Analysis
	Log X Axis
	Add Trace
	Evaluate Measurement
	Text label
	Mark Data Points
	Toggle Cursor
	Toggle Measurement Results Window

Simulate

Icon	Name

	Run
	Save Simulation State
	Pause
	Stop

View

Icon	Name
	Always on Top
	View Circuit File
	View Simulation Output File
	View Simulation Results
	Simulation Queue
	Edit Simulation Settings

Alternate Display

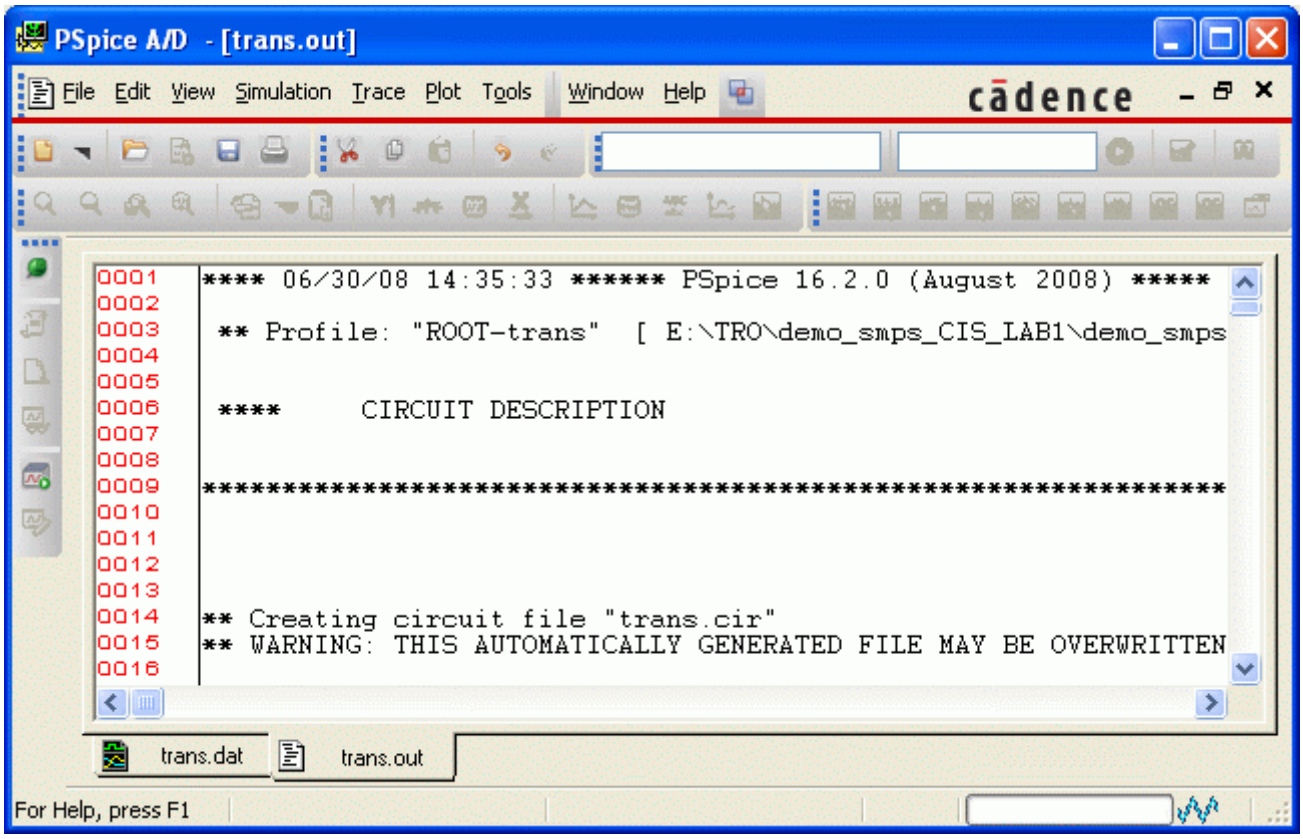
Edit Runtime Settings

Branding Changes

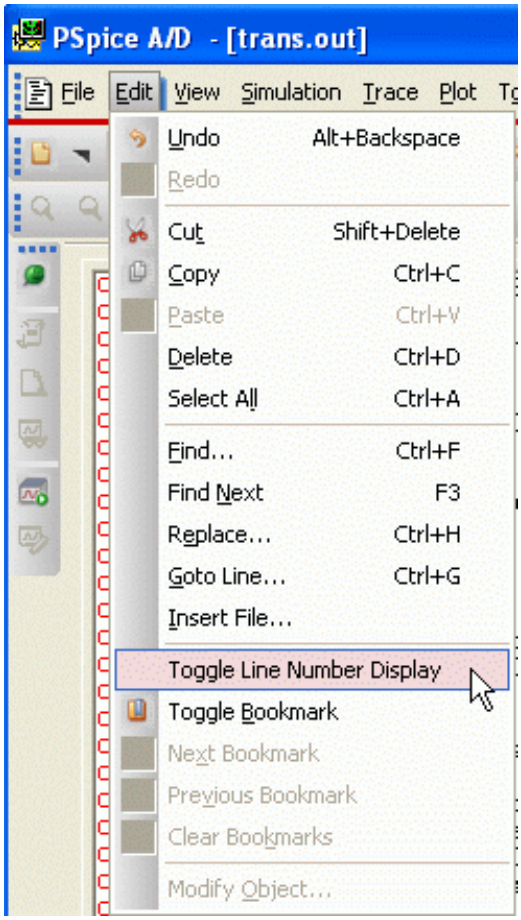
The corporate logo of Cadence now appears in the upper right corner of the main application window of PSpice. The corporate logo and a red line under the top-level menus are common across all products.

Line Numbers in PSpice Text Editor

The text editor of PSpice now shows line numbers making it easier to edit large files.



You can switch off or on the display of line numbers by choosing *Edit – Toggle Line Number Display*.



Progress Indicator for Large Simulation Data File

When you load large simulation data files, PSpice displays the progress on the left-bottom corner of the PSpice window status bar. This informs about the progress enabling users to estimate the time required to load the entire file.

Convinient and Easy Method to Zoom In and Zoom Out in Probe Window

You can zoom in or zoom out in the Probe window of PSpice pressing the following keys:

- Press either `i` or `I` to to zoom in
- Press either o or 0 to to zoom out

Mouse Wheel Support for Scrolling in Probe Window

You can now use the mouse wheel, in addition to the scroll bars, in the Probe window to view the wave forms displayed after running a simulation.

New Supported Devices in Smoke Analysis

Smoke Analysis has been enhanced in 16.2 by supporting following new devices:

- Inductor for DC Current
- VSWITCH
- Transformer (Single and Double Winding)
- Electrolytic Capacitor

In addition, now you can add smoke parameters to the following new devices in Model Editor:

- LED
- Zener Diode
- Varistor
- Diode Bridge
- GaAs MESFET
- Thyristor
- Voltage-Controlled Switch
- 4 Pin Optocoupler
- NPN-PNP
- NMOS-PMOS
- Dual BJT
- Dual MOS
- Transformer

Enhanced Performance for Large DAT files

PSpice takes much lesser time to load large DAT files that are more than 2 GB in size. In addition, the percentage progress of loading is displayed on the status bar, making it easier for users to approximate the time taken. This enhancement makes the probe window much faster in its performance.

New Models

The following new vendor models have been added to 16.2:

- 8-bit Shift Register CD4094BC
- ABM for Digital Primitive
- ARINC-429 Drivers
- Dual High Side MOSFET Driver
- Gate Turn Off Thyristor (GTO)
- LOGIC Gate OptoCouplers
- Low Dropout Adjustable Regulator LM2941
- Microsemi Bidirectional suppressor
- On-Semi Microprocessor supervisor circuit
- Planar Core Models
- Precision Isolation Amplifier
- Precision Voltage Reference
- SAC Models
- Surface Mount Zener Voltage Regulator

New Vendor Models

- EPCOS inductors and coils
- NXP MOSFET models
- STMicroelectronics OpAmp models
- Vishay MOSFET models

CheckPoint Restart Support for Digital and Mixed Circuits

The CheckPoint Restart feature of PSpice can be used to generate CheckPoints at specified timepoints of a simulation and then restart the simulation from a specific CheckPoint. In 16.2, this feature is also available for digital and mixed circuits, in addition to analog circuits. This enables users to restart and run simulations from only a range of interest instead of running the simulation again from start for any changes.

Support for Split Part as a Single Component

In 16.2, Design Entry HDL - AMS Simulator flow is enhanced to simulate split parts as single components. For example, if you split a part into three sections and simulate the design, AMS Simulator will identify the different sections of the split part and simulate them as a single component by intelligently combining the sections into one single part.

AMS Simulator uses the two properties `SPLIT_INST` and `LOCATION` to identify split part sections and combine them. Alternatively, the `SPLIT_INST_NAME` can be used to identify sections of a split part. The sections of a split part can be spread across different pages of a design.

However, it is important to ensure that the sections of a split part are at the same level of a hierarchical design. It is also important to ensure that all sections of the split part have the same PSpice template.

Displaying PSpice Names

You can choose *AMS Simulator - Display PSpice Names* to contro the display of the `$PSPICE_LOCATION` value on the schematic. Selecting the *Display PSpice Names* option displays the `$PSPICE_LOCATION` value. If this option is not selected, the `$LOCATION` value is displayed provided Attributes dialog box specifies the value to be shown.

Fixed CCRs

The following lists the problems reported and fixed in PSpice 16.2. For detailed information about a fixed problem, contact your customer support.

CCR ID	Description
28533 (PCR 440305)	Displayed PSpice REFDES in Concept all over the shop
29513 (PCR 445494)	Duplicate AA Variables part in PSpice Special library.
38121 (PCR 482187)	PSpice Model for GTO Gate turn off Thyristor
173114 (PCR 737527)	Model request for Zener reference diode IS-1009RH
176520 (PCR 741292)	Need planar core models like E18/4-3C90-A250-E and ER23-3F3
186050 (PCR 751813)	change the shortcut keys for zoom in zoom out
188400 (PCR 754424)	Add component variable in concepthdl special library
201491 (PCR 768534)	Request for Vendor Models
203650 (PCR 770722)	Migration of SAC library from AWB into PSpice
296995 (PCR 872124)	Need to disable the zoom in functionality from Mouse
337567 (PCR 905137)	Measurement list to be updated after loading *.prb file
369582 (PCR 2369582)	Problems with measurements in Probe
385545 (PCR 2385545)	Problems with measurements in Probe
401140 (PCR 2401140)	Model request for CD 4094 8-bit shift register
403985 (PCR 4014859)	sir file is not generated if library still created
420841 (PCR 4018552)	AA crashes when user does not have Admin privileges
424280 (PCR 2424280)	Opening multiple dat files in Probe results in crash
426183 (PCR 2426183)	simserver module crash followed by RPC server unavailable message
446892 (PCR 2446892)	Level 2 BJT equations looks choped off in Page 282 of pspcref.pdf
447939 (PCR 2447939)	Models from ana_swit are missing mention on lib_list
452610 (PCR 4024986)	Lose waveform if Add plot is used in stimulus editor

468060 (PCR 2468060)	Archive mechanism does not work correctly
473887 (PCR 2473887)	LT1259/LT part in library LIN_TECH.OLB has worng pin types for GND pins
477348 (PCR 2477348)	Results in AA Sensitivity vary greatly depending on the no of components added in the AA UI for Legacy flow
484758 (PCR 2484758)	Simulation Server Crashes with RPC Unavailable message.
487682 (PCR 2487682)	Request for support of split parts for simulation purposes in CON_PSP flow
489400 (PCR 2489400)	TJ parameter for dual MOS infineon parts not getting smoke checked
492154 (PCR 4033412)	The d1n6036 model does not appear to be correct
496201 (PCR 4034512)	Need AMS Help files corrected for errors and typos
497874 (PCR 2497874)	Question : With reference to which manufacturer TL082 part has been created?
503744 (PCR 2503744)	Autoconvergence only for PSpice A/D
511148 (PCR 2511148)	Measurements not applicable for parametric sweeps
515818 (PCR 2515818)	Results not matching with HIer block
515959 (PCR 2515959)	Description of Probes moved from pspice_elem to Standard Library
516713 (PCR 2516713)	AUTOCONVERGE option description missing from pspug_concept.pdf
517209 (PCR 2517209)	Base current variation issue
518329 (PCR 2518329)	NatSemi LMV part symbols incorrect
521154 (PCR 2521154)	Enhancement: Ability to save multiple Macros with one click
522785 (PCR 2522785)	Option to enter Tknee value from datasheet for smoke calculation
522888 (PCR 2522888)	Option to display the GAIN property and value for E; F; G and H Parts
523440 (PCR 4041453)	PSpice part gives error while opening in part developer
524041 (PCR 2524041)	PSpice modes request for ARINC-429 drivers
524841 (PCR 2524841)	Request for Error Message while using Model with Name only in Numbers

526599 (PCR 2526599)	Components from BJN lib do not work
527636 (PCR 2527636)	Model editor duplicates lib definition in cds.lib while creating symbol
528569 (PCR 2528569)	Bias points not displayed in 16.0
530215 (PCR 2530215)	Incorrect simulation results using checkpoint restart
534087 (PCR 2534087)	Enhancement : Improve PSpice performance to handle large .dat
535442 (PCR 2535442)	Partname and generic name difference in lip_list.pdf
538891 (PCR 2538891)	AA Measurement evaluation fails PSpice evaluation works
548139 (PCR 2548139)	Components from BJN lib do not work
549025 (PCR 2549025)	Import txt file to probe
550073 (PCR 2550073)	Components from BJN lib do not work
551969 (PCR 2551969)	Incorrect menu reference on AA users guide
558007 (PCR 2558007)	Cannot display $Pspice_location attribute on schematic
558015 (PCR 2558015)	Unable to display $PSPICE_LOCATION property on Schematic
558101 (PCR 2558101)	Calculation of TJ/PDM in Smoke Analysis
568836 (PCR 2568836)	Smoke Derating calculation seems to be wrong
569008 (PCR 2569008)	0 symbol has no Voltage property
572452 (PCR 2572452)	Too few terminals on generated DE_HDL symbol
573430 (PCR 2573430)	Viewing the CheckPoints on the traces
574462 (PCR 2574462)	Incorrect simulation results using checkpoint restart
575457 (PCR 2575457)	Documentation errors in pspug and pspcref
576261 (PCR 2576261)	Appending .DAT file with Import text format waveform result in incorrect results
576445 (PCR 2576445)	Issue in displaying current plots for multi design
577552 (PCR 2577552)	No simulation data for marker warning message
577868 (PCR 2577868)	On PSpice projects want to make $location invisible automatically
577874 (PCR 2577874)	Next Page option does not open the correct Page

577889 (PCR 2577889)	analog toolbar grayed out in multi design environment
578302 (PCR 2578302)	$PSPICE_LOCATION Property visibility is inconsistent
578818 (PCR 2578818)	Incorrect number of arguments for macro
580727 (PCR 2580727)	cir file options for check point restart and auto converge
585837 (PCR 2585837)	Cannot display $Pspice_location attribute on schematic
586373 (PCR 2586373)	Message "Failed to create PSpice netlist" after moving part in schematic.
589828 (PCR 2589828)	Missing Model Error using 2N3501 part from AA BJN Library
600419 (PCR 2600419)	$PSPICE_LOCATION Property invisible in the Schematic
601102 (PCR 4063637)	ENVMAX function hangs Probe window
603759 (PCR 2603759)	Discrepancy between Linear and Log graph style in sensitivity analysis
608544 (PCR 2608544)	Crash due to incorrect memory delete

What’s New in OrCAD PCB Editor

This chapter describes the new features in PCB Editor 16.2.

Important

OrCAD PCB Editor is available with the OrCAD PCB Designer and OrCAD PCB Designer with PSpice suite licenses.

New Features and Enhancements:

- Etch Edit Applications
- Manufacturing Applications
- Padstack Enhancements
- Design-Level DRCs
- Productivity Enhancements
- Miscellaneous Productivity Enhancements
- Color and Graphics
- Miscellaneous Manufacturing Applications and Interfaces
- Database

Etch Edit Applications

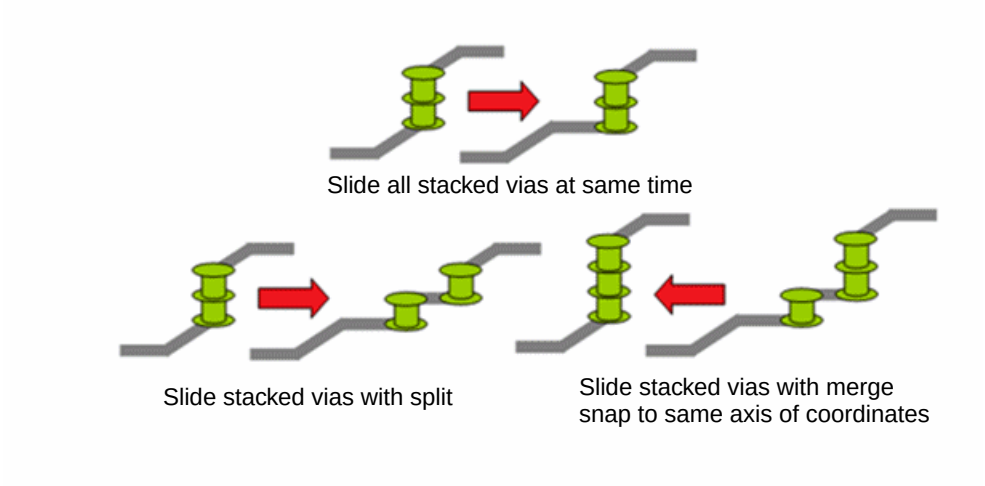
This section describes:

- Improved Stacked Via Handling
- Tangent Rule Adherence
- Sliding Via-in Pad

Improved Stacked Via Handling

Stacked vias are now seen as a group entity by the `slide` command. Slide a pair of stacked microvias or the complete stack of micro and core vias with a single pick. While executing the `slide` command, right-click and choose the *Split Stack* command to separate via instances from the stack. Merge a via into a stack, rules permitting, by sliding it into the adjacent via. At this point, the via on your cursor snaps to the adjacent via to form a stack.

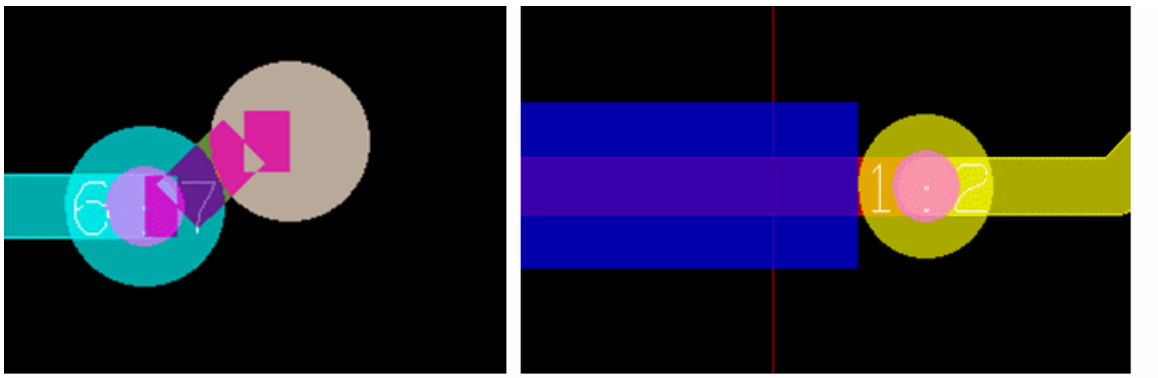
Figure 4-1 Stacked Vias



Tangent Rule Adherence

As a result of etch edit alignment with the Same Net DRC system, the sliding of vias to be tangent with other vias or pins is now done effortlessly.

Figure 4-2 Via:Via =0 (left) and Via:SMD Pin=0 (right)



Sliding Via-in Pad

Sliding a via located in a pad to a point outside the pad boundary now produces a cline attachment. Prior to 16.2, this resulted in an orphan via.

Manufacturing Applications

This section describes:

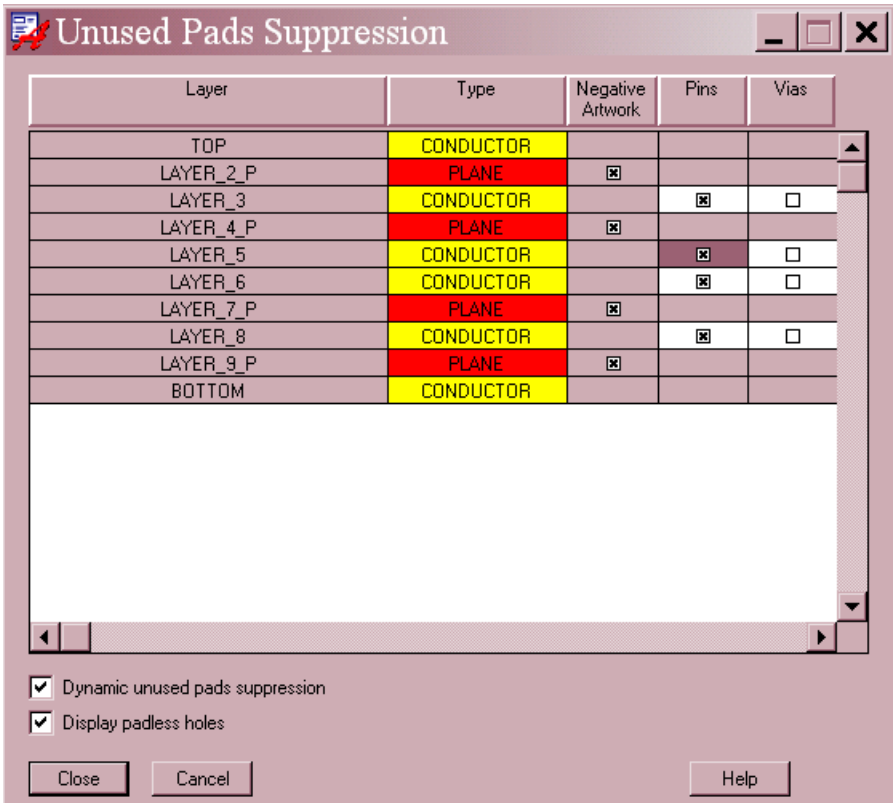
- Dynamic Unused Pad Suppression
- Exception Properties
- Drill Hole to Metal DRC
- Shape-based Fillets

Dynamic Unused Pad Suppression

The removal of unused inner layer pads has traditionally been used to reduce capacitance effects at each hole site. The fabricator's CAM department would be responsible for this application prior to film generation. Possibly the OEM removed the pads as a function of the artwork generation process. With the ever increasing demand to miniaturize consumer products, unused inner layer pads are being removed not only for electrical effects but also for physical. Specifically, by removing pads, higher routing densities are achieved by allowing traces to be closer to the edge of the hole. On HDI designs, candidates for pad removal can be the unused internal layer pads of the core via.

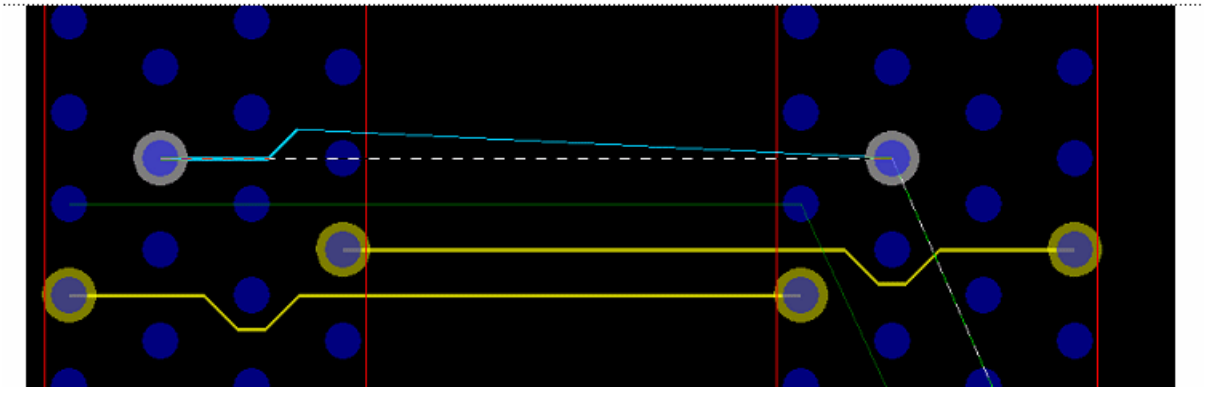
The *Unused Pad Suppression* user interface controls the suppression state for pins and vias. Suppression can be applied to any or all of the inner signal subclasses. Exceptions include Top and Bottom layers, negative planes, and begin and end layers of blind and buried vias.

Figure 4-3 Unused Pad Suppression UI



Pad suppression enters a dynamic state once the dynamic option is enabled and form closed. At this point, all eligible pads are removed. Pads are restored as connections are made to inner layer pins or vias. Conversely, pads are dynamically removed when etch is deleted from pins/vias.

Figure 4-4 Dynamic Pad Restoration



Exception Properties

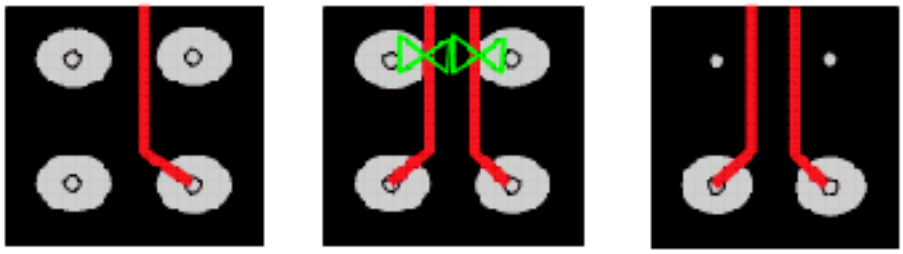
- UNUSED_PAD_IGNORE: Use to prevent pads from being removed at the symbol, net, pin, and via level.
- UNUSED_PADS_OVERRIDE: Use to allow pad removal on outer layer elements (edge connector, for example).

Drill Hole to Metal DRC

A new class of hole-based checks, supported in both Spacing and Same Net domains of Constraint Manager, provides the DRC capability when Unused Pad Suppression is enabled or pad definitions are set to null. A hole-to-metal check occurs only when the respective hole is void of pads on conducting layers. When pads are present, the hole check yields to the convention pin and via checks.

The following example illustrates the potential benefits of drill-based checks. The channel width with pads present restricts the number of lines routed between the pin pads to just one. The removal of used pads coupled with a Hole to Line space that permits the line to be routed closer to the edge of the hole but tangent to the annular ring opens up the channel to permit two lines between.

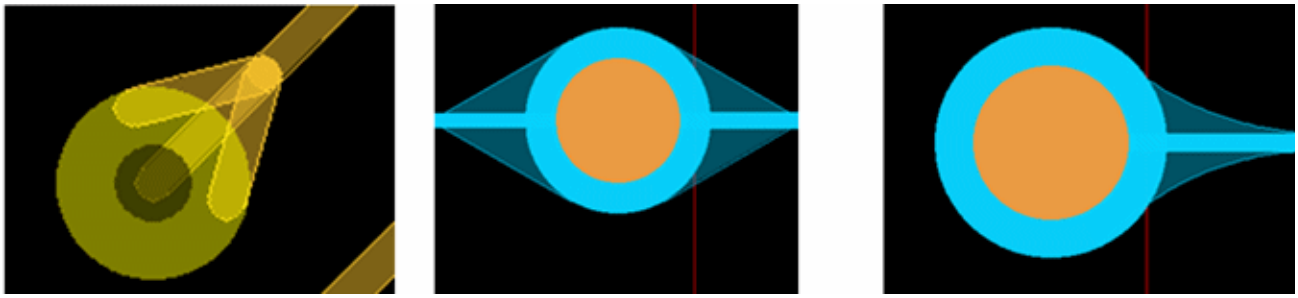
Figure 4-5 Drill Hole to Metal DRC



Shape-based Fillets

The fill associated with fillets has transitioned from line- to shape-based. A single entity fillet is managed more efficiently in the database. For DRC considerations, regard the fillet as an extension of the pin or via.

Figure 4-6 Line- (left), Shape- (middle), and Shape-based Curve Fillets (right)



Fillet Parameter Enhancements

New parameters associated with the fillet application include:

- Allow DRCs: Fillets can be created with DRCs
- Max Line Width: Enable to prevent fillets from be added when junction line width is equal to or greater than this value.

Exception Property

The NO_FILLET property can be applied to pins, vias, and nets to prevent restoration of fillets in dynamic mode.

Padstack Enhancements

This section describes:

User-Defined Mask Layers

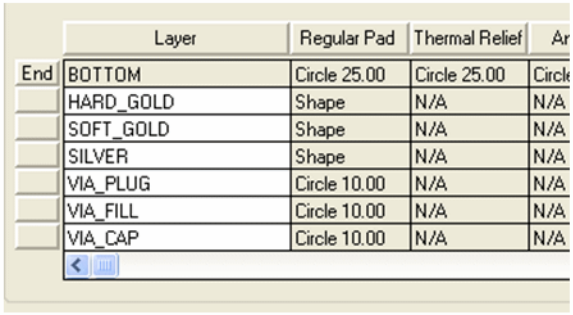
Non-Standard Drill Types

Slotted Vias

User-Defined Mask Layers

The padstack definition now supports a maximum of 16 user-definable mask layers. Mask layers can be used for HDI via plugging, filling, capping, or other masking applications such as silver as well as hard and soft gold. DRCs are not performed on these layers.

Figure 4-7 User-Definable Mask Layers



	Layer	Regular Pad	Thermal Relief	Ar
End	BOTTOM	Circle 25.00	Circle 25.00	Circl
	HARD_GOLD	Shape	N/A	N/A
	SOFT_GOLD	Shape	N/A	N/A
	SILVER	Shape	N/A	N/A
	VIA_PLUG	Circle 10.00	N/A	N/A
	VIA_FILL	Circle 10.00	N/A	N/A
	VIA_CAP	Circle 10.00	N/A	N/A

Non-Standard Drill Types

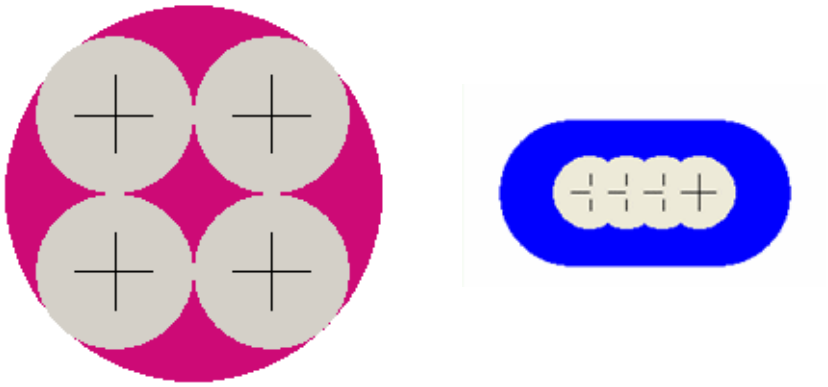
Additional HDI drill types are available in the *Non-standard Drill* section of the Padstack Editor. Use non-standard attributes to control NC Drill output.

- Wet/Dry etching
- Photo Imaging
- Conductive Ink Formation

Slotted Vias

Plural vias are used in high-current applications. The *Multiple Drill* section of the Padstack Editor form now supports negative clearance entries for slot formation.

Figure 4-8 Examples of Multiple Microvias



Design-Level DRCs

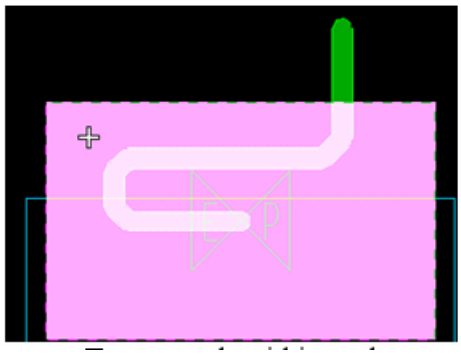
This section describes:

- Etch Turn Under SMD Pin
- Exception Properties for Etch Turn under SMD Pin
- Mechanical Pin to Metal

Etch Turn Under SMD Pin

This check detects etch compensation buried within the pad. Driven by concern that etch segments within pad boundaries adversely affect timing rules, the checker reports if more than two vertex points are located within the pad boundary. By default, this check only applies to nets with timing or length rules.

Figure 4-9 Excess Etch Within Pad



Exception Properties for Etch Turn under SMD Pin

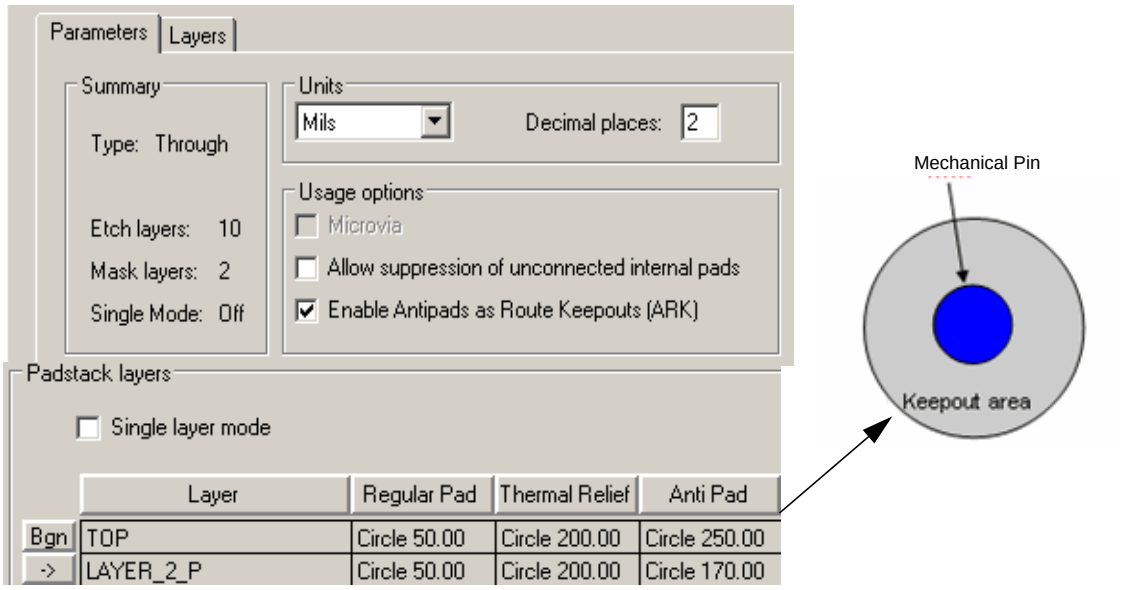
- ETCH_TURN_UNDER_ALL_PADS - enable this drawing-level property to check all nets.
- ETCH_TURN_UNDER_PAD - Suppresses DRCS at symbol, net, pin level.

Mechanical Pin to Metal

Mechanical pins are non-logical elements, typically used as mounting or tooling holes and fiducials. Manually drawn keepout areas are traditionally attached to the mechanical symbol to restrict etch around the perimeter of the hole or pad. A new pad usage option, *Enable Antipads as Route Keepouts (ARK)*, permits the antipad associated with the padstack of

the mechanical pin to be used as an implicit route keepout area. The mechanical pin checks are located in the Design Modes form.

Figure 4-10 Mechanical Pin to Metal



Productivity Enhancements

This section covers:

- Context-Sensitive Editing
- Automatic Execution of Commands
- Funckey Key Suggestions for Snap

Context-Sensitive Editing

The right mouse button is context sensitive where commands and parameter options associated with component placement are available based on the selection set of elements. A context-sensitive environment reduces the extra steps involved in traveling to the toolbar, menus, or Options tab while maintaining focus on the work area in the canvas.

An example of context-sensitive menus is shown in the figures below. The menus are a result of either hovering over or selecting with the left mouse button a symbol or pin followed by a right mouse button pick.

Figure 4-11 Symbol-based Commands (left) and Pin-based Commands

Automatic Execution of Commands

Certain commands associated with component placement can be automatically executed using the left-mouse-button pick or drag functions. Simply click on a symbol, group, text or rat T to move it. *Spin* or *Copy* commands require the combination of either the `Shift` or `Ctrl` key while in a drag operation with the left mouse button.

Placement Application Mode - Automatic Execution of Commands

Element Type	Drag	Shift Drag	Ctrl Drag	Single Click
Group	*Move*	*Spin*	*Copy*	*Move*
Symbol	*Move*	*Spin*	*Copy*	*Move*
Text	*Move*	*Spin*	*Copy*	*Move*
RatT	*Move*			*Move*

Graphical User Interface

Convenient access to unplaced components is available from the side options panel. This form is a subset of the master placement user interface and offers a *Place by Refdes* field with wildcard support.

Figure 4-12 Placement Edit Application Mode

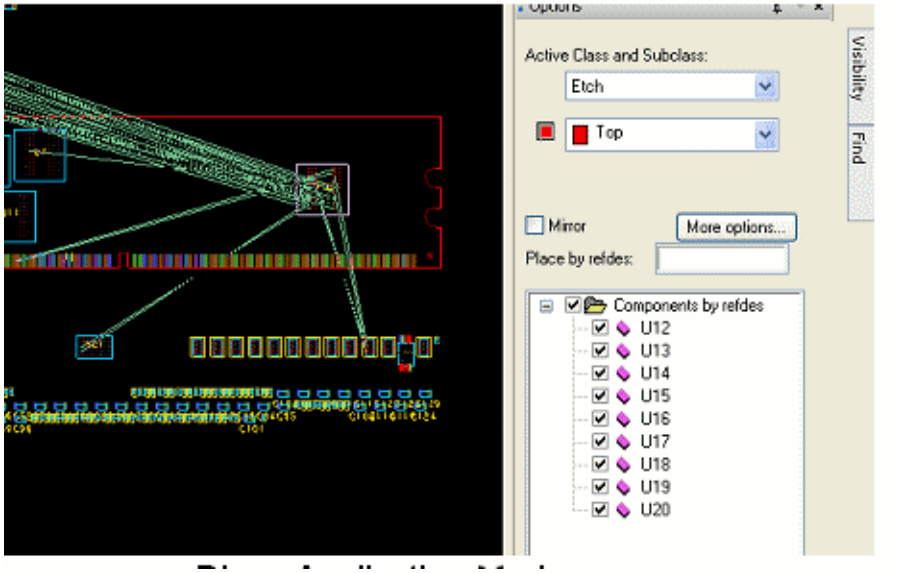
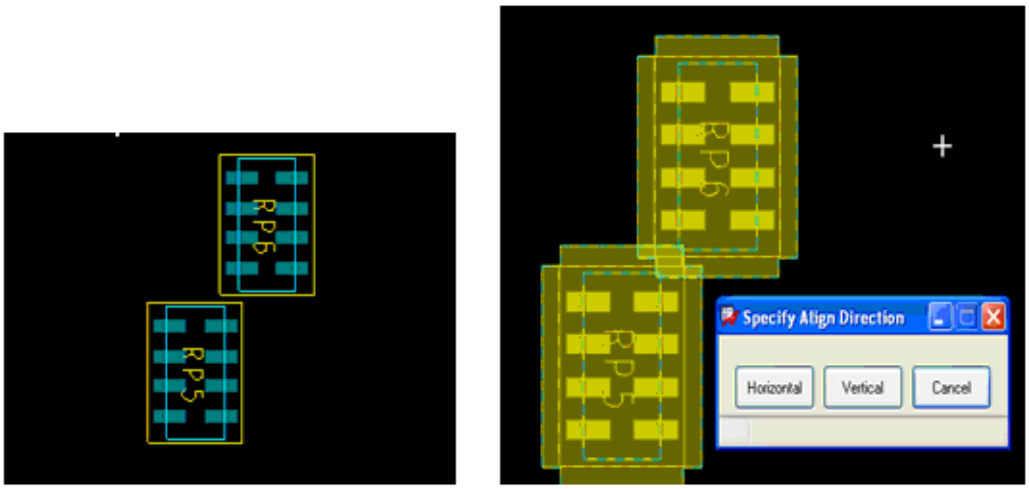


Figure 4-13 Before Alignment (left) and User-Prompt for Direction (right)



Snap Integration Across Edit Commands

Snapping functionality has been integrated to many editing commands associated with backend SPB products. Applications involving the use of snap may include the manual placement of mechanically constrained components such as connectors, key pads, or mounting holes to targets imported from an MCAD system or snapping a testvia to a fixture probe location. There are 11 snap options available on the right-mouse-button menu of most editing commands (move, slide, and place manual), for example. The use model entails positioning the cursor over or near the target object while in an edit-based command followed by right-clicking and choosing the *Snap Pick to* function. Confirmation of the snap appears in the console command window.

Figure 4-14 Snapping

Slide used to snap testvia to probe figure

Snap completed to figure

Funckey Key Suggestions for Snap

The use of functions keys can accelerate the actions from the right mouse button. Simply hover near the target object, then click the respective key to initiate the action. Here are a few examples:

```
funckey f "prepopup;pop dyn_option_select 'Snap pick to@:@Figure'"
funckey i "prepopup;pop dyn_option_select 'Snap pick to@:@Intersection'"
funckey c "prepopup;pop dyn_option_select 'Snap pick to@:@Arc/Circle Center'"
funckey v "prepopup;pop dyn_option_select 'Snap pick to@:@Via'"
```

Miscellaneous Productivity Enhancements

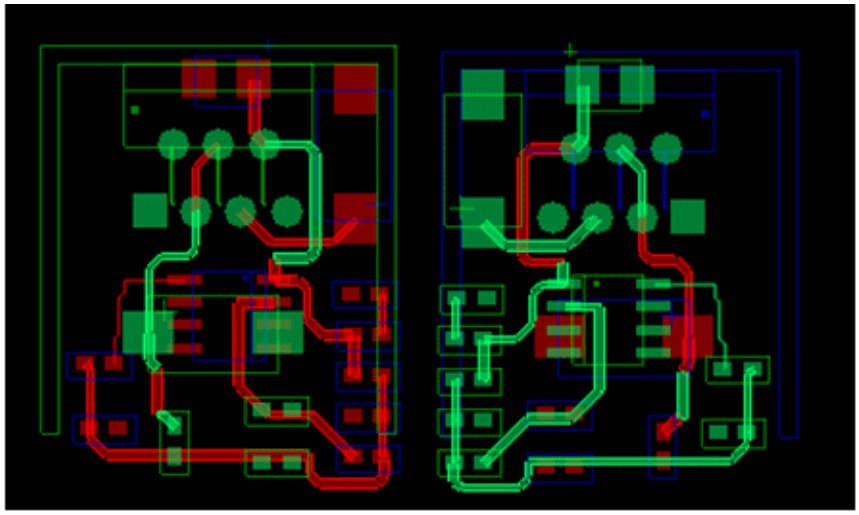
This section describes:

- Mirror support for Re-Use Modules
- Replace Padstacks by Window Selection
- `Prepopup/Pick` Commands
- Subdrawings
- Dialog Boxes

Mirror support for Re-Use Modules

Modules can now be mirrored using the *Group Find Filter* option. From the *Edit – Mirror* command, enable *Group* from the *Find Filter*, then select the module.

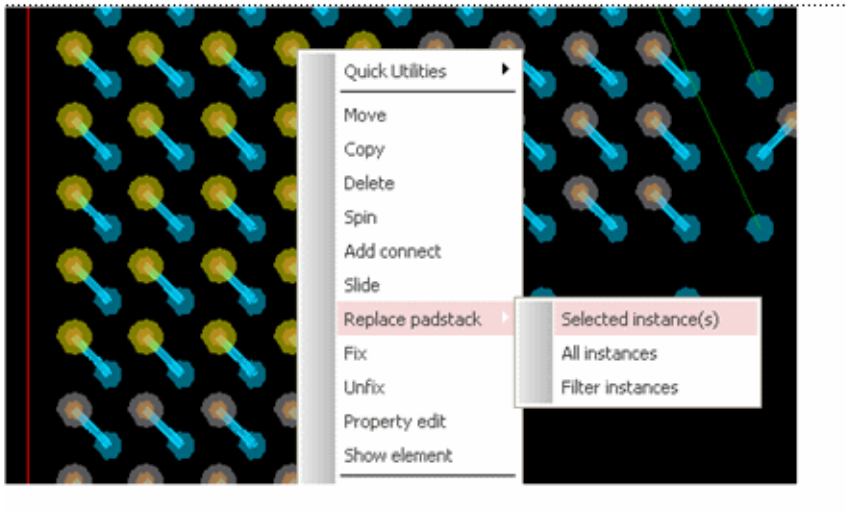
Figure 4-15 Mirror Support for Re-Use Modules



Replace Padstacks by Window Selection

Using general edit application mode, window around a group of vias, then right-click and choose the *Via – Replace Padstack – Selected Instances* command. Use the `Shift` or `Ctrl` keys to extend or toggle the selection. Consider setting the *Super filter* to via to eliminate a step in the right mouse button menu path as shown below.

Figure 4-16 Replace Padstacks by Window



`Prepopup/Pick` Commands

The `prepopup` and `pick` family of commands now supports a `-cursor` option. This option is targeted for use in funckeys. If this option is present,the command will use the current location of the cursor as the pick location. With prepopup, no arguments imply the `-cursor` option.

Function Key examples:

- Click Space Bar to add via at cursor location:

```
funckey " " "pop bbdrill-cursor"
```

- Click F key to Snap selected object to closest figure:

```
funckey f  "prepopup;  pop dyn_option_select 'Snap pick to@:@Figure'"
```

- Click D key to delete element at cursor location:

```
funckey d "prepopup; pop dyn_option_select @:@Delete"
```

Subdrawings

Sub-drawing (clipboard) will now preserve constraint region membership of a constraint area.

Dialog Boxes

Padstack names now use alphanumeric sorting in most dialog boxes.

Color and Graphics

This section describes:

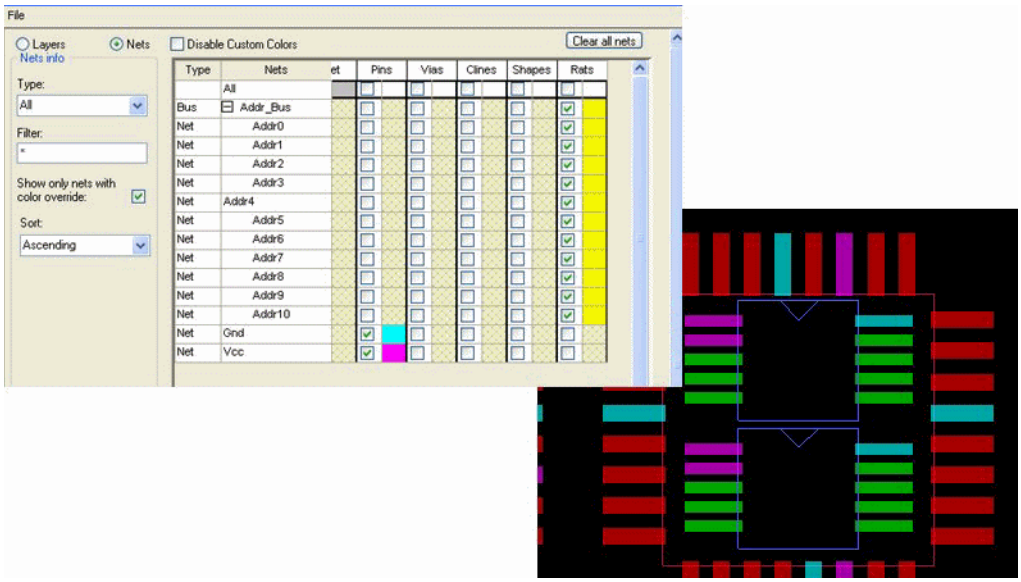
- Net Element Coloring
- Highlighting and Coloring
- Display Priority

Net Element Coloring

The *Color* dialog has been enhanced to support *Net* element coloring. The new *Net* worksheet lists net objects where unique colors can be assigned to their respective elements. These elements consist of pins, vias, clines, shapes, and ratsnests. An example might be the need to color the vias of the GND net green while maintaining default colors across the remaining elements of the net.

The *Net* worksheet supports bus, diff pair, Xnet and net objects. Colors assigned at the hierarchical level descend to their respective membership. Filtering is available to display only the nets with color overrides making the display easier to manage. Color settings can be preserved while reverting back to layer based colors by a disablement option built into the form. Alphanumeric sorting and net override sorting is an available option. Color settings can also be saved and reloaded as a function of the design parameter file.

Figure 4-17 GND and Vcc Pin Coloring



Highlighting and Coloring

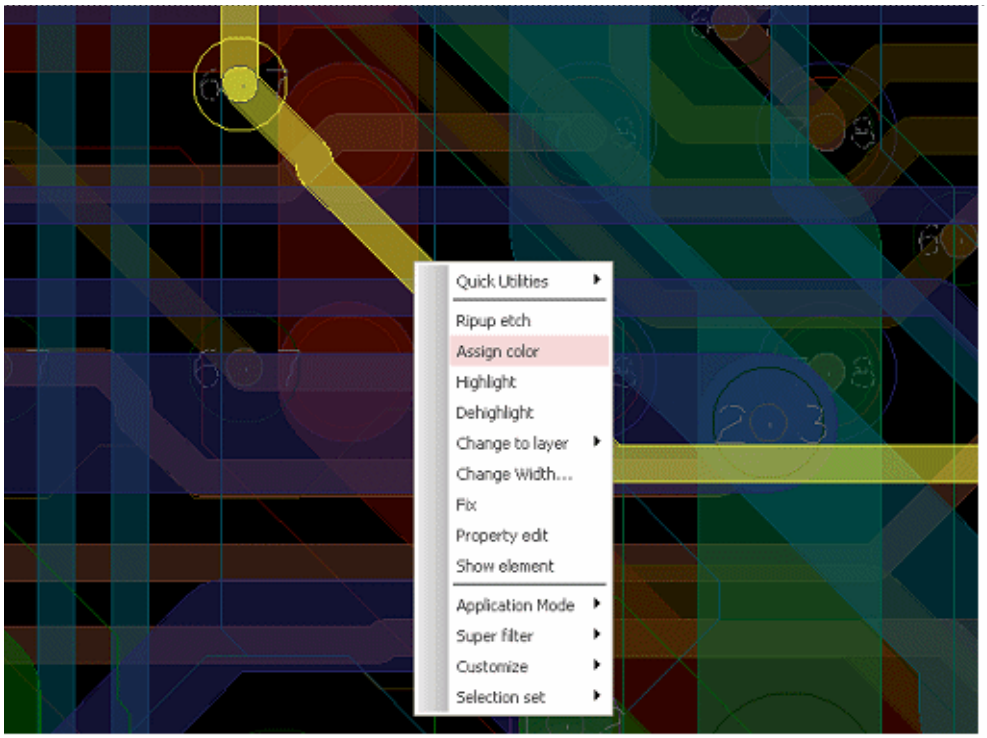
There are three states of graphical accentuation in the SPB backend tools. An element can be:

- Colored
- Highlighted
- Colored and highlighted

Prior to 16.2, the `highlight` command served dual roles as a coloring and accentuation function. The 16.2 release separates these functions but also offers a state that emulates previous behavior; hence the third option mentioned above.

In addition, elements can be assigned color by hovering over them, then right-clicking and choosing the *Assign Color* command.

Figure 4-18 Assign Color Added to Context-Sensitive Menu



Display Priority

Display priority, formally done on the basis of color, has changed to a subclass-based model. Objects are drawn within their respective groups (*Stackup, Board Geometry, Package Geometry and Components, Manufacture*, etcetera) in a predetermined order to ensure key elements are not blocked by solids. Examples of elements designed to appear on top of other graphical elements include DRCs, diff pair uncoupling segments, and ratsnests.

Unchanged is the method Allegro uses to draw at the system level. The order of priority continues to be:

1. Permanent highlight objects
2. Active subclass
3. Remaining objects, including ones assigned a color override
4. Dimmed objects

Miscellaneous Manufacturing Applications and Interfaces

This section describes:

- Drills
- Artwork
- Cutmarks
- Valor
- Reports

Drills

- The Drill Legend dialog box (`ncdrill legend` command) now has a *Library* button to load template files via the *`nclegend`* path variable.
- Plotting of drill holes is now supported on Windows systems.

Artwork

- Prefix and suffix Support

  Parameter-driven option to globally prefix and suffix the film file names created from the layout tool. These affixes are supported on a per design basis. Control these strings via the *Global film filename affixes* fields found in artwork's dialog *General Parameters* tab. They can also be set via design properties; ARTWORK_PREFIX and ARTWORK_SUFFIX. This enhancement, while not removing the root film name limit of 18 characters, does allow the generation of a film file names of up to 256 characters. While Allegro permits longer film names, your operating system generally limits file names (including the extension) to 256 characters. Example, if the film name is TOP and the prefix is `front-` and the suffix is `-back,` then the resulting file name will be `front-TOP-back.art.`

- Artwork Film Filename Extension Definition

  Allegro's default file extension for artwork film names is `.art`. This can be modified by setting the EXT_ARTWORK environment variable. If you plan on changing the default, Cadence recommends that you do this at your CDS_SITE level so that a common extension can be used by your company. You should verify that your downstream tools can support the extension you choose. This can also be used with the existing environment variable, ADS_SDART to control the directory where artwork files are deposited. Cadence recommends that a relative path be used with this variable.

- Artwork now treats filming layers whose polarity (positive/negative) does not match the artwork polarity as an error condition.

Cutmarks

The `cut marks` command now supports designs using inch units.

Valor

- The `extract valor_view.txt` file has been renamed to `old_valor_view.txt` in the Cadence view directory to avoid conflicts with the file supplied by Valor.
- Use the environment variable ALLEGRO_BRD2ODB_USER_OPTIONS to set Valor interface options not available from the Allegro dialog box.

Reports

- *Unused Blind/Buried Via*: This new report detects unused buried or blind vias included in a stack. The removal of these vias can open up routing real estate and reduce stub effects at the via site.
- *Dangling Line - Antenna Via* section added along with formatting updates.
- *Missing Fillets*: Lists junctions with missing or partial fillets.

Database

This section covers:

- DBdoctor
- Batch DRC
- Downrev to Release 16.01
- New Variables
- New Properties
- Changed Properties
- Deleted Properties
- Sample env File

■ Performance Enhancements

DBdoctor

DBdoctor now reports as warnings non-plated padstacks used for connections.

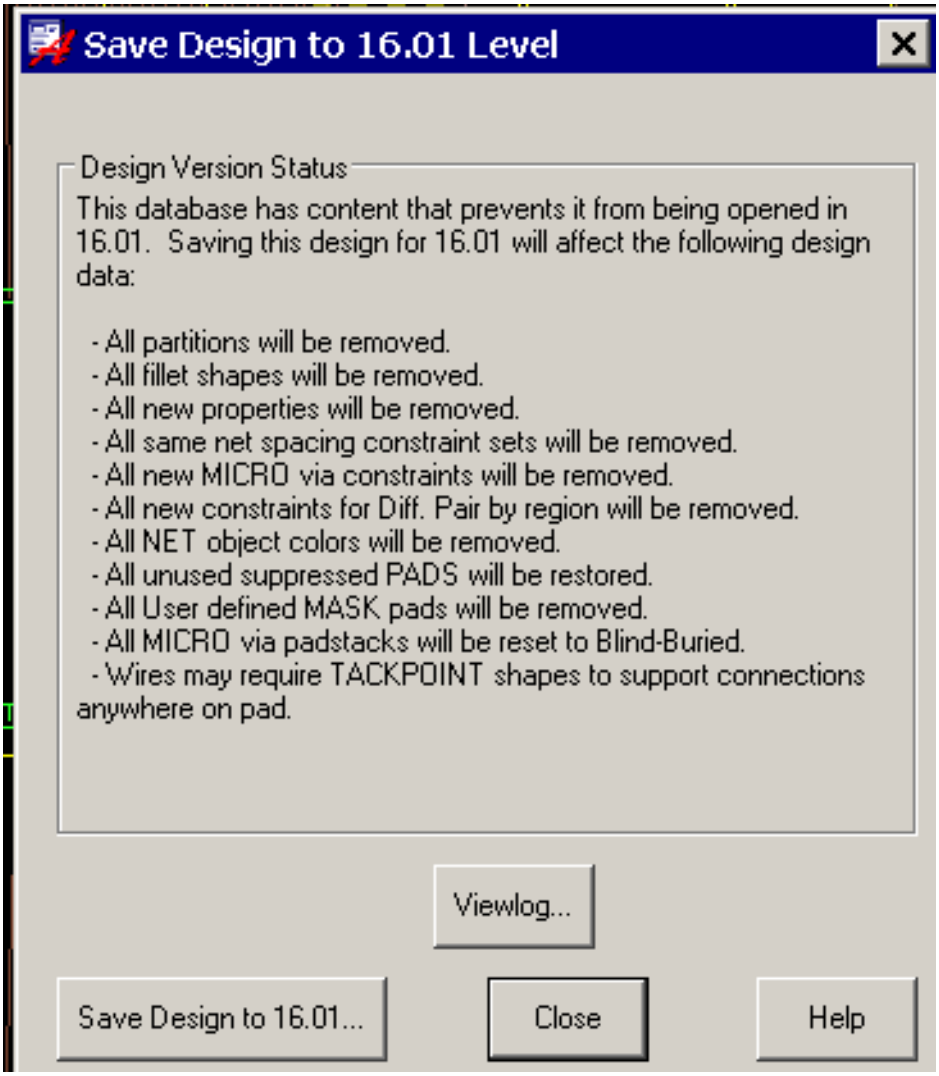
Batch DRC

The `batch_drc.log` file format now reports delta times for each DRC pass.

Downrev to Release 16.01

Downrev to Release 16.01 is available from the *File – Export* menu. Caution is advised due to the magnitude of changes made in Release 16.2 especially in the area of Same Net Constraints.

Figure 4-19 Downrev to 16.01



New Variables

`lstpath` - search path to locate list files

New Properties

("xxx" string indicates a multiple properties with a root name)

- VIA_AT_SMD_FIT, SN_xxx, ETCH_TURN_UNDER_PAD, VIA_AT_SMD_THRU, MECH_PIN_TO_MECH_PIN, HOLE_xxx,

SAME_NET_SPACING_CONSTRAINT_SET, xxx_MVIA_xxx, MECH_PIN_TO_CONDUCTOR_SPACING

- ETCH_TURN_UNDER_PAD_EXEMPT, ETCH_TURN_UNDER_ALL_PADS
- DIFFP_USERS_PROPERTIES - boolean set at board level, tiers PCB L Perf and above.
- LAST_PIN_SWAP - set on pin
- UNUSED_PAD_IGNORE and UNUSED_PADS_OVERRIDE
- ARTWORK_PREFIX and ARTWORK_SUFFIX - board-level strings
- INCLUDE_IN_RF_TOPOLOGY
- NO_FILLET - net, pin, and via boolean property

Changed Properties

- PACKAGE_HEIGHT_MAX and PACKAGE_HEIGHT_MIN are now supported on the component definition.
- DFA_DEV_CLASS is no longer supported on the symbol instance. This was an error since the DFA DRC checker does not support this property at the symbol instance level.

Deleted Properties

- SAME_NET_VIA2VIA_SPACE - superseded by the Same Net constraint domain.

Sample env File

An annotated `env` file with example funckeys is provided at this location:

<cdsroot>/share/pcb/examples/env_examples.txt.

Performance Enhancements

- Dynamic Shapes

Substantial performance improvements with dynamic shapes on complex designs. In general, the more voiding of a shape that is required the better the performance gain. Noticeable improvements in both the etch editing and batch updating of shapes.

  - Some general improvements and global improvements if designs are migrated to new teardrop (fillet) method.

- Performance improvements in DRC with complex designs. Additional targeted areas of improvement are:
  - Designs with > 3000 active DRC errors
  - Designs with more then 400 waived DRC errors
  - DFA checking (typically see a 7x or better improvement in this area)

What’s New in OrCAD Signal Explorer

This chapter describes the new features in Signal Explorer 16.2

Important

OrCAD Signal Explorer is available with the OrCAD Designer license.

New Features and Enhancements:

- EMS2D Full Wave Field Solver
  - Coplaner Waveguides
  - Library Enhancements
  - Dispersive Material Support
  - Algorithm-Based Interconnect Modeling
- Enhanced Etch Factor Support
- Channel Analysis Developer’s Toolkit
- ICM Support
- Non-Native Database Support
- Spectre Upgrade
- Eye Mask and Measurement Enhancements

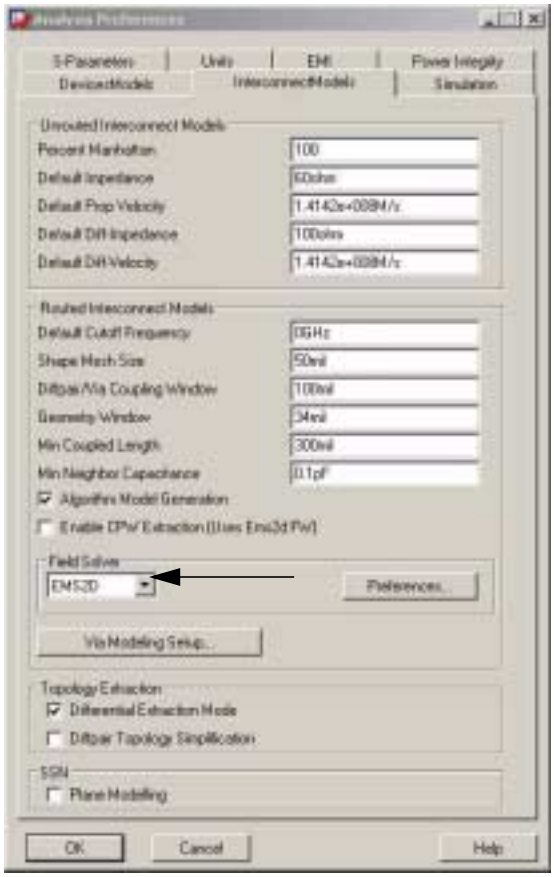
EMS2D Full Wave Field Solver

The Electromagnetic Solution 2D Full Wave field solver–EMS2D–in PCB SI and SigXplorer provides the full-frequency range analysis from DC, through the middle frequency range which covers the skin effect, to the THz range of the electromagnetic interactions which address resonances, radiations and EM signal integrity issues.

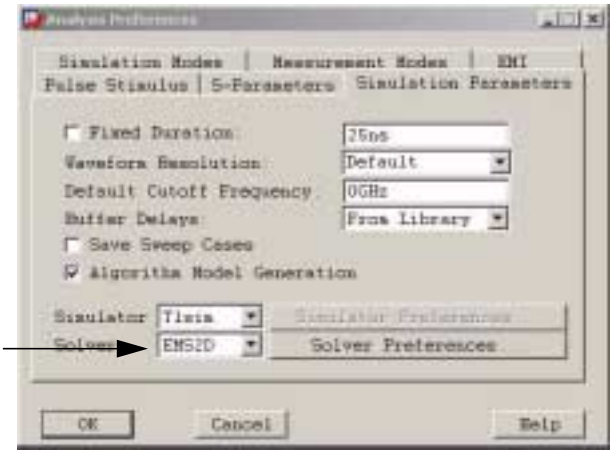
EMS2D is implemented using the finite element method (FEM), which complements Allegro’s moment-based BEM2D field solver. EMS2D combines multiple EM computation modules, static, quasi-TEM, and full-wave analysis. Additionally, EMS2D is able to analyze arbitrary

transmission line-type and waveguide structures over PCB cross-sections and provide characterized models in RLGC and/or S-Parameter format.

Figure 5-1 EMS2D Field Solver Selector in Analysis Preferences Dialog Boxes



PCB SI



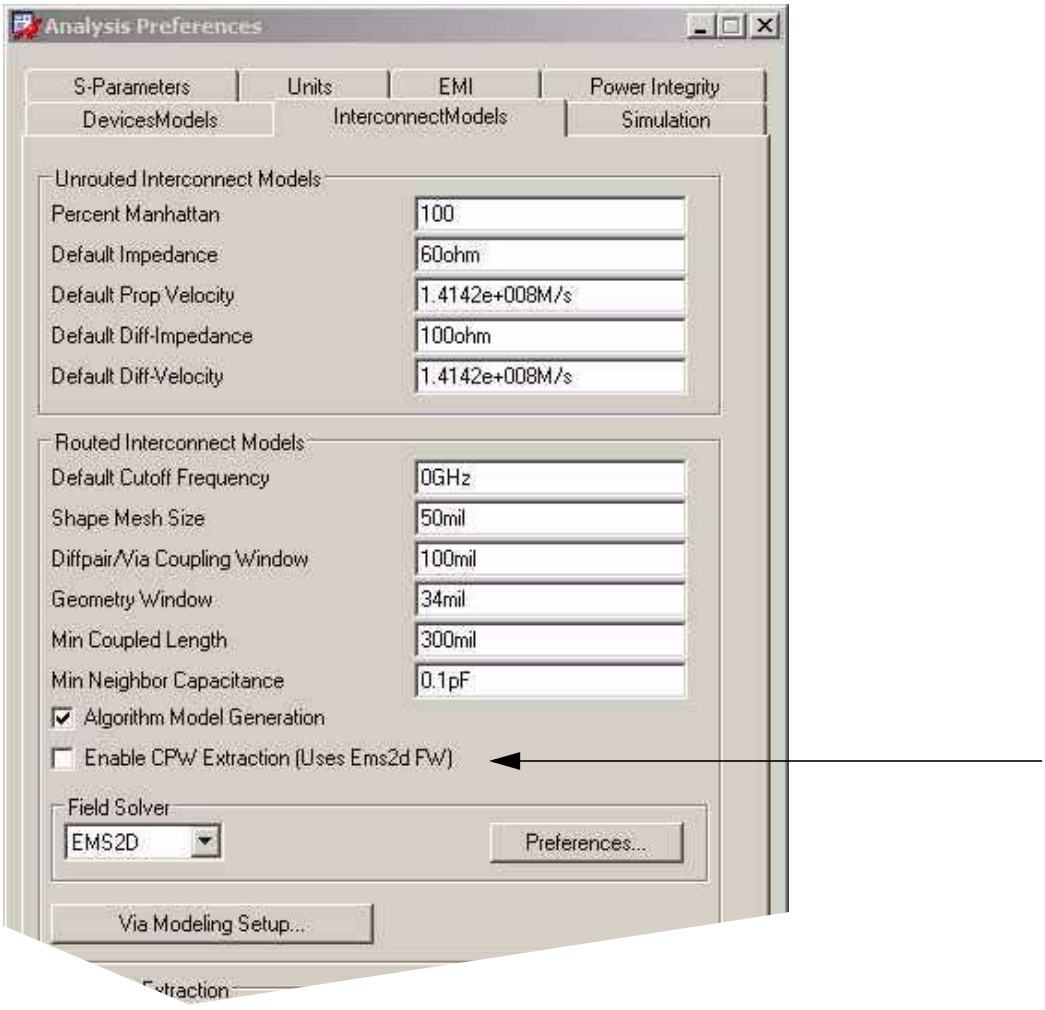
SigXplorer

The EMS2D full wave field solver supports the following capabilities:

Coplaner Waveguides

EMS2D supports analyses of coplaner waveguide (CPW) structures, including single and differential coupled CPWs in differential pair, microstrip, or stripline types. In Allegro PCB SI and SigXplorer, you can extract CPWs for model generation by enabling the CPW extraction option in the tools' Analysis Preferences forms.

Figure 5-2 CPW Extractor Option

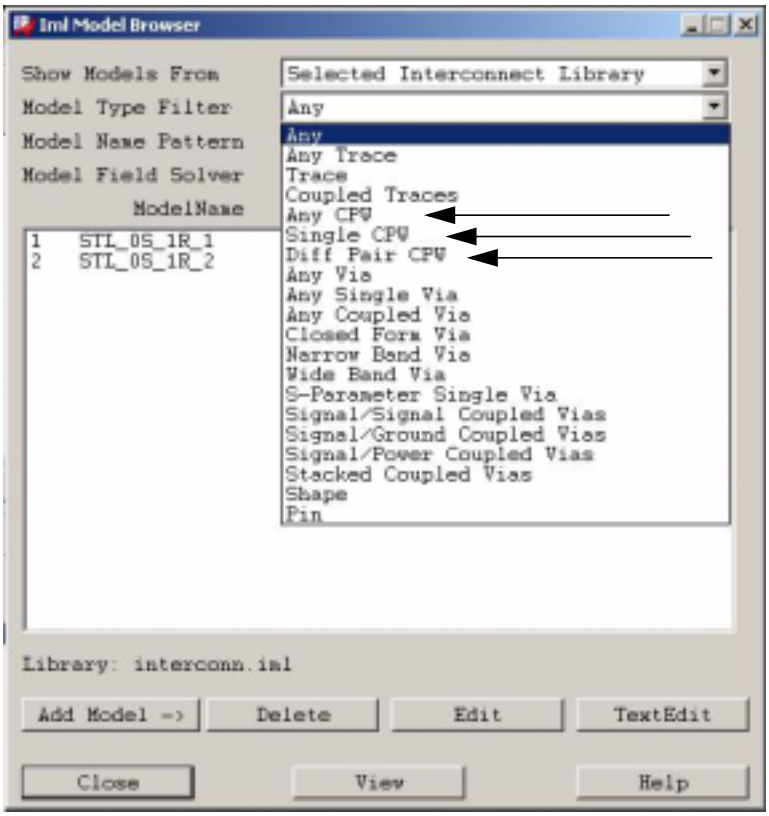


Library Enhancements

Interconnect libraries in Allegro products that support EMS2D contain a number of enhancements, including:

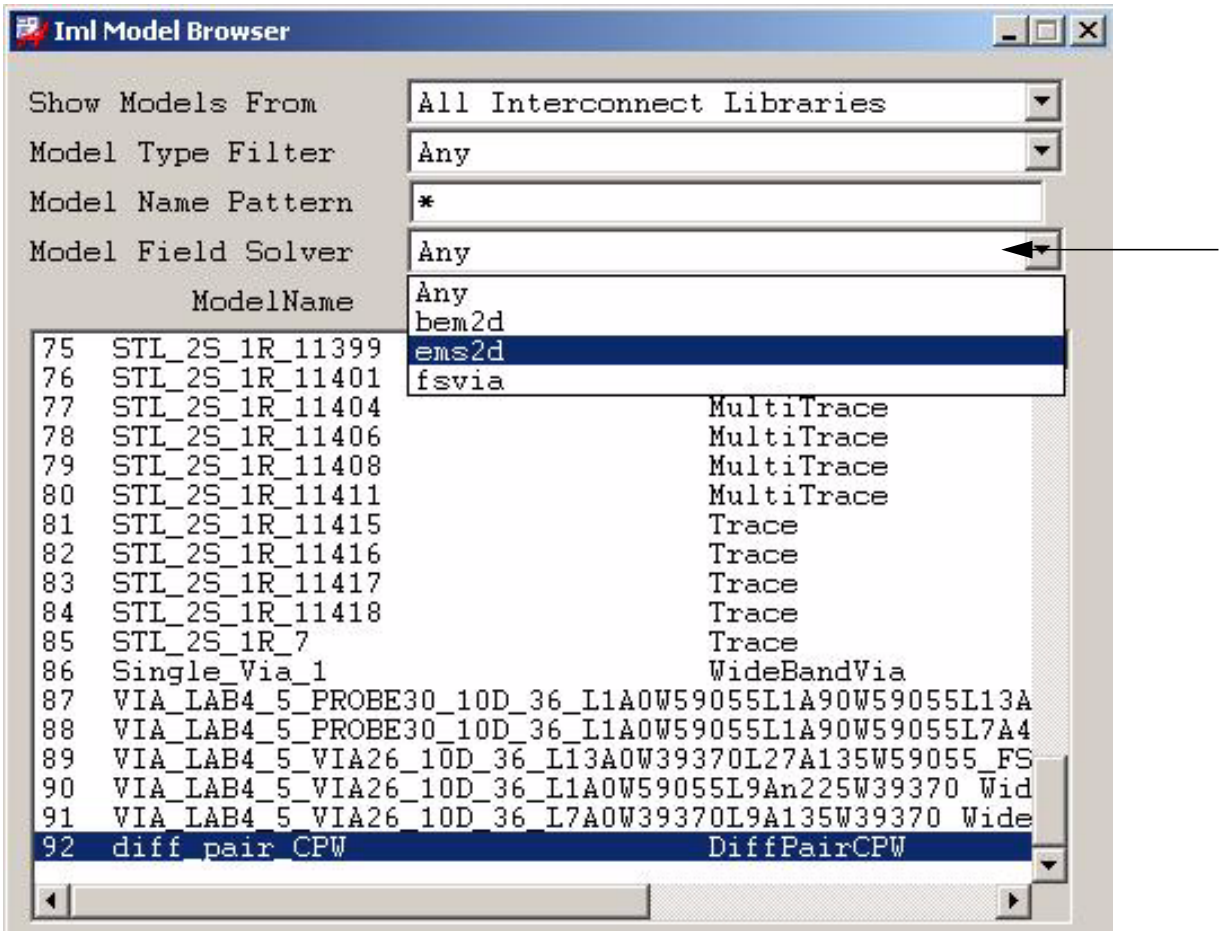
- CPW structures represented by interconnect models in IML libraries. You can filter model displays in the Iml Model Browser or create new or cloned models for single and/or differential pair CPWs.

Figure 5-3 CPW Models in the IML Model Browser



- Interconnect models that are created by specific field solvers and identified as such in the model syntax (`FieldSolver`). This information is used to “tag” models that can be reused by the field solver that created the model. Models created by specific field solvers are displayed in the Iml Model Browser when the appropriate field solver is selected from the *Model Field Solver* drop-down menu.

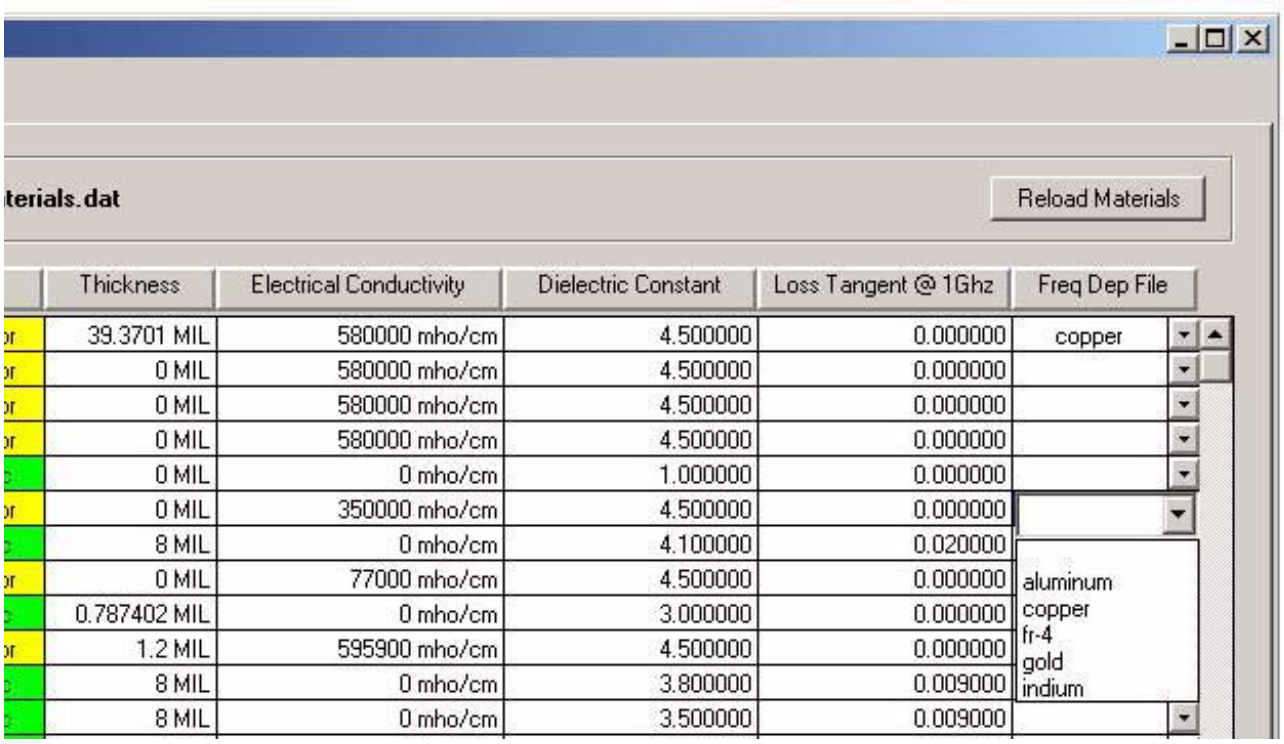
Figure 5-4 Model Field Solver Selector



Dispersive Material Support

The EMS2D field solver is capable of accurately modeling the delay and dispersive behavior of arbitrary materials, thus allowing rigorous analysis of frequency-dependent material properties. Frequency-dependent materials are defined in a frequency-dependent material (`.material`) file. This file contains electrical properties for individual materials (for example, FR4) defined over a range of frequencies. Frequency-dependent material files for specific materials and/or layers are defined graphically in the Material Properties and Layout Cross Section forms in your Allegro tools.

Figure 5-5 Material File Selectors in Materials Properties Dialog Box

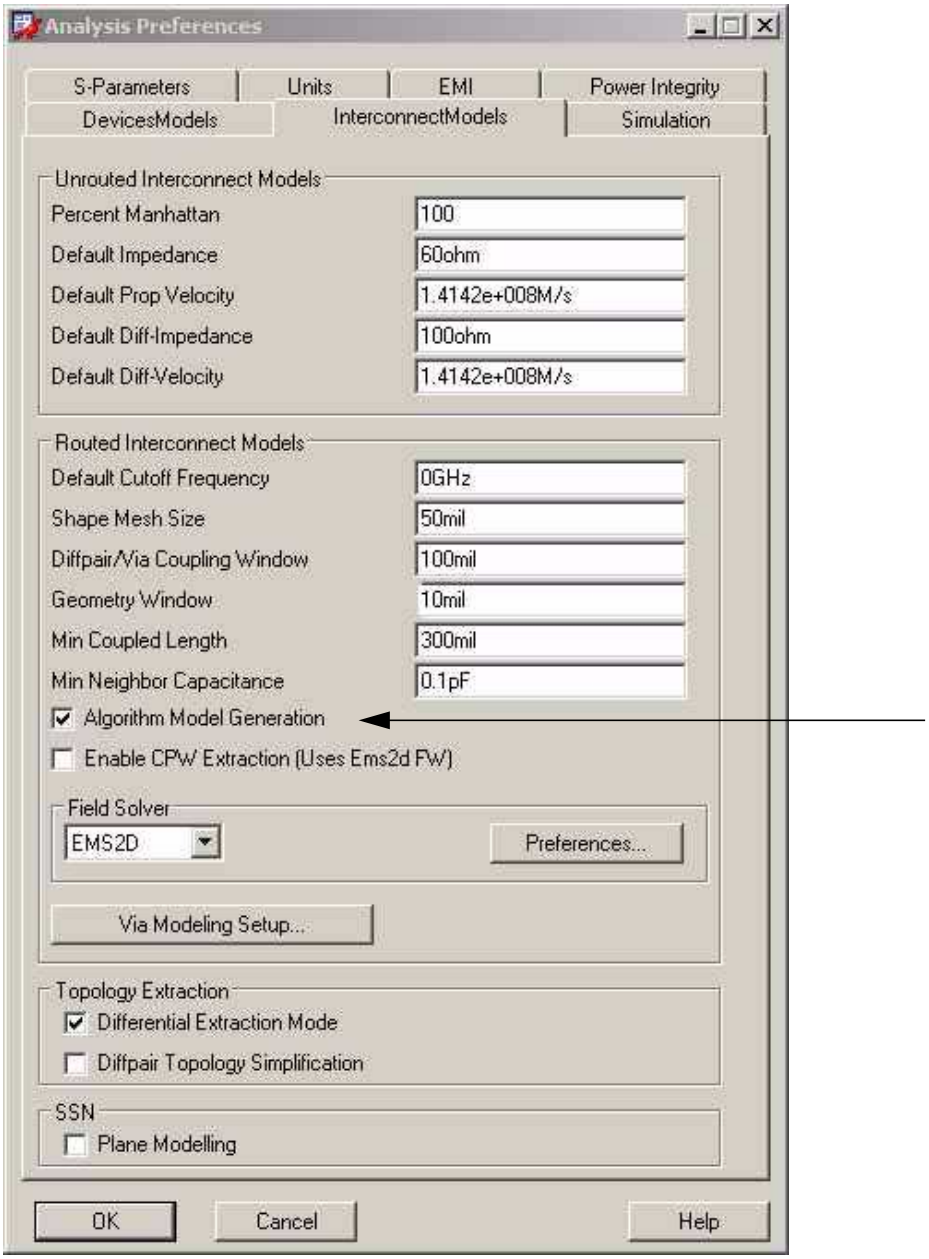


Algorithm-Based Interconnect Modeling

Algorithm-based interconnect models (ABIML) are designed to greatly enhance field solving times when interconnect models do not already exist in the referenced interconnect libraries and, therefore, must be created. Previously, the only method for creation was by calling the field solver. Algorithm model generation lets you create accurate interconnect models off-line that exactly match not only shield, dielectric, trace and physical geometry layer information but also entire frequency spectrums. These models are then integrated into libraries for reuse in multiple simulations.

Algorithm-based modeling is optional. You can enable/disable it from the InterconnectModels tab of the Analysis Preferences dialog box in Allegro PCB SI or the Simulation Parameters tab in SigXplorer. A default set of tables is provided for each interconnect part that can be added to the SigXplorer canvas through the *Edit – Add Part* command.

Figure 5-6 ABIML Control in PCB SI Analysis Preferences



For detailed descriptions of all EMS2D-supported functionality described above, see *"Dynamic Analysis with the EMS2D Full Wave Field Solver"* in the Allegro PCB SI User Guide.

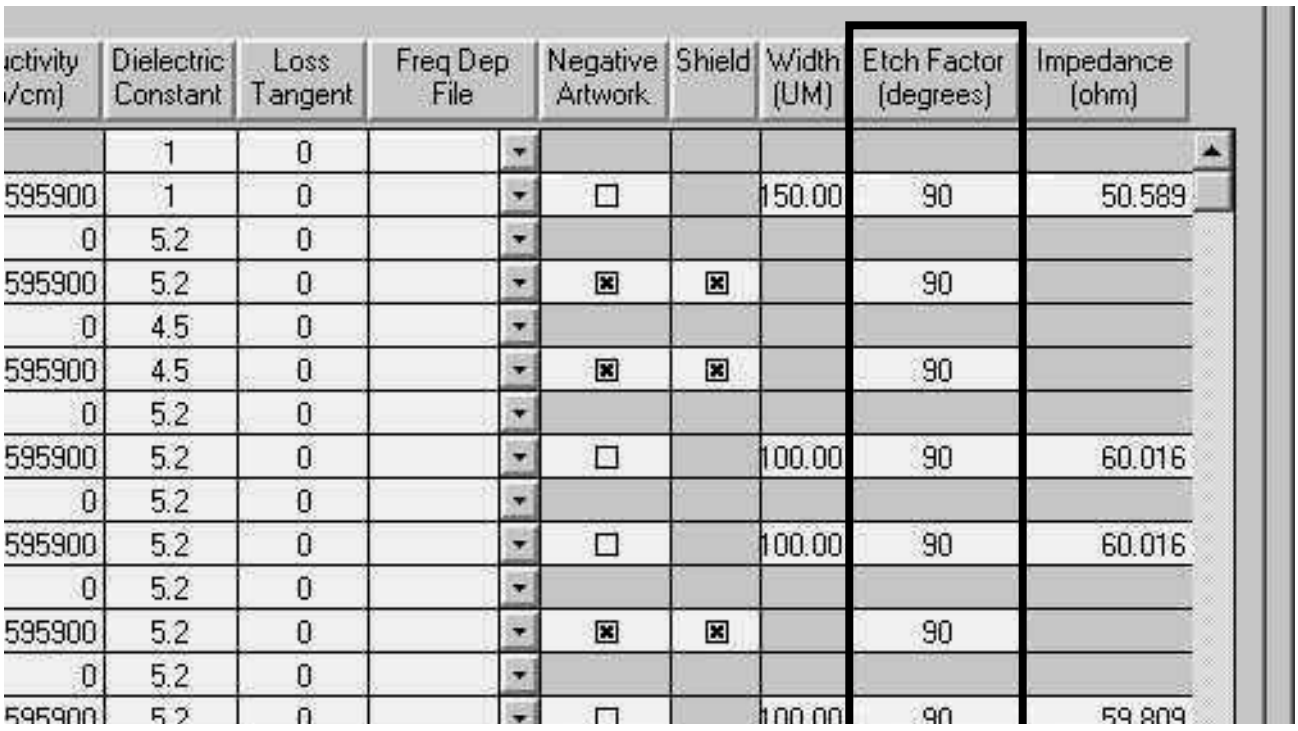
Enhanced Etch Factor Support

This feature is an enhancement of the functionality that allows you to define a trapezoidal cross-section for clines on conductor and plane layers. This functionality differs from the existing *trapezoidal_angle_in_degree* environment variable in the following respects:

- Allows different degree of angle for clines on different layers
- Allows you to set the degree of angle for either the top or the bottom of the cline
- Supports graphical displays that allow you to view where you apply the angle and line width

Additionally, if you specify an etch angle factor for a cline within a CPW structure, EMS2D automatically applies the specified angle value to the bottom edges of the surrounding ground shapes when the angle is something other than 90 degrees. You set etch angles for clines in the Layer Cross Section dialog box (*Setup – Cross-section*).

Figure 5-7 Layer Cross-Section Dialog Box



ctivity /cm)	Dielectric Constant	Loss Tangent	Freq Dep File	Negative Artwork	Shield	Width (UM)	Etch Factor (degrees)	Impedance (ohm)
	1	0						
595900	1	0		☐		150.00	90	50.589
0	5.2	0						
595900	5.2	0		☒	☒		90	
0	4.5	0						
595900	4.5	0		☒	☒		90	
0	5.2	0						
595900	5.2	0		☐		100.00	90	60.016
0	5.2	0						
595900	5.2	0		☐		100.00	90	60.016
0	5.2	0						
595900	5.2	0		☒	☒		90	
0	5.2	0						
595900	5.2	0		☐		100.00	90	59.809

Channel Analysis Developer's Toolkit

A new Channel Analysis Developer's Toolkit containing sample topology files and DML models lets you analyze a real system consisting of advanced SERDES devices and interconnect structures from chip to board to package within the PCB SI and SiP SI environments. The files and an instructional application note is located in your Allegro installation hierarchy at `//share/pcb/channelanalysis/ami/toolkit`.

Note: The Channel Analysis Toolkit is supported on the following platforms: Linux, SUN4, Sol86, IBMRS, and Windows.

ICM Support

Model Integrity now provides complete support for the IBIS interconnect modeling specification and the ability to translate ICM model syntax to ESpice blackbox or PackageModel DML formats for use in simulations.

Non-Native Database Support

For system-level configurations, you can now open in one application designs created in other applications; for example, opening from Allegro PCB SI a `.mcm` design created in APD or a `.sip` design created in SiP. Because designs created in another tool may not contain signal integrity data that your application requires (voltage properties, cross-section data, model assignments, etc.), only limited editing of the non-native drawing is allowed. For additional details, see the associated Help topic.

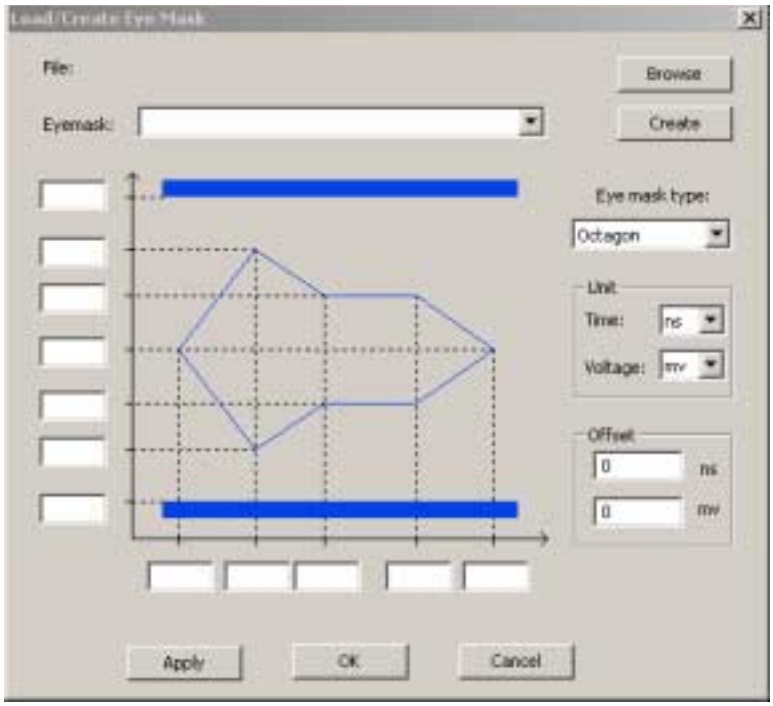
Spectre Upgrade

Release 16.2 upgrades to version MMSIM 7.0.1 of the Cadence Spectre simulator.

Eye Mask and Measurement Enhancements

SigWave now lets you create eye masks that you can save in `.sim` files and view/edit when you display the waveform in Eye Diagram mode. You create a new eye mask or load an existing one into SigWave by way of the Load/Create Eye Mask dialog box. The eye masks you create can be embedded in DML models and used in all standard, bus analysis, and channel analysis simulations. For details on this feature, see *"Using Eye Masks"* in the SigWave User Guide.

Figure 5-8 Load/Create Eye Mask Dialog Box



6

Layout to PCB Editor CCR Fixes in16.2

This chapter lists the CCRs fixed fot Layout to PCB Editor in 16.2.

■ Fixed CCRs on page 92

Fixed CCRs

The following lists the problems reported and fixed in16.2 for Layout to PCB Editor translation. For detailed information about a fixed problem, contact your customer support.

CCR ID	Description
568436 (PCR 4053507)	OrCAD to Allegro translator Package height in symbols
567992 (PCR 2567992)	Free Text are not Translated while doing LtoA
571717 (PCR 2571717)	package_height missing after Layout to Allegro translation
479460 (PCR 2479460)	The L2A translator is misplacing; changing sizes and re-orienting silkscreen text
478898 (PCR 2478898)	Character length limit be increased for padstacks; footprints; vias; netnames
478959 (PCR 2478959)	L2A translator is renaming Layout layer names to something different in Allegro
592499 (PCR 4060849)	Layout to Allegro doesn’t translate free text