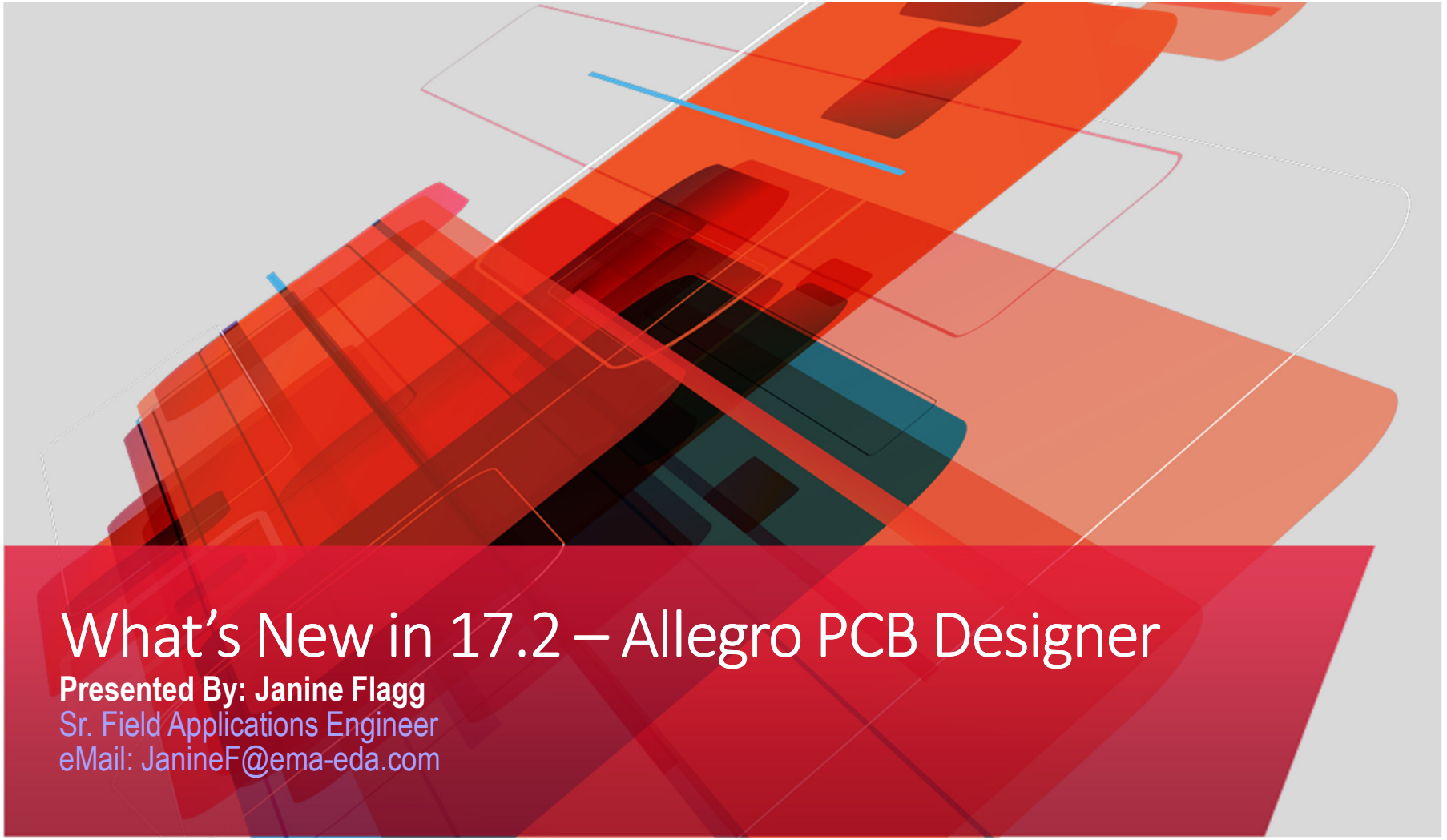

What's New in 17.2 – Allegro PCB Designer

Presented By: Janine Flagg
Sr. Field Applications Engineer
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Migration to SPB17.2
Database and OS

- Allegro database now at 64 bit
- Working memory size increased from 4GB to 18,446,744,073,709,551,616 (18 Quintillion)
- Max database size increases from 400MB to 3GB
- 400 new user subclasses possible with the addition of Rigid-Flex and Surface Classes
- Vista and XP no longer supported
- Supported 64 bit Operating Systems
  - Windows 7,8 &10

17.2 Migration
Database

- **Database Performance Gains**
  - CPU intensive applications, 10 - 20% with 64 bit architecture
  - Import logic (netrev) for very large pin count devices (>2k pins)
  - Copy Fanout using via structures
    - Hours to minutes in 1 test using 1.5 million uvias
  - Notable Database Improvements
    - > 20,000 pins on a symbol
    - > 50,000 pins on a net
    - > 20,000 components
    - Quickplace with > 1,000 components
    - Placement with > 5,000 components
    - Drill chart generation with > 1 million drills

17.2 Migration
Database

- **Script Migration**
  - Scripts that depend upon the following User Interfaces will need to be regenerated:
    - Cross section
    - Pad suppression
    - Embedded layer management
    - Padstack Editor
    - Property edit and the DYN_<xxx> properties

- DYN_CLEARANCE_OVERSIZE
- DYN_CLEARANCE_TYPE
- DYN_DELETE_ISLAND
- DYN_DO_NOT_VOID
- DYN_FIXED_THERMAL_WIDTH
- DYN_MIN_THERMAL_CONNS
- DYN_MAX_THERMAL_CONNS
- DYN_OVERSIZE_THERM_WIDTH
- DYN_THERMAL_BEST_FIT
- DYN_THERMAL_CON_TYPE
- DYN_XHATCH_THERM_WIDTH

17.2 Migration
Database

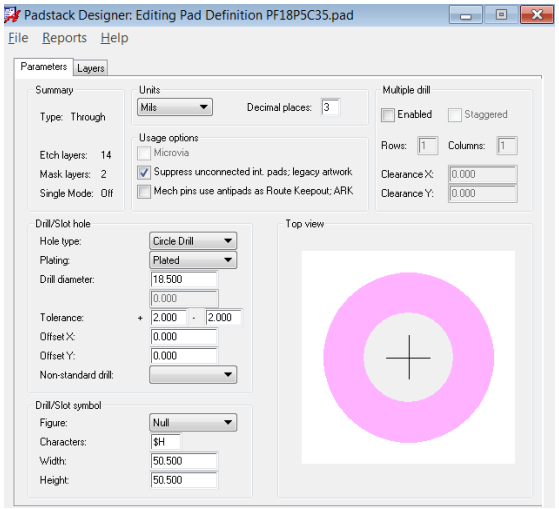
- **Skill**
  - Context Skill files will require recompiling (due to 64 bit)
  - Place them in a sub-directory called 64bit to use them
- **Tech Files**
  - Legacy Technology File (.TECH) will not be compatible with 17.2
  - File > Import > TechFile supports .tcf and .tcfx formats
  - Tech file supports hierarchical layer types (Plane, Conductor, User Defined)
  - Tech File Schema located in share/pcb/consmgr/schemas
- **Downrev**
  - Files saved in 17.0 such as .brd, .mcm, .sip, .pad cannot be downrev'd to 16.x versions
  - Maintaining 16.6 and 17.2 libraries recommended during migration

17.2 Migration
SW Binaries, ENV

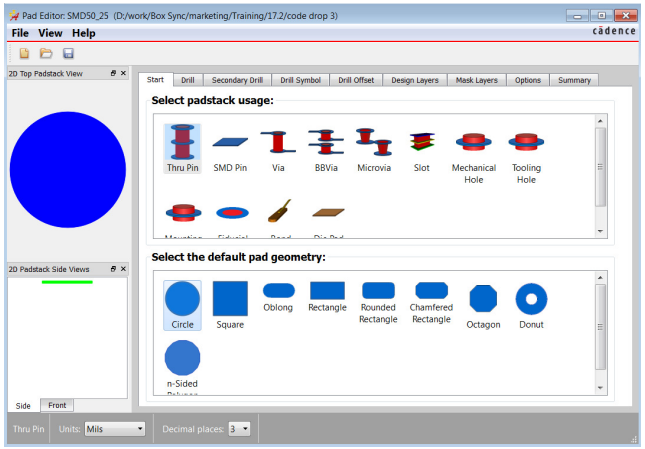
- **Software Binaries**
  - All user-accessible binaries moved to <cdsroot>/tools/bin
  - Should eliminate missing or wrong .dll error messages on Windows
  - Programs renamed and moved to <cdsroot>/tools/bin
    - allegro_uprev, allegro_uprev_overwrite, allegro_cshrc, allegro_profile
- **SPB "switchrelease"**
  - Still required to support older SPB releases and allow resetting file associations
- **allegro_cmd.bat** (tools\bin ; includes instructions)
  - Provided to eliminate SPB from the PATH but still desire to run SPB tools from Windows cmd.exe or PowerShell
- **Net Short**
  - If *Retain Net on Via* option is not selected, *NET_SHORT* property is no longer copied during copy command

17.2 Migration
Padstack Editor

- **Significant upgrades**
  - GUI
  - Several new data fields
- 16.x pads will load into 17.2 databases
- 17.2 pads will **not** load into 16.6 databases
- Maintaining 16.6 and 17.2 libraries is recommended during migration
- Migration considerations
  - New pad primitives including rounded/chamfered rectangular
  - Keepouts built into padstacks
  - Increased user mask layers (16 to 32)



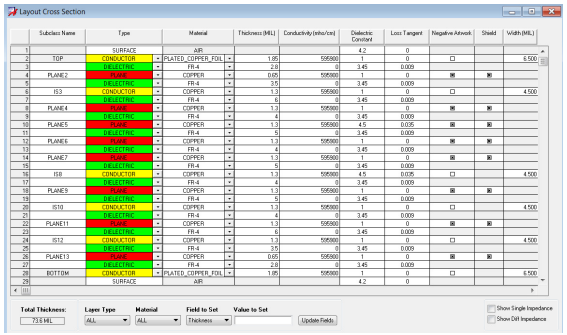
16.6



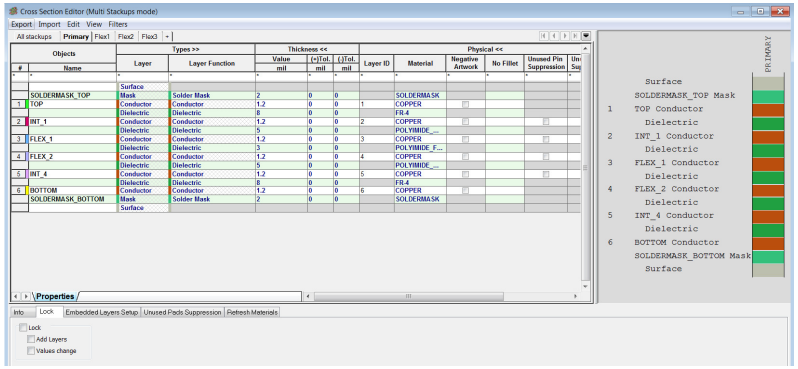
17.2

17.2 Migration
Cross Section Editor

- **Cross Section Editor New Look and Feel**
- Now includes Unused Pad Suppression and Embedded Component Setup
- Non-Conductor layer support
  - Soldermask, Paste, Coverlay
- Material character length increased to 250



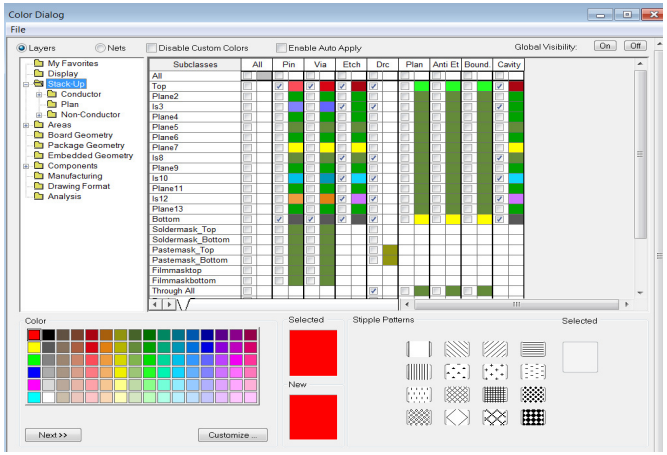
16.6



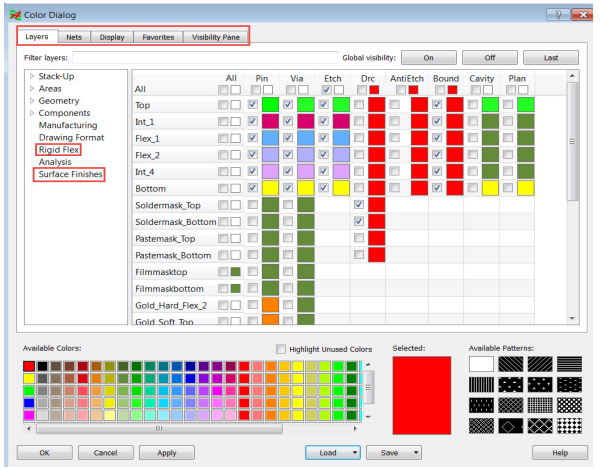
17.2

17.2 Migration
Forms

- **Color Dialog**
  - Tabular based UI
  - Supports new classes “Rigid-Flex” and “Surface Finishes”
  - Control settings for Visibility panel



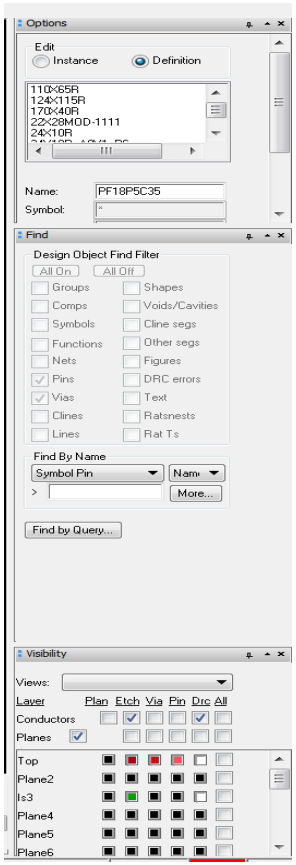
16.6



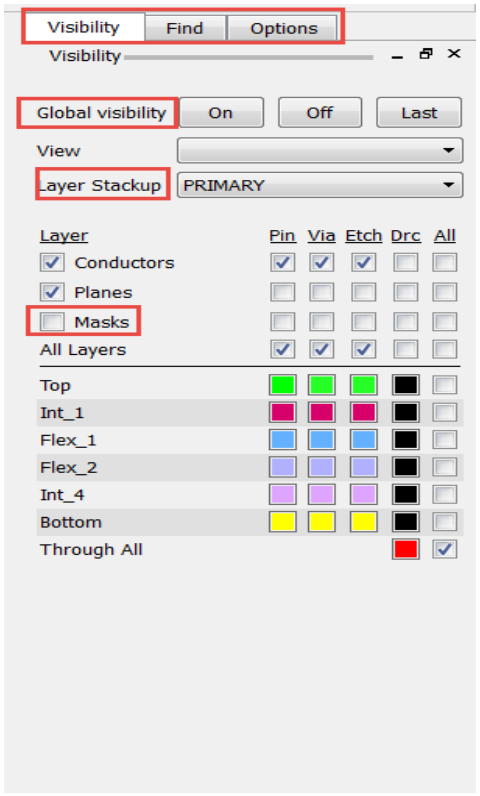
17.2

17.2 Migration
Forms

- **Window Panes/Tabs**
  - More flexible for docking
  - Pre 16.0 horizontal Tab style is now possible
  - Scroll bars now supported
  - New controls in Visibility Panel



16.6



17.2

17.2 Migration
Backdrill

- **Backdrill Overhaul –** Library Impact
  - Backdrill hole size
  - Backdrill figure, char, size
  - Start layer pad
  - Mask Layer pad
  - Anti-pad and KOs

Start | Drill | Secondary Drill | Drill Symbol | Drill Offset | Design Layers | Mask Layers | Options

Select pad to change

Layer Name	Regular Pad	Thermal Pac	Anti Pad	Keep Out
TOP	Circle 56.00	Circle 56.00	Circle 66.00	None
LAYER_2_P	Circle 56.00	Circle 56.00	Circle 66.00	None
LAYER_3	Circle 56.00	Circle 56.00	Circle 66.00	None
LAYER_4_P	Circle 56.00	Circle 56.00	Circle 66.00	None
LAYER_5	Circle 56.00	Circle 56.00	Circle 66.00	None
LAYER_6	Circle 56.00	Circle 56.00	Circle 66.00	None
LAYER_7_P	Circle 56.00	Circle 56.00	Circle 66.00	None
LAYER_8	Circle 56.00	Circle 56.00	Circle 66.00	None
LAYER_9_P	Circle 56.00	Circle 56.00	Circle 66.00	None
DEFAULT INTERNAL	Circle 56.00	Circle 56.00	Circle 66.00	None
BOTTOM	Circle 56.00	Circle 56.00	Circle 66.00	None
ADJACENT LAYER	-	-	-	None
BACKDRILL START	Circle 35.00	-	None	-
BACKDRILL CLEA...	-	-	Circle 70.00	Circle 65.00

Start | Drill | Secondary Drill | Drill Symbol | Drill Offset | Design Layers | Mask Layers | Options

☑ **Backdrill**

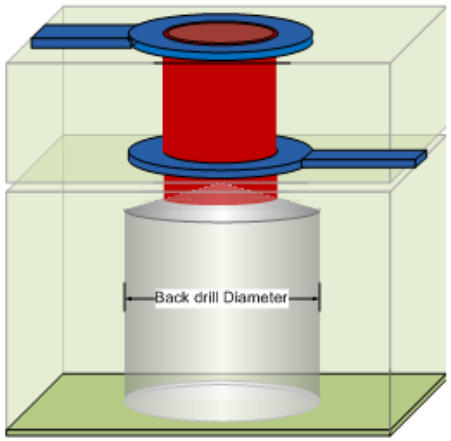
Diameter: 54.00

Backdrill drill symbol

Type of drill figure: Square

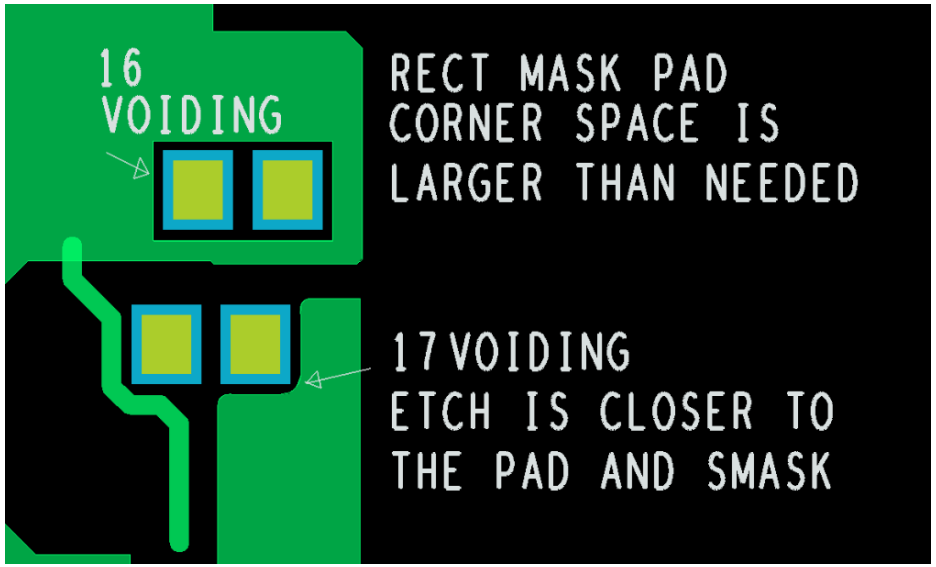
Characters: BD1

Drill figure size: 27.00



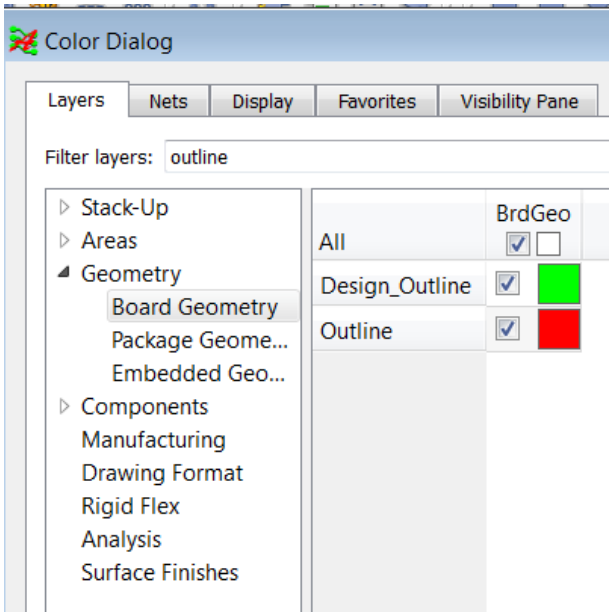
17.2 Migration
Shape Voiding

- **Shape voiding** associated with rectangular pads
  - More consistent in maintaining minimum DRC clearance to the pad boundary
- Noticeable difference with corners
  - Now rounded



17.2 Migration
New Design Outline

- **Replaces legacy “Outline”**
- Contiguous, shape based outline
- Upreved 16.6 databases will have largest board geometry outline converted to shape on new "Design Outline" layer.
  - Smaller shapes within design outline are converted to shapes on new "Cutout" layer.
  - No objects on the Board Geometry layer will be deleted as part of migration process
- Outlines with smaller objects contained within will be converted to new “Cutout” subclass

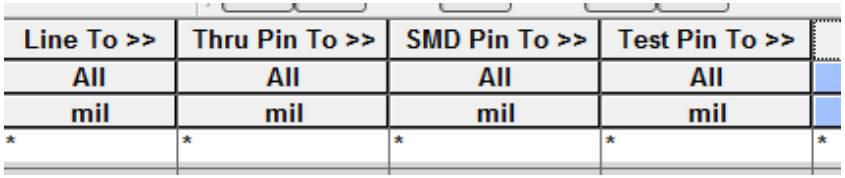


17.2 Migration
New Design Outline

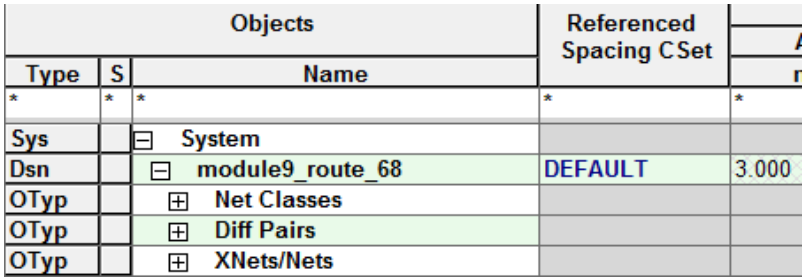
- **Necessary to support:**
  - New design rule checks
  - Cross section by zone
  - Inlay material sections
- Multiple Design Outlines not supported
- Legacy Board Geometry Outline retained in Database
- IDF/IDX-In will write to new Design Outline & Cutout subclasses
- IDX-Out and IPC-2581 will fail if no Design Outline is present
- Create Artwork will provide “warnings” if legacy outline is used in film records

17.2 Migration
Constraint Manager

- **Worksheet Data Compression**
  - Worksheet column headers are collapsed by default and can be expanded by double clicking the double arrows
  - Net worksheets upon invocation default to Hierarchical objects which can be expanded to net level members



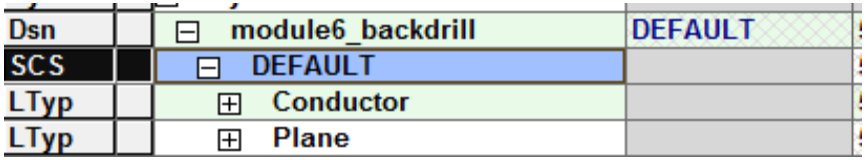
Line To >>	Thru Pin To >>	SMD Pin To >>	Test Pin To >>	
All	All	All	All	
mil	mil	mil	mil	
*	*	*	*	*

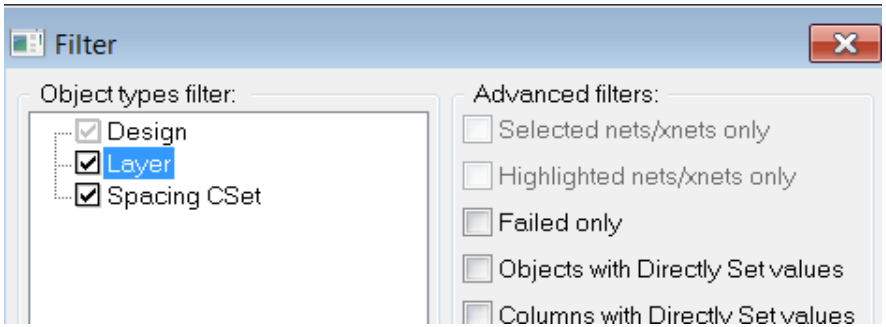


Objects			Referenced Spacing CSet	
Type	S	Name		
*	*	*	*	*
Sys		⊟ System		
Dsn		⊟ module9_route_68	DEFAULT	3.000
OTyp		⊞ Net Classes		
OTyp		⊞ Diff Pairs		
OTyp		⊞ XNets/Nets		

17.2 Migration
Constraint Manager

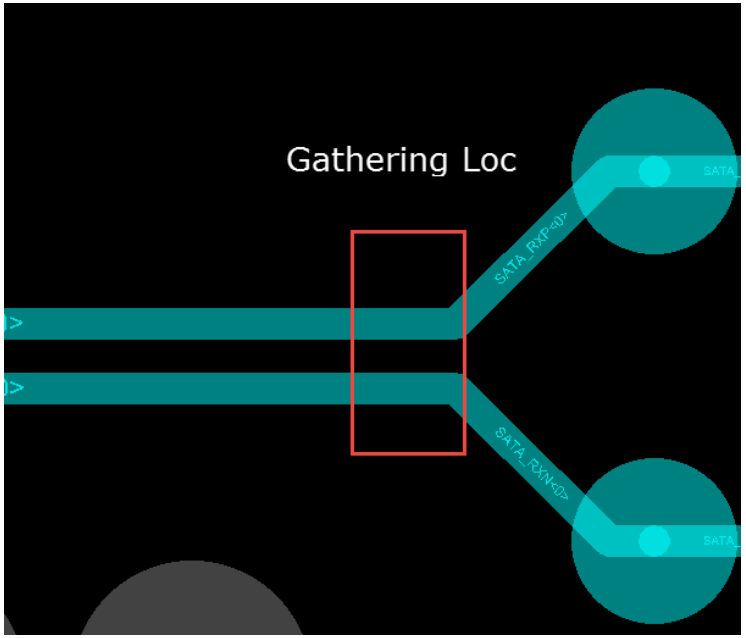
- **Worksheet Data Compression**
  - Constraint Sets grouped by Hierarchical names
    - Conductor
    - Planes
  - Setting to revert back to legacy view (Filter – Layer)





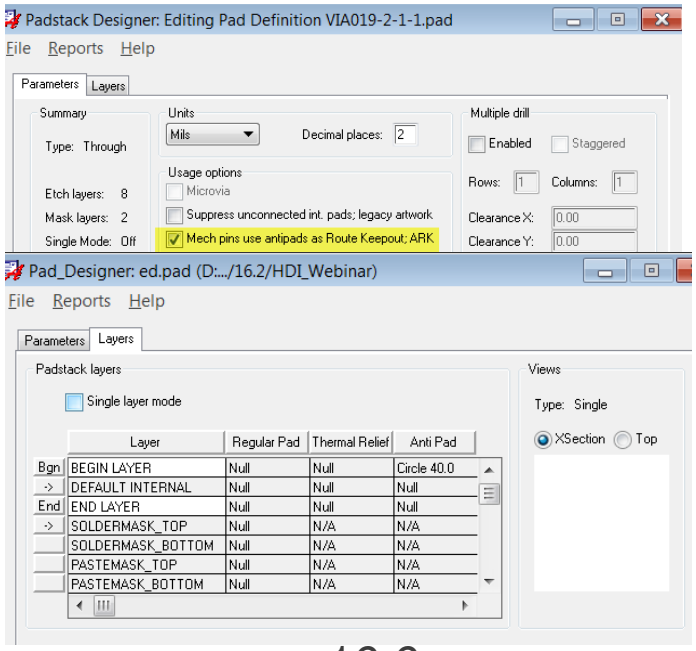
17.2 Migration
Differential Pair DRC

- **Dynamic Phase**
  - Dynamic Phase DRC
    - Now checks back to driver pins
    - Formerly the gathering location
  - Changes to the Differential Pair Dynamic Phase DRC algorithm may introduce DRCs after uprev
  - Set legacy_diffpair_checks variable to maintain the pre 17.x DRC state for Differential Pairs



17.2 Migration
Eliminated

- The “ARK” padstack option (mechanical pins use anti-pad as keepout)
- If pads were saved with the “ARK” option in 16.6, their anti-pad value will transfer to the “Keepout” field in 17.2



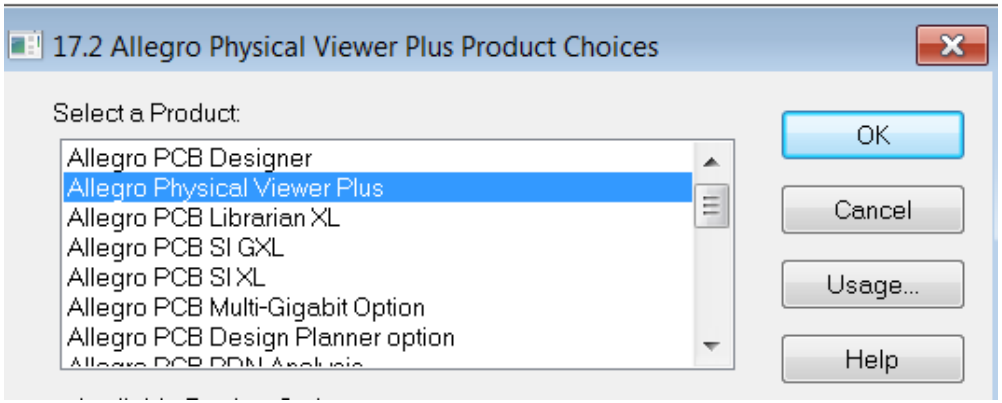
16.6

Layer Name	Regular Pad	Thermal Pad	Anti Pad	Keep Out
BEGIN LAYER	None	None	Circle 40.0	Circle 40.0
ADJACENT LAYER	-	-	-	None

17.2

17.2 Migration
Products

- Allegro Viewer Plus now accessible from Product Choices



Overhaul of Padstack Editor

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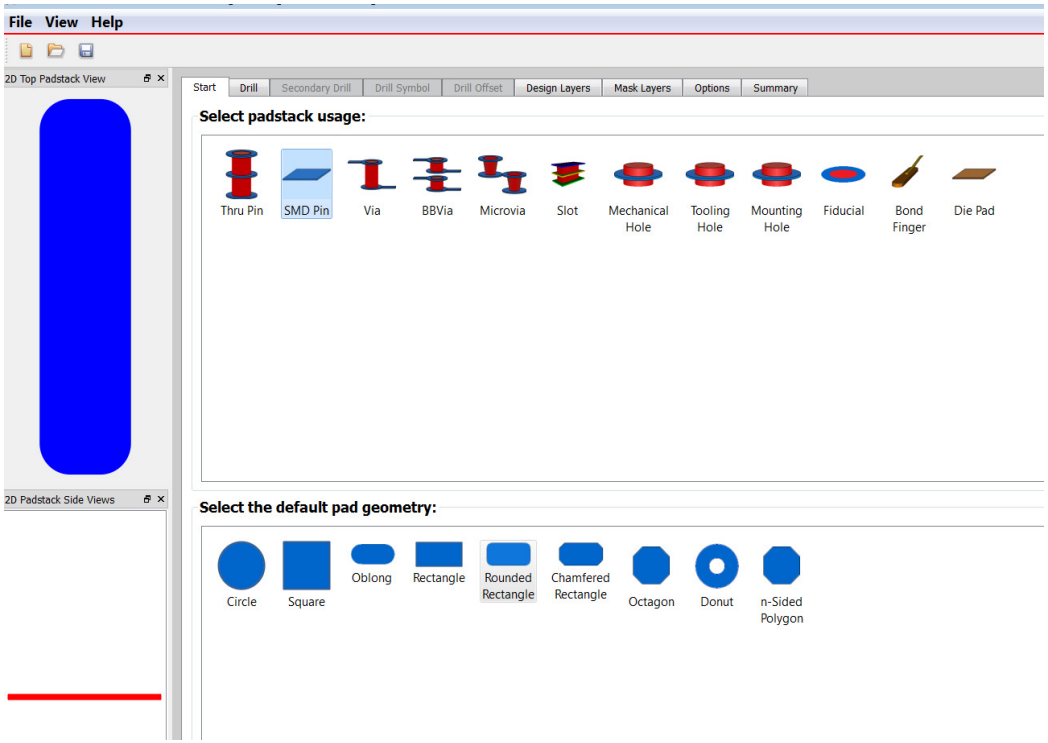
New Graphical User Interface

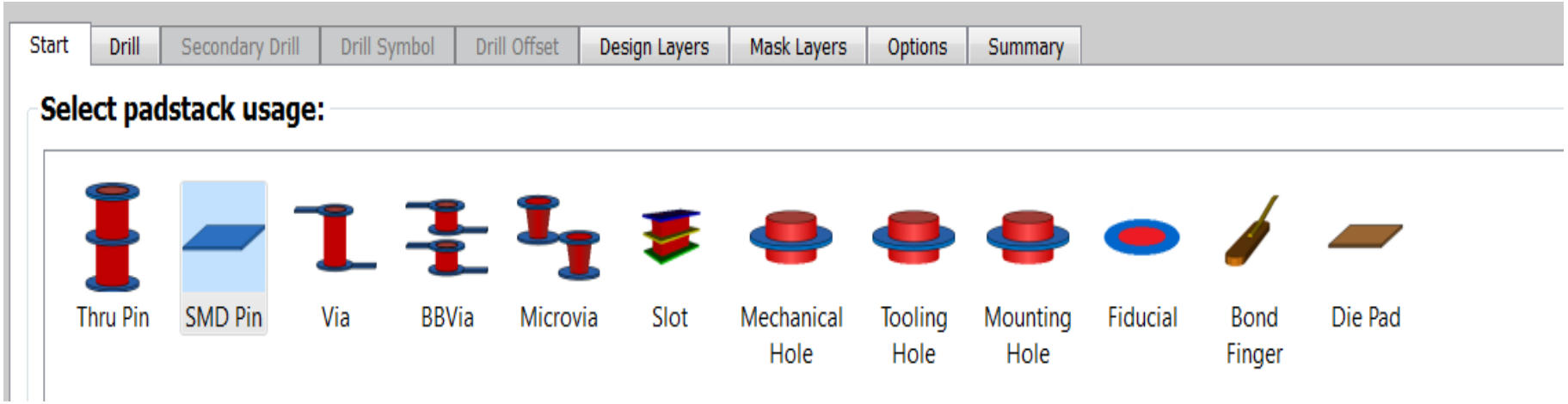
- Modern, easier to use interface
  - Improved graphics/bitmaps
  - Sizable docking views/forms
- Supports flow driven Pad creation
  - Thru
  - SMD
- Integration to supporting editors
  - Shape Symbol
  - Flash Symbol
- Scripting Supported
  - 16.x scripts not compatible



New Padstack “Usage” Types

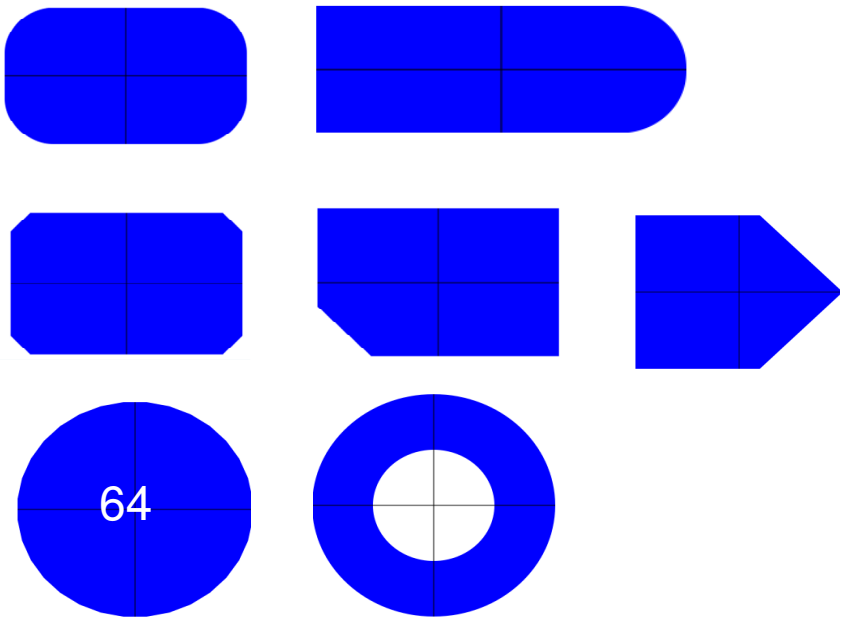
- Bond Finger
- Die Pad
- Tooling Hole *
- Mounting Hole *
- Fiducial *

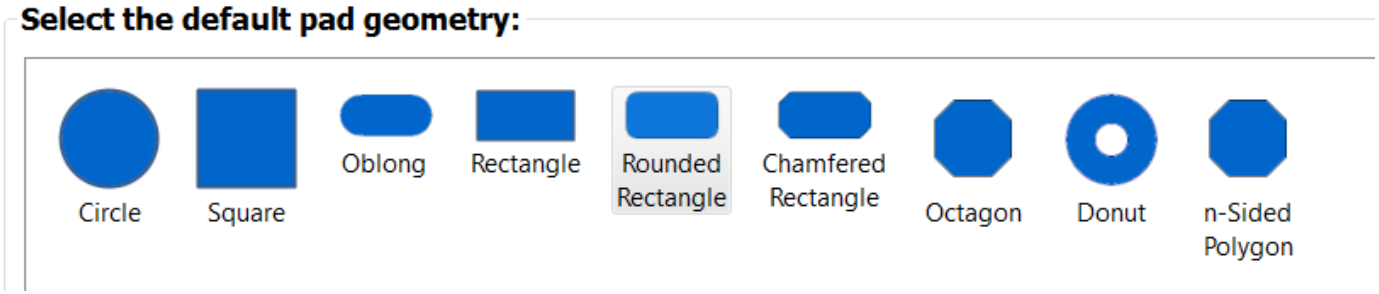
* *Alignment with IPC 2581 schema*



New Padstack Geometries

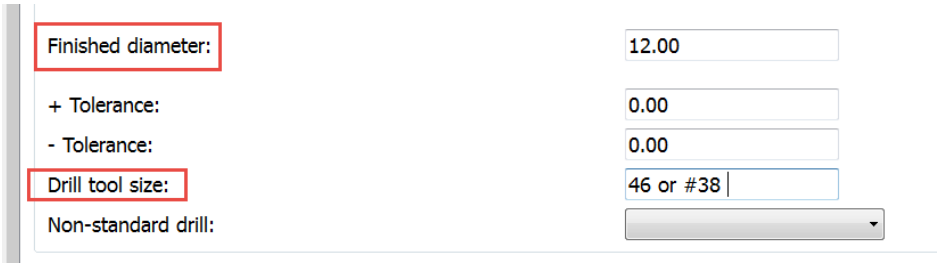
- Rounded Rectangle
- Chamfered Rectangle
- Multisided Polygon
  - 8 to 64 sides (even only)
- Donut Pad

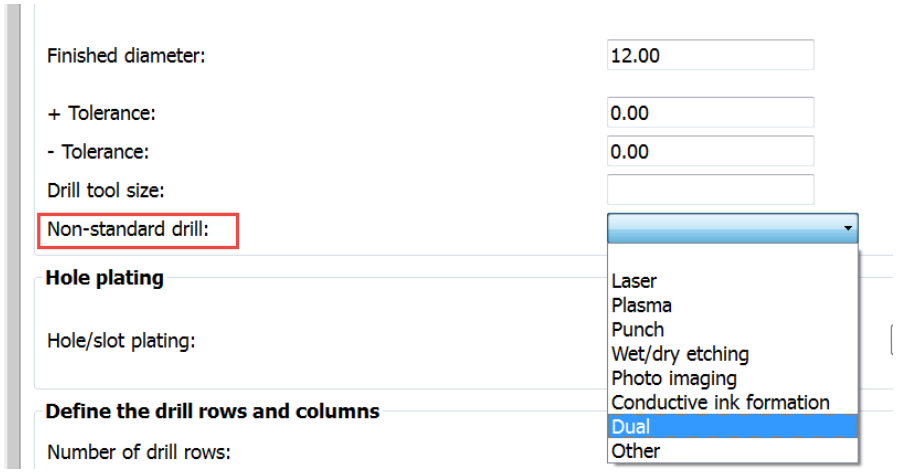




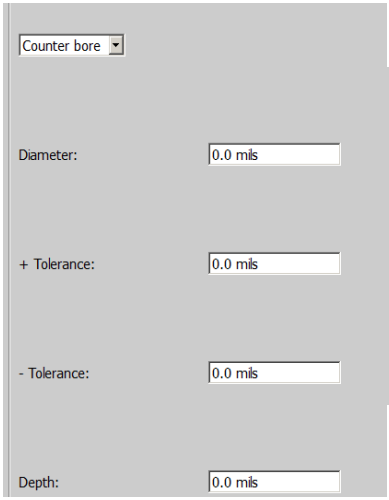
Drill Definition

- Finished Drill Hole
  - Hole diameter after plating
  - 16.x data migrates to this field
- Hole Type options
  - Circle
  - Square (New)
- Drill Tool Size (New)
  - Drill size used before plating
  - Reference data output to NC Legend
  - Typically used with Connectors
  - Exports to IPC-2581
- New “Dual” Drill Attribute
  - Use for Co-Ax or Dual-Drill applications

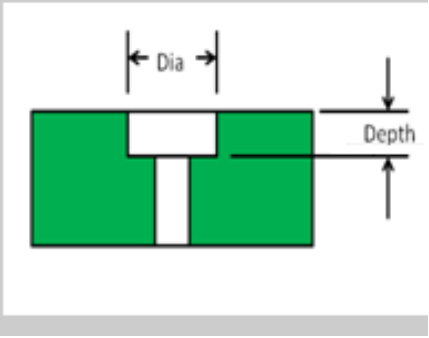




Counterbore and Countersink Drill Types

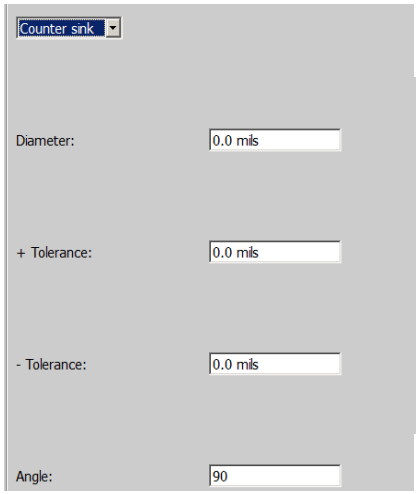


Counterbore

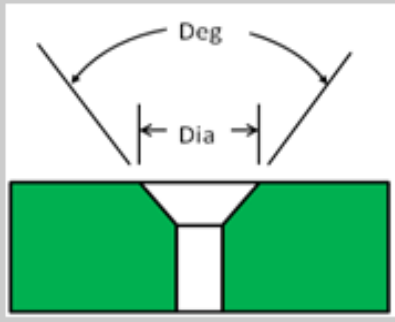


COUNTERBORE/COUNTERSINK: TOP					
ALL UNITS ARE IN MILS					
FIGURE	DIAMETER	TOLERANCE	ANGLE	DEPTH	QTY
⌀	130.0	+3.0/-2.0	0.000	40.0	4

DRILL CHART: TOP to BOTTOM						
ALL UNITS ARE IN MILS						
FIGURE	FINISHED_SIZE	ROTATION	TOLERANCE_DRILL	PLATED	NONSTANDARD	QTY
▲	10.0	-	+0.0/-0.0	PLATED		26
◇	30.0	-	+0.0/-0.0	PLATED		18
○	55.0	-	+0.0/-0.0	PLATED		16
	60.0	0.000	+0.0/-0.0	PLATED	SQ-	16
⌀	118.0	-	+0.0/-0.0	PLATED		4
□	40.0	-	+0.0/-0.0	NON-PLATED		4
I	125.0	-	+0.0/-0.0	NON-PLATED		2
	250.0	-	+0.0/-0.0	NON-PLATED		2
⌯	109.0x50.0	0.000	+2.0/-2.0	NON-PLATED		2
◊	109.0x50.0	90.000	+2.0/-2.0	NON-PLATED		2

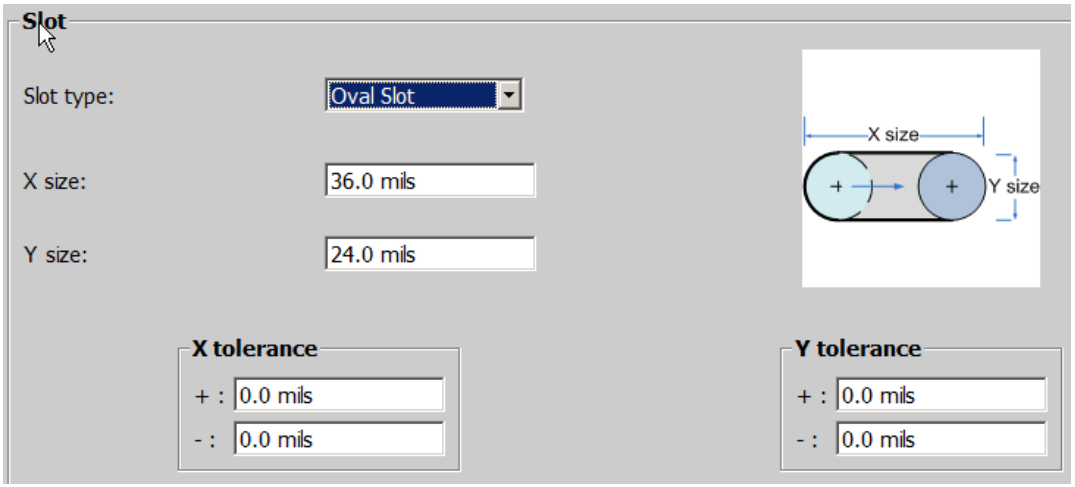


Countersink



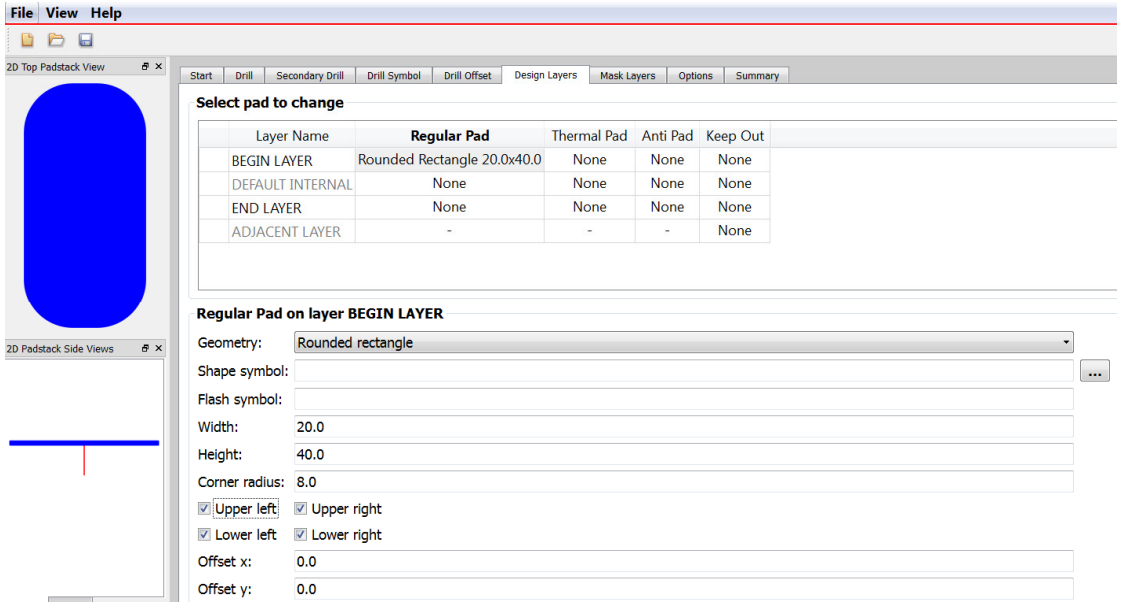
Slot Enhancement

- Tolerance expanded to cover length and width
- Currently only one set of +/-tolerances is supported for both directions
- Length is typically the larger tolerance



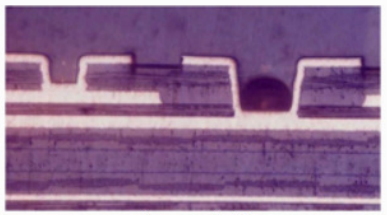
Design Layer Entry

- Design Layers Tab contains pad data on conductive layers
  - Begin, End, Internal
  - Regular Pad, Thermal and Anti Pad
  - New Keepout Pad
- Launch supporting tools
  - Shape Symbol Editor
  - Flash Symbol Editor



Route Keepout Support in Padstack

- Route KO areas can be defined in the Pad Definition or Instance
  - Previously limited to Mechanical Pins only using (ARK) pad option
- Skip via requires KO on middle layer



Skip-via hole

Select Pad To Change

Layer Name	Regular Pad	Thermal Pad	Anti Pad	Keep Out
BEGIN LAYER	Circle 16.000	Circle 0.000	Circle 21.000	None
IN2	None	None	None	Circle 21.000
GND1	Circle 16.000	Circle 0.000	Circle 21.000	None
IN4	None	None	None	None
GND2	None	None	None	None
IN6	None	None	None	None
IN7	None	None	None	None
DEFAULT INTERNAL	None	Circle 0.000	None	None
END LAYER	None	None	None	None
ADJACENT LAYER	-	-	-	None

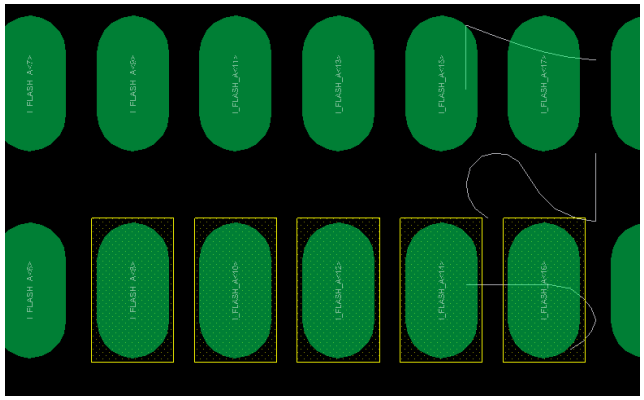
Adjacent Layer Route Keepout

- Define keepout requirements beyond begin/end layers of the pad definition
- Define geometry in Pad Editor
- Define layer range in PCB Editor via properties
  - *Adjacent_layer_keepout_above*
  - *Adjacent_layer_keepout_below*
  - Applied to consecutive layer spans only; max 8 layers
- Examples
  - Adjacent Layer(s) under SMD Pins
  - BB Vias (adjacent layers above & below)
    - Overshoot of drilling to layer beyond target can result in short if area not void of metal
  - Fiducials

Start | Drill | Secondary Drill | Drill Symbol | Drill Offset | Design Layers | Mask Layers | Options

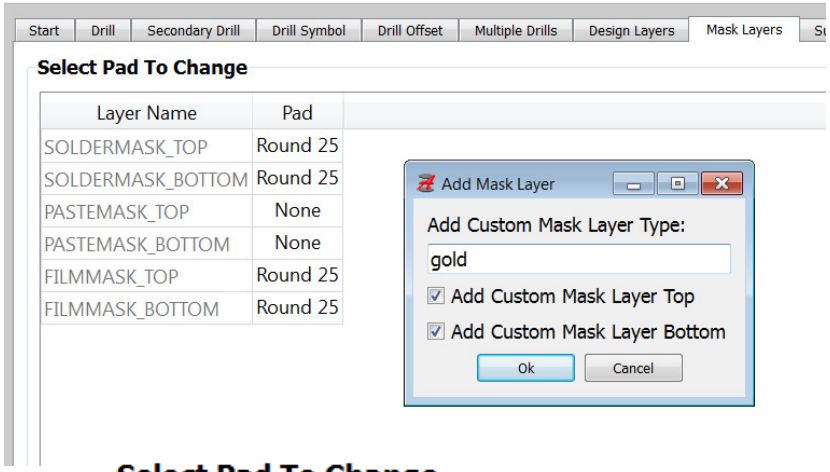
Select Pad To Change

Layer Name	Regular Pad	Thermal Pad	Anti Pad	Keep Out
BEGIN LAYER	Circle 6.000	Circle 14.000	Circle 14.000	None
IN2	Circle 6.000	Circle 14.000	Circle 14.000	None
GND1	None	None	None	None
IN4	None	None	None	None
GND2	None	None	None	None
IN6	None	None	None	None
IN7	None	None	None	None
DEFAULT INTERNAL	Circle 9.843	Circle 9.843	Circle 9.843	None
END LAYER	None	None	None	None
ADJACENT LAYER	-	-	-	Square 10.000



Mask Layer Entry

- Mask Layers Tab is used to enter all mask data
  - Soldermask, Pastemask, User Defined Mask
- New user interface to add mask “root” names
  - i.e. gold
- Options to add Top/Bottom extensions
- User Mask layers increased from 16 to 32



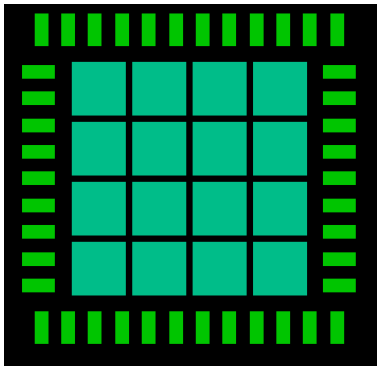
Select Pad To Change

Layer Name	Pad
SOLDERMASK_TOP	Round 25
SOLDERMASK_BOTTOM	Round 25
PASTEMASK_TOP	None
PASTEMASK_BOTTOM	None
FILMMASK_TOP	Round 25
FILMMASK_BOTTOM	Round 25
GOLD_TOP	Round 25
GOLD_BOTTOM	Round 25

Segmented Mask Schemes

- Pad definition with multiple shapes/voids entries
- Create “window pane” mask configurations to reduce solder deposition on large pads
- Mask pads can either be .ssm or .fsm types
  - Flash symbol (.fsm) supports multiple elements

Printing solder paste 1-1 on large pads can cause device to float during reflow. Device floating can be controlled by reducing the amount of solder paste .



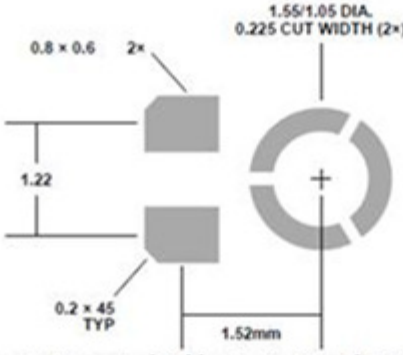
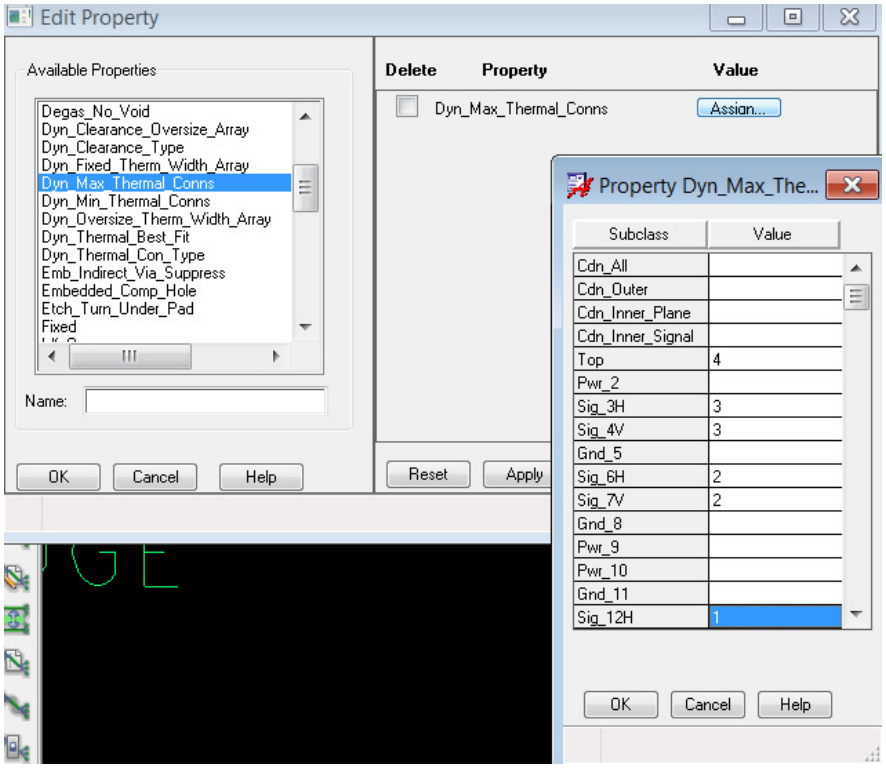


Figure 7. Suggested Solder Paste Stencil Pattern Layout

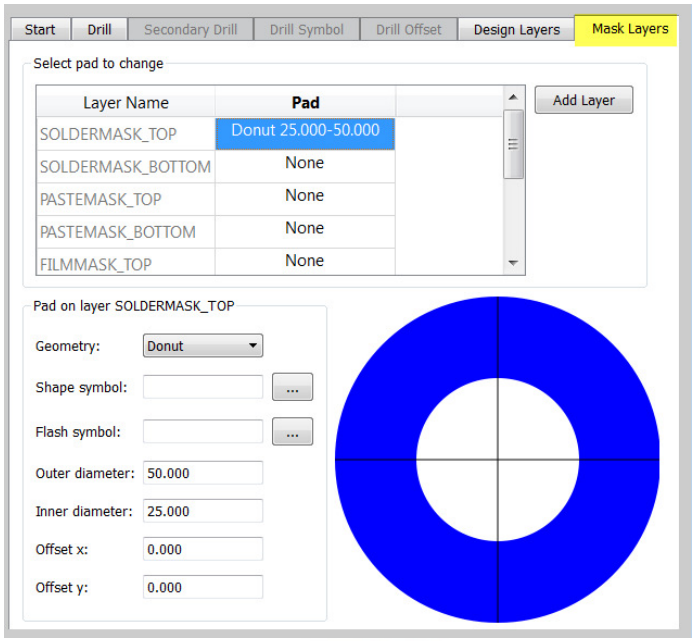
Thermal/Voiding controls by layer

- Dynamic shape properties that control thermal generation and clearance can now be applied BY LAYER!
- Formally applied at the Global or Shape Instance level
- Beneficial in controlling max metal making contact with pins



Productivity Enhancement
QIR5 Addition

- Padstack Editor
  - Donut pads now supported on mask layers
    - Application: Solder Dam to reduce solder flowing towards the center of the pad/hole
  - Copy/paste across domains (Design to Mask)
  - Issues related to auto-scrolling addressed



Overhaul of Cross Section Editor

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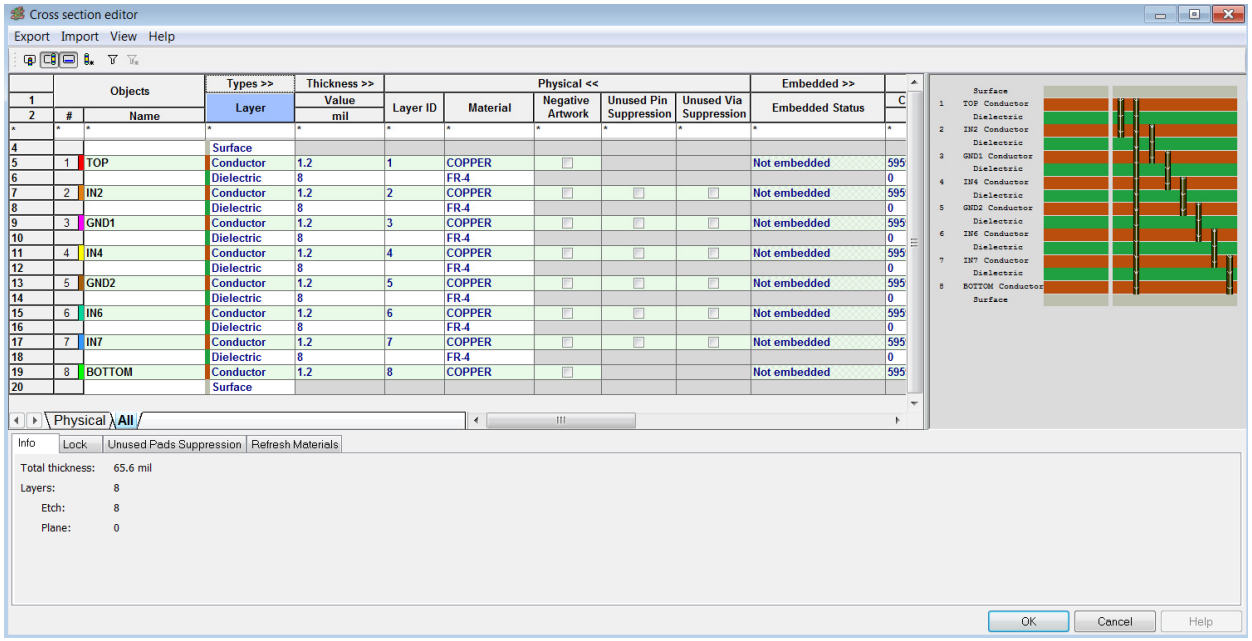
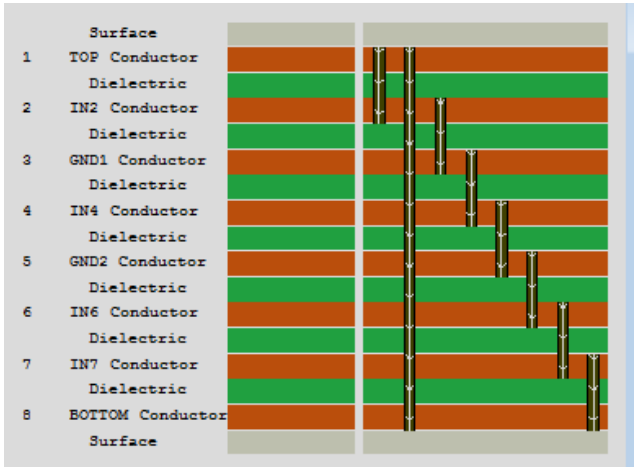
Cross Section Editor

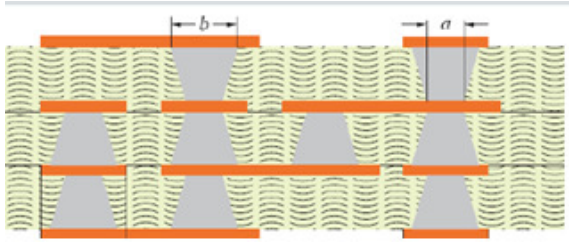
- Familiar Constraint Manager look and feel
- Columns may be expanded or compressed to minimize data on screen
- Multiple Board Stackup Definition
- Non-Conductor Layer support (mask, coatings, stiffeners)



Cross Section Editor

- Graphical display of layers & attributes
- Display of drill direction (reversible)
- Material thickness: +/- tolerance
- “No Fillet” on/off control by Layer
  - Set ON to disable





Thickness			Layer ID	Material	Ne A
Value	(+)Tol.	(-)Tol.			
mm	mm	mm			
*	*	*	*	*	*
0.03048	0.0002	0.0001	1	COPPER	
0.2032	0.0002	0.0001		FR-4	
0.03048	0.0002	0.0001	2	COPPER	
0.2032	0.0002	0.0001		FR-4	
0.03048	0.0002	0.0001	3	COPPER	

Thickness Tolerance

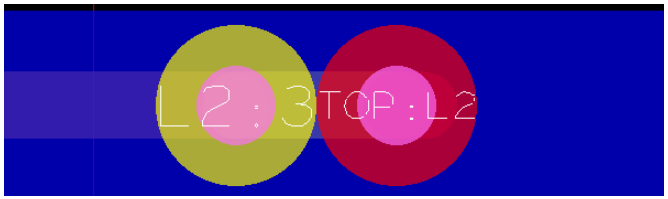
Physical <<						
Layer ID	Material	Negative Artwork	No Fillet	Unused Pin Suppression	Unused Via Suppression	
*	*	*	*	*	*	*
1	COPPER	☐				Not
	FR-4					
2	COPPER	☐	On	☑	☑	Not
	FR-4					
3	COPPER	☐		☑	☑	Not
	FR-4					
4	COPPER	☐		☑	☑	Not
	FR-4					
5	COPPER	☐		☑	☑	Not
	FR-4					

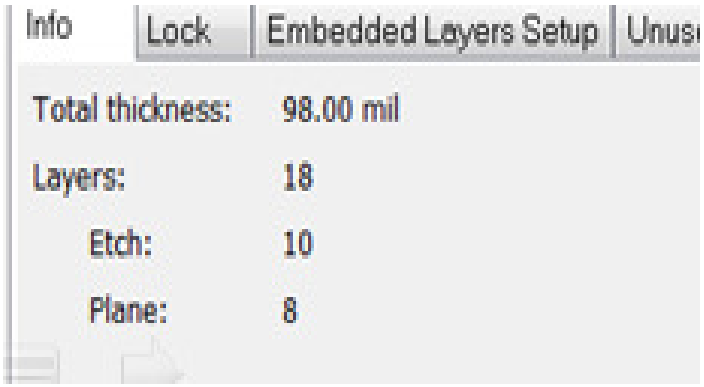
No Fillet by Layer

Cross Section Editor

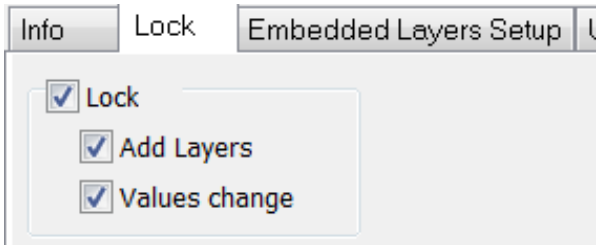
- Custom layer ID's to control microvia labels
  - 3 alpha-numeric character limit
- Material names
  - Increase character length
  - 19 to 250 characters
- Info and Lock functions

Thickness <<				
Value mil	(+)Tol. mil	(-)Tol. mil	Layer ID	Material
	*	*	*	*
	0	0	TOP	COPPER
	0	0		FR-4
	0	0	L2	COPPER
	0	0		FR-4
	0	0	3	COPPER
	0	0		FR-4

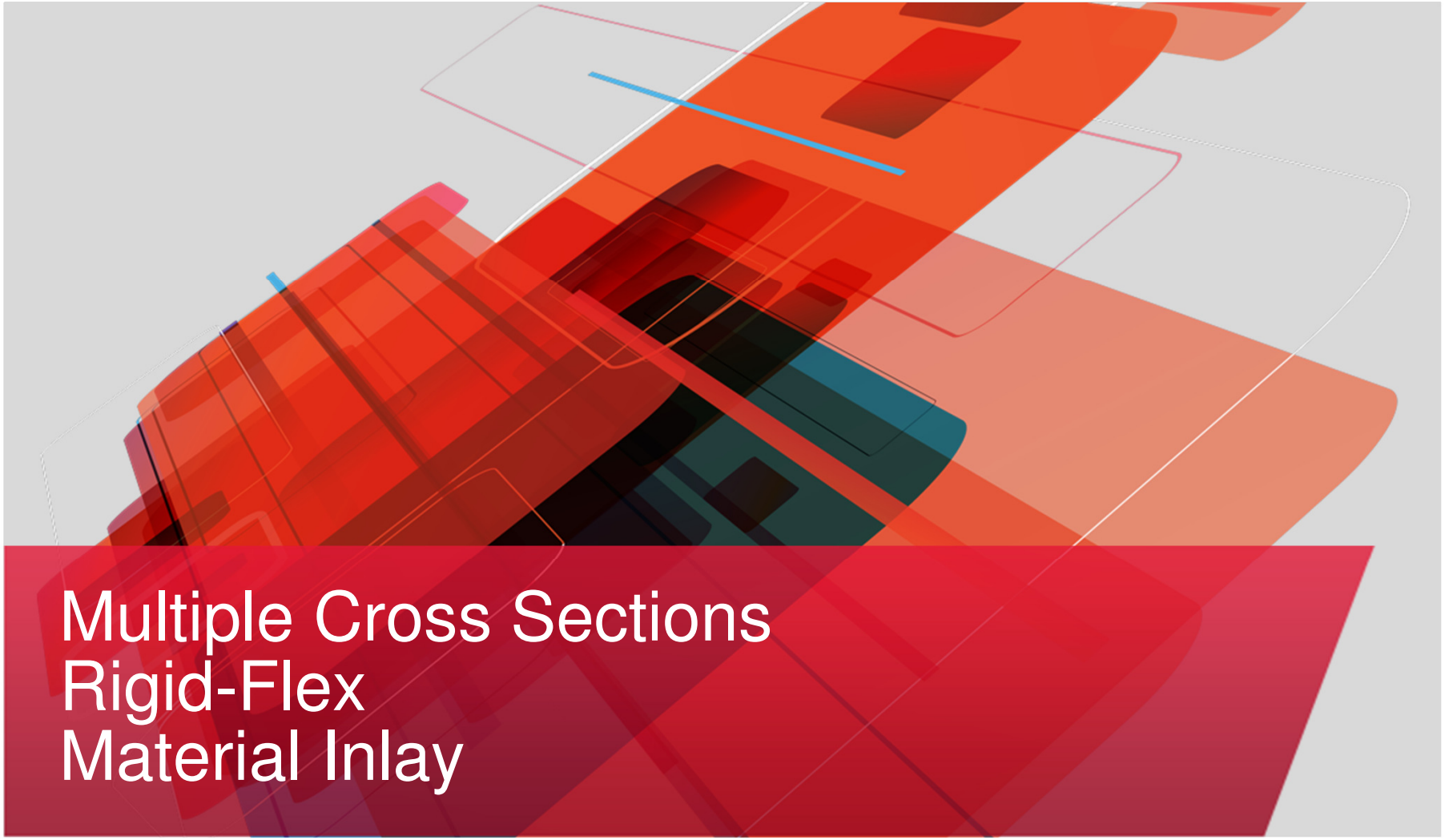




Total Layer Count



Safeguard against adding layers or changing values



Multiple Cross Sections
Rigid-Flex
Material Inlay

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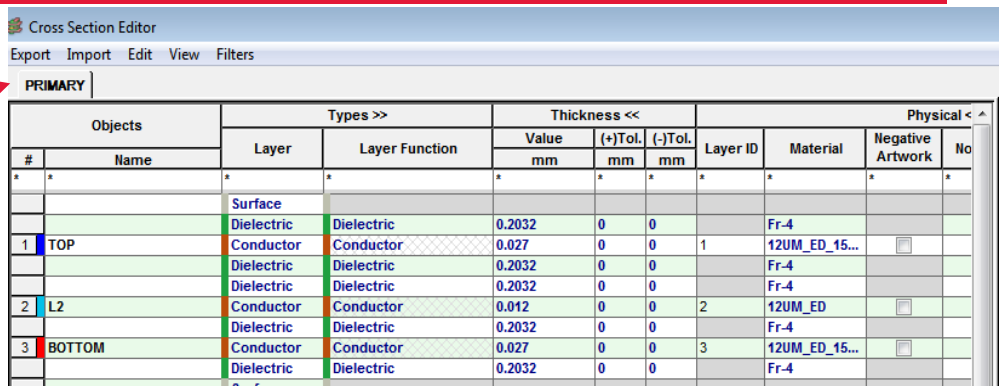
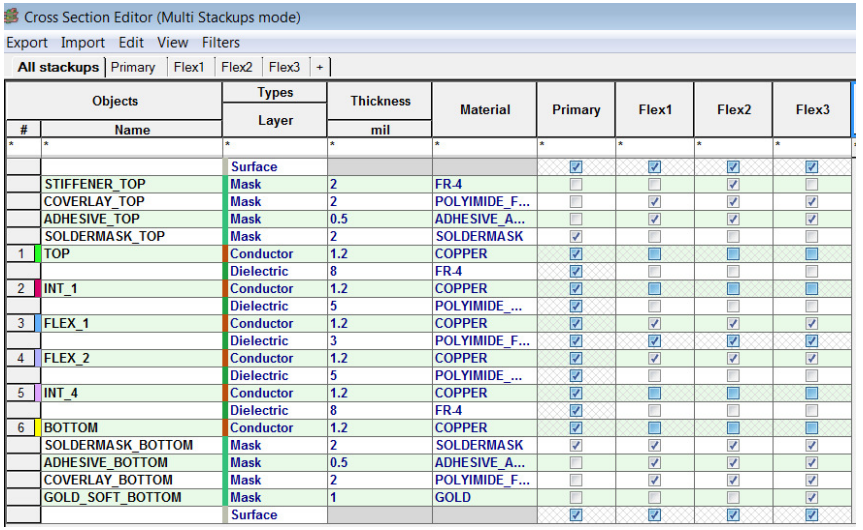
Multiple Cross Sections

- Default Mode
  - "**Primary**" TAB represents single stackup for design
- Multi Stackups Mode
  - "All Stackups" Tab: all possible layers (conductor and mask)
  - "Primary" represents base stackup
    - Typically no zone associated
  - "Flex" in this example is a deviation from Primary
    - Physical Zone required
    - Configure boxes to align with the appropriate layers in the Objects column



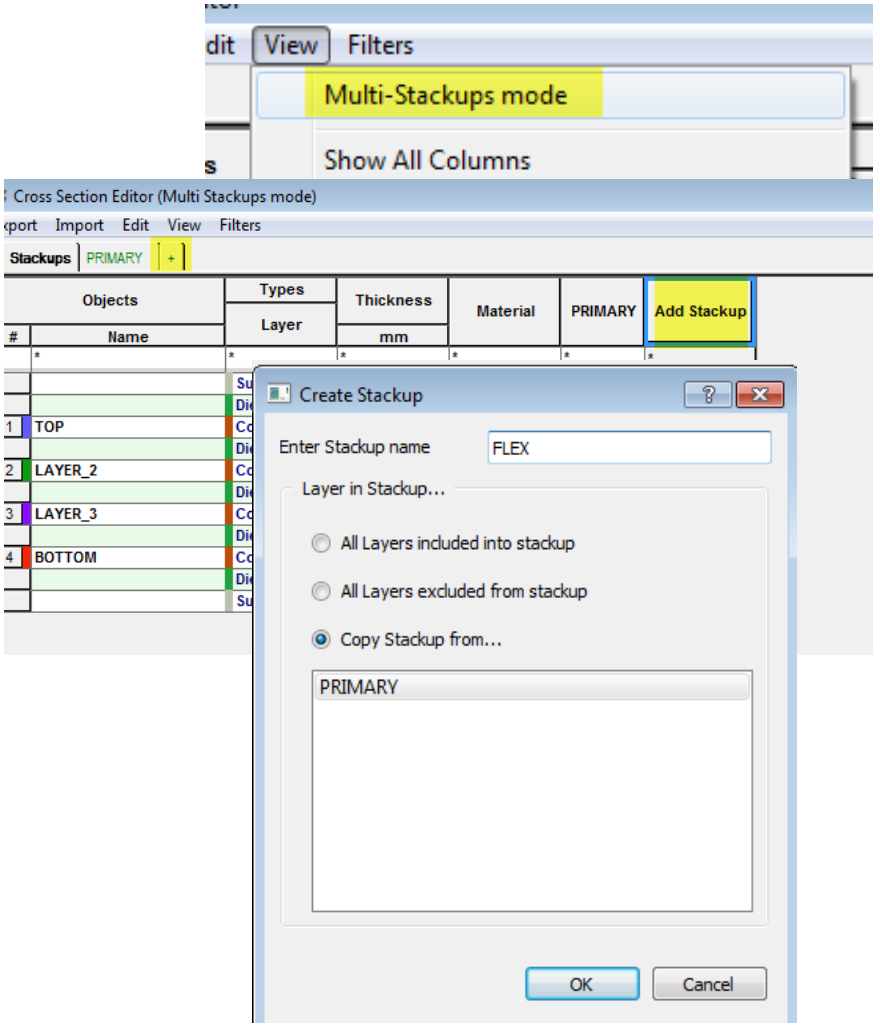
Default mode



Multi-stackup mode

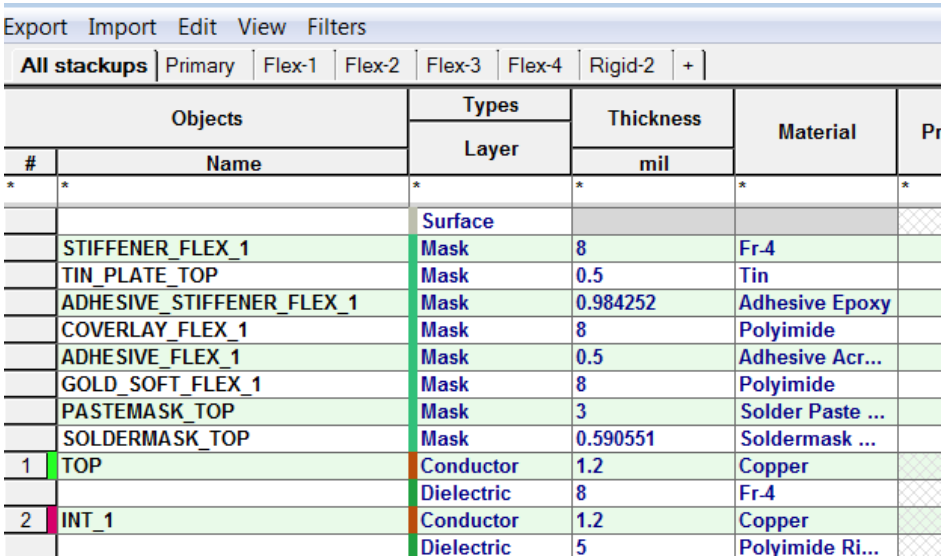
Multiple Cross Sections

- Process Steps
  - Enable View - Multi-Stackup mode
  - Add new stackups by clicking the “+” sign or the “Add stackup” column header
  - Name the stackup as appropriate; otherwise it defaults to stackup1, stackup2, etc.
  - Leverage the “Copy Stackup from” option when adding new stackups to save steps



Cross Section
Non-Conductor Layers

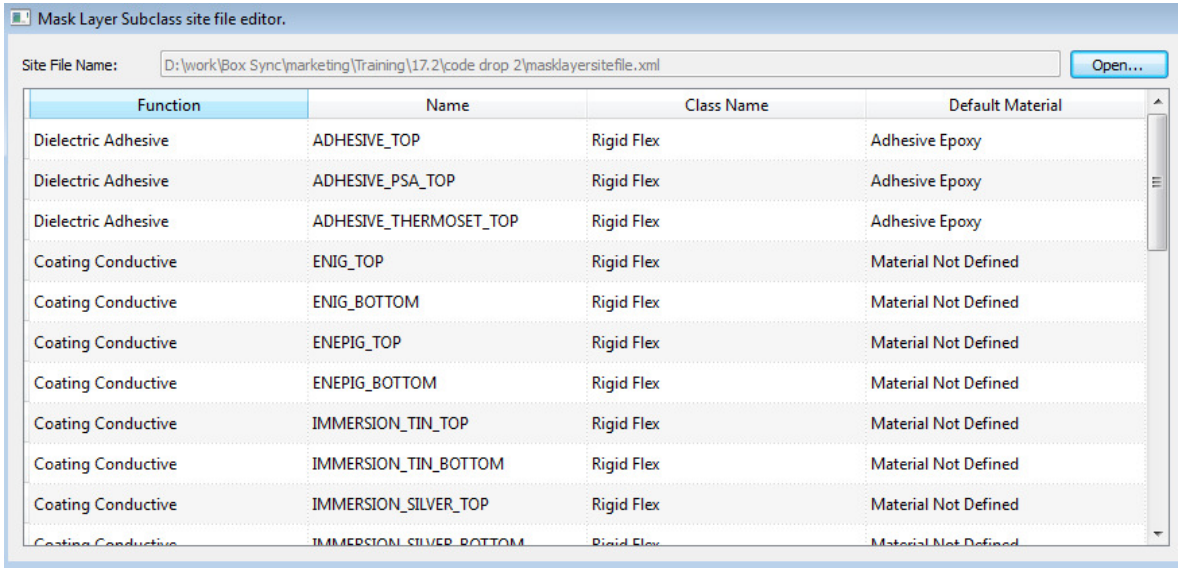
- Cross Section now supports Conductor, Dielectric and Mask layers
- Layer Type “Mask” is a hard coded attribute for all mask/coating/shielding layers above the surfaces
- Click “All Stackups” Tab to enter all possible layers across the multi fabrics



Objects		Types	Thickness	Material	Pr
#	Name	Layer	mil		
*	*	*	*	*	*
		Surface			
	STIFFENER_FLEX_1	Mask	8	Fr-4	
	TIN_PLATE_TOP	Mask	0.5	Tin	
	ADHESIVE_STIFFENER_FLEX_1	Mask	0.984252	Adhesive Epoxy	
	COVERLAY_FLEX_1	Mask	8	Polyimide	
	ADHESIVE_FLEX_1	Mask	0.5	Adhesive Acr...	
	GOLD_SOFT_FLEX_1	Mask	8	Polyimide	
	PASTEMASK_TOP	Mask	3	Solder Paste ...	
	SOLDERMASK_TOP	Mask	0.590551	Soldermask ...	
1	TOP	Conductor	1.2	Copper	
		Dielectric	8	Fr-4	
2	INT_1	Conductor	1.2	Copper	
		Dielectric	5	Polyimide Ri...	

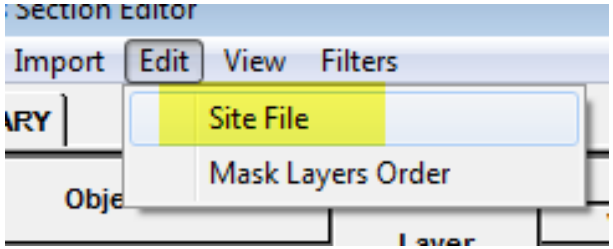
Cross Section
Non-Conductor Layers

- Adding Mask Layers
  - Option 1: Source from new “Mask layer site file”
  - Option 2: Source from Design-based Mask Layers
- Mask Layer Site File
  - Promotes consistency across Design groups
  - Reduces chances of typos
  - File format: XML
  - Site path variable: materialpath

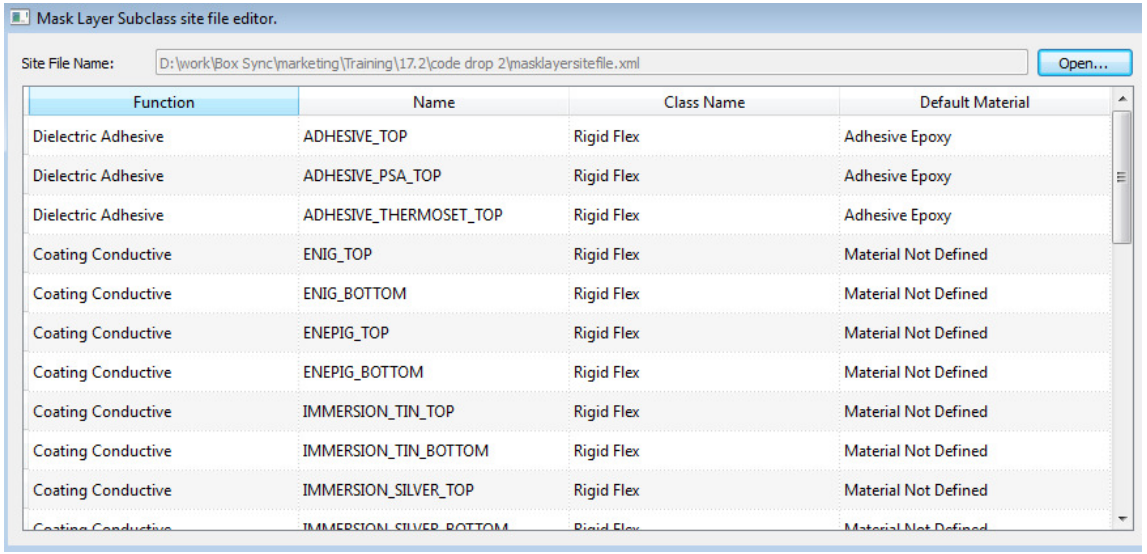


Cross Section
Mask Layer Site File

- Site File User Interface
  - Invoke from Cross Section “Edit” menu
  - Enter Function, Layer name, Allegro Class and material



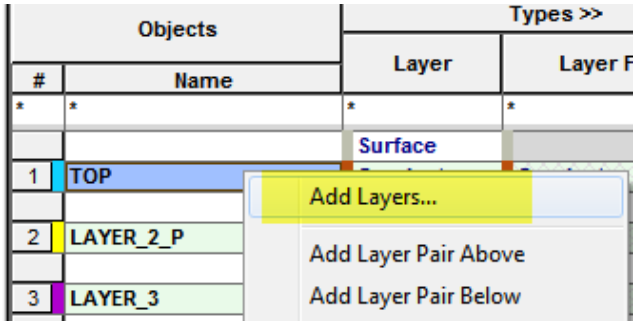
Edit Site File

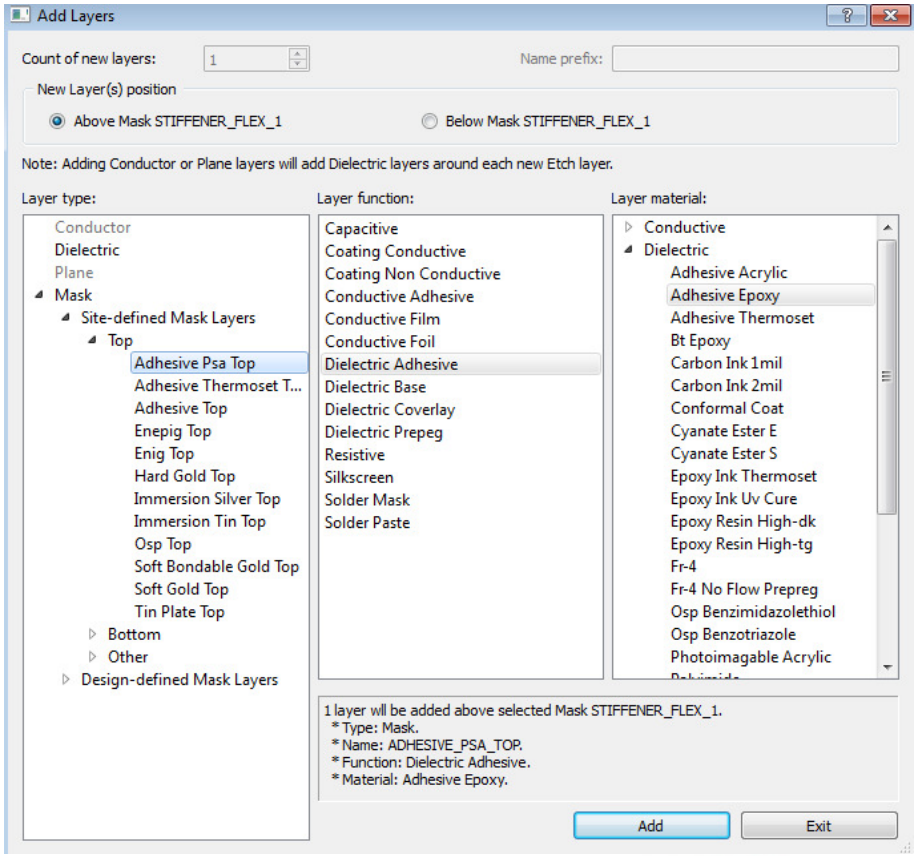


User Interface

Cross Section
Mask Layer Site File

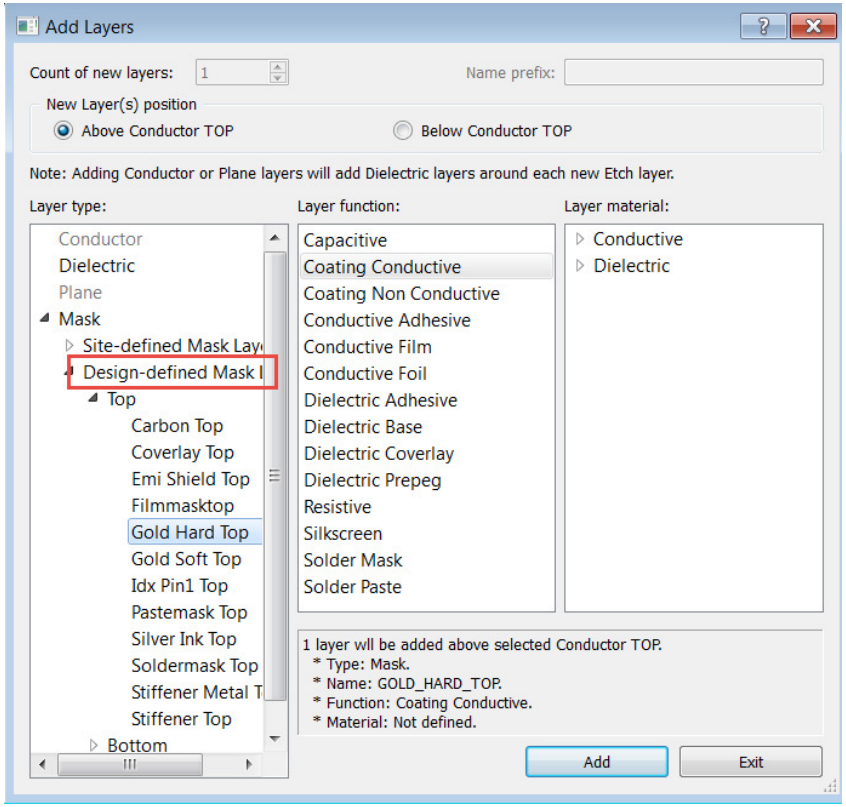
- Adding Layers Sourced from Site file
  - Select “Site defined Mask Layers”
  - Select Top or Bottom
  - Select layer from list





Cross Section
Design Based Mask Layers

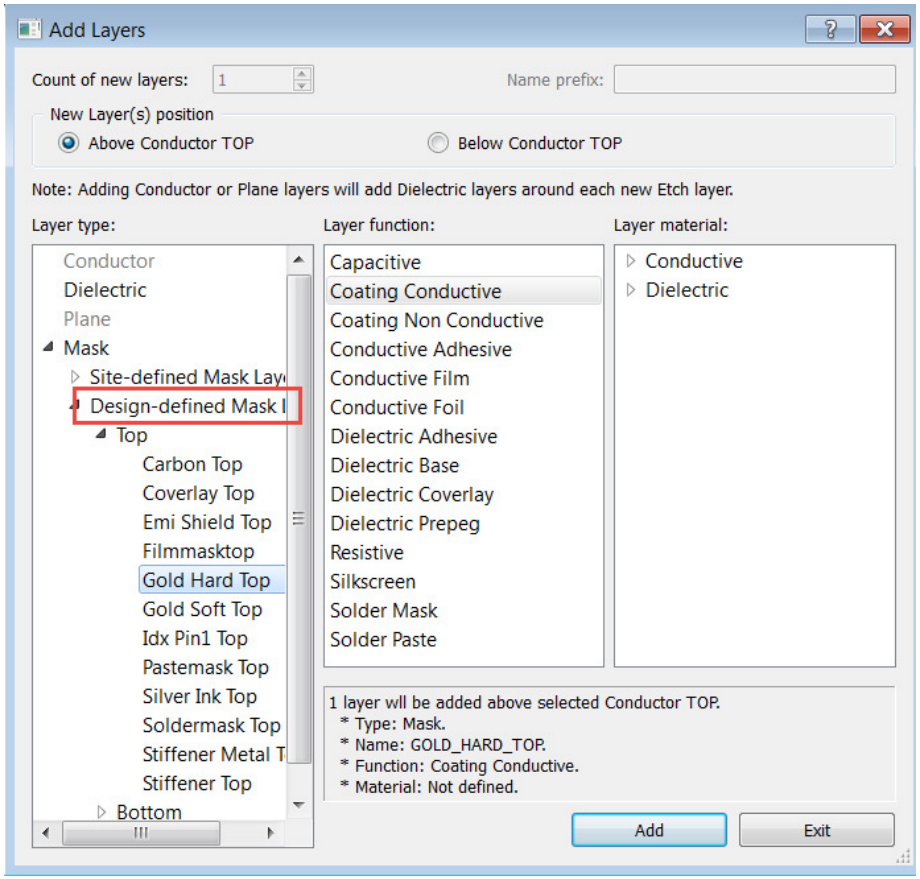
- Add mask layers based on existing subclasses in the database
- User defined layers (some filtering by Allegro)
- Allegro defined mask layers (soldermask, coverlay, stiffener, emi_shield)
- Anything that is a subclass of Board/Package_Geometry, Surface_Finishes or Rigid_Flex that has a suffix on the subclass name of Top/Bottom



If conflict, Site file supersedes Design-defined. Layer will be removed from Design-defined List

Cross Section
Design Defined Mask Layers

- Native Design Layers
  - Carbon
  - Coverlay
  - Emi Shield
  - Enepig
  - Enig
  - Filmmask
  - Gold_Hard
  - Gold_Soft
  - Immersion_Silver
  - Immersion_Tin
  - OSP
  - Pastemask
  - Silver Ink
  - Stiffener
  - Stiffener_Metal
  - Tin_Plate
  - User Defined Layers

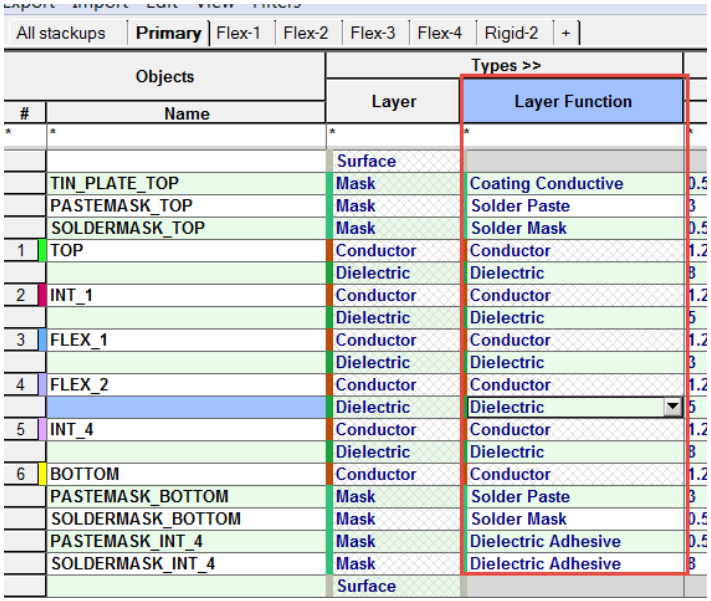


Cross Section
Support for IPC Layer Functions

- Layer Functions
  - IPC 2581 driven Mask and Dielectric subtypes
  - Attached to IPC-2581 stackup as attributes for fab instructions

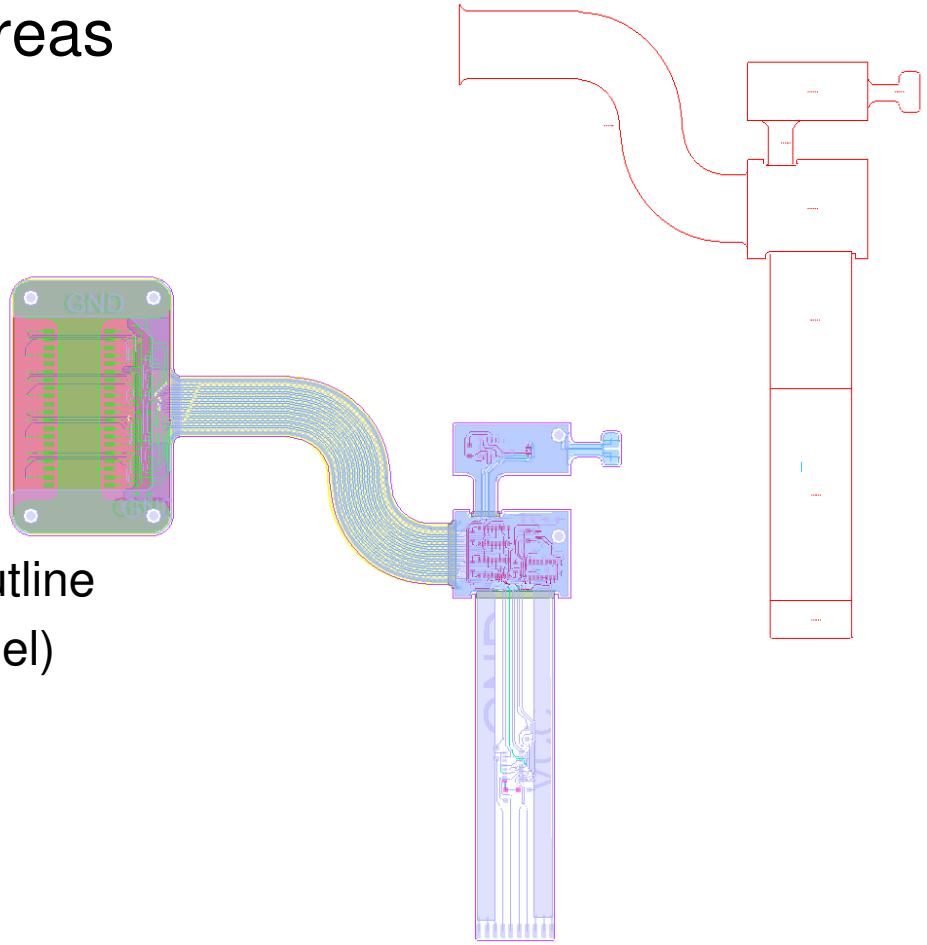
Mask Category
Capacitive
Coating Conductive
Coating Non Conductive
Conductive Adhesive
Conductive Film
Dielectric Coverlay
Resistive
Silkscreen
Solder Mask
Solder Paste
Dielectric Adhesive
Dielectric Prepreg

Dielectric Category
Dielectric Core
Dielectric Base
Dielectric Bong Ply
Dielectric Adhesive
Dielectric Prepreg



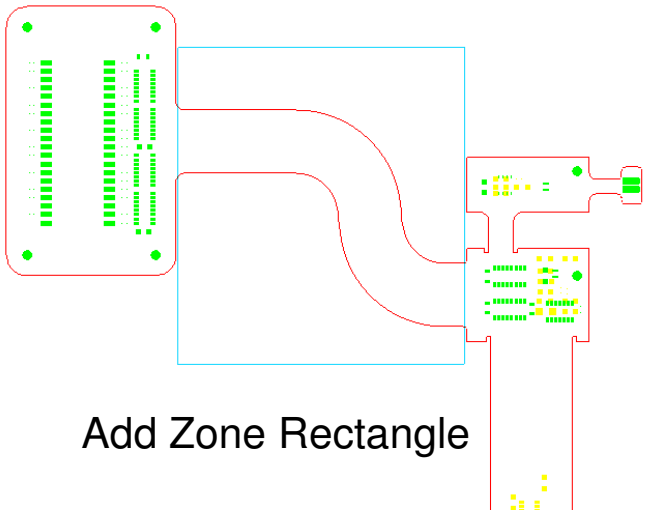
Physical Zones

- Zones represent physical areas of the board that differ in layers/materials
  - Rigid Flex
  - Material Inlay
- Zone details
  - Single contiguous shape
  - Automatic snapping to Design Outline
  - Applies to All layers (Vertical model)
  - References to
    - Stackup
    - Constraint Region
    - Room

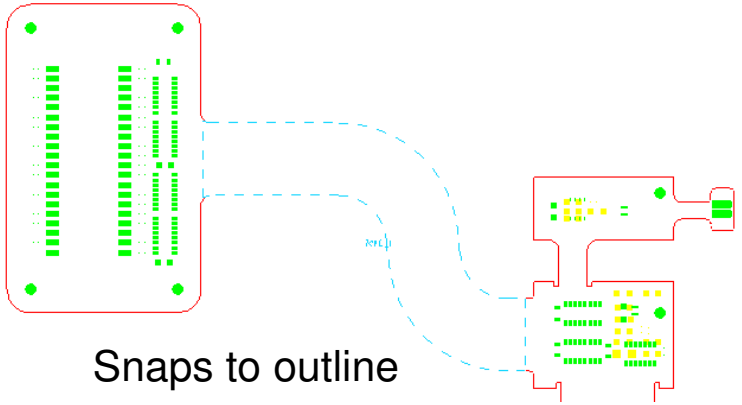


Adding Zones

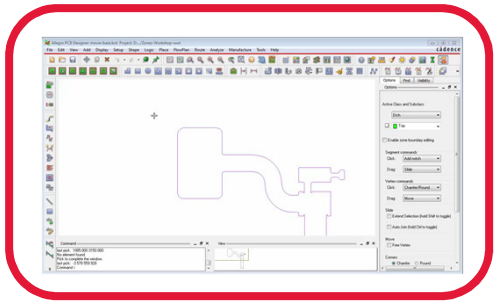
- Using the new ***Zone > Create*** command, simply window select an area
- Does not require precise mouse picks
- Automatic snapping to Design Outline



Add Zone Rectangle



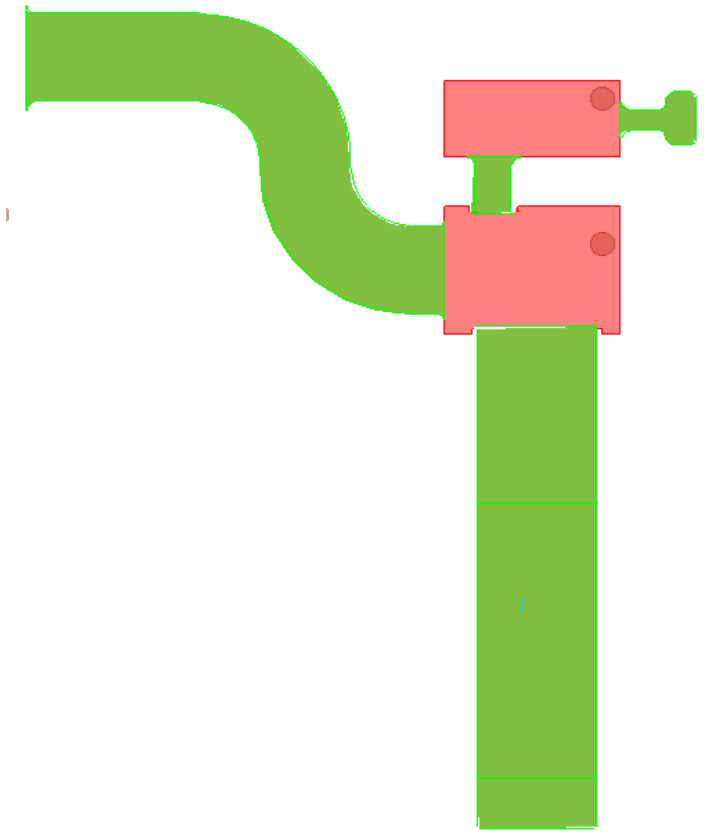
Snaps to outline



Movie

Zone Route Keepouts

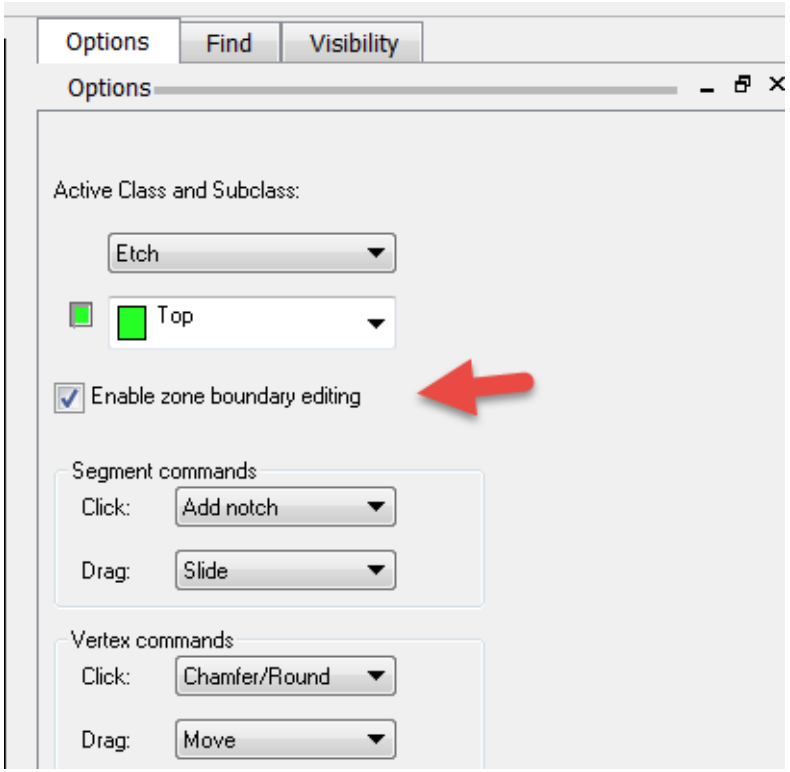
- Automatic Route Keepout Generation
- Applied to layers not associated with the zone
- Flex zone might have RKO's added to layer Top and Bottom

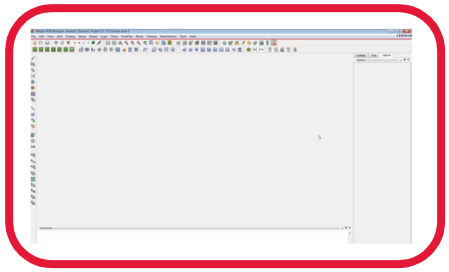


Route Keepouts

Editing Zone Boundaries

- A special mode is required to edit Zone Boundaries
- Requires Shape Application Mode
  - Enable “Zone boundary editing”

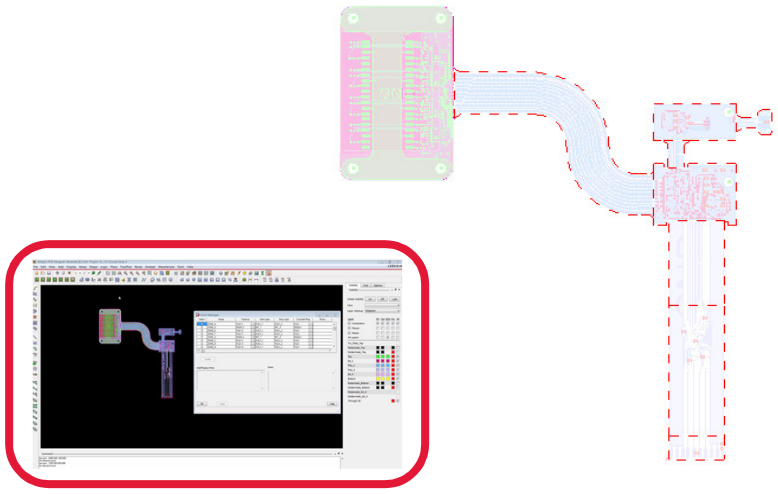




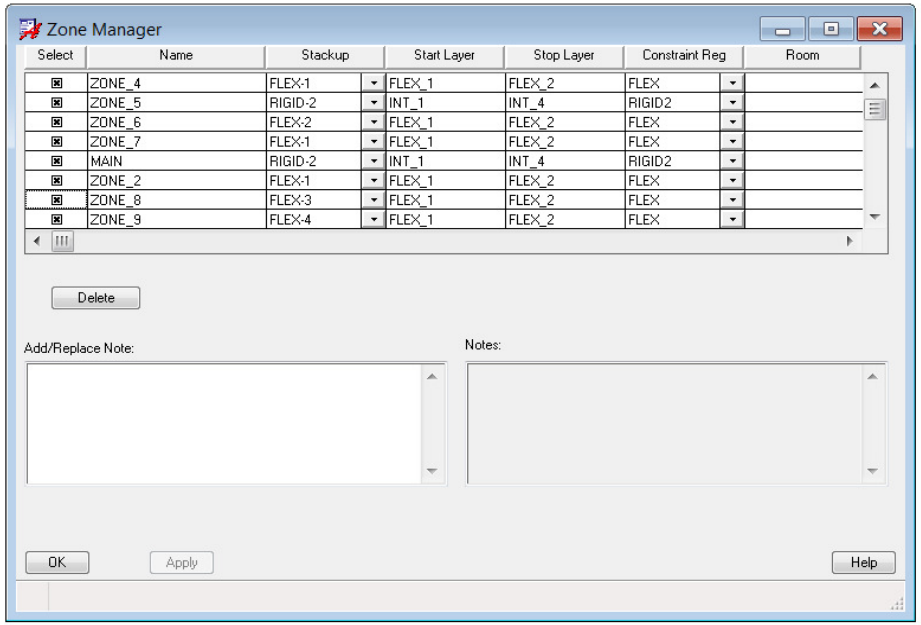
Movie

Zone Manager

- Method to Assign Physical Zones to Stackups
- Includes Renaming and Deleting functions
- View Start/Stop layer of Zone
- Assign existing Regions to Zone
- Room generation based on Zone outline

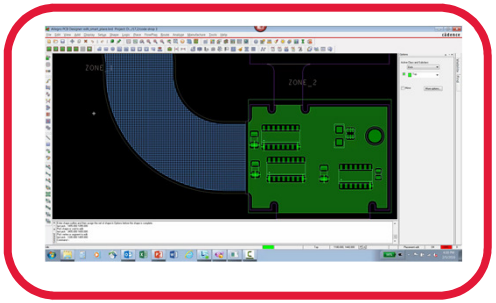


Movie



Dynamic Zone Placement
Auto Drop Down

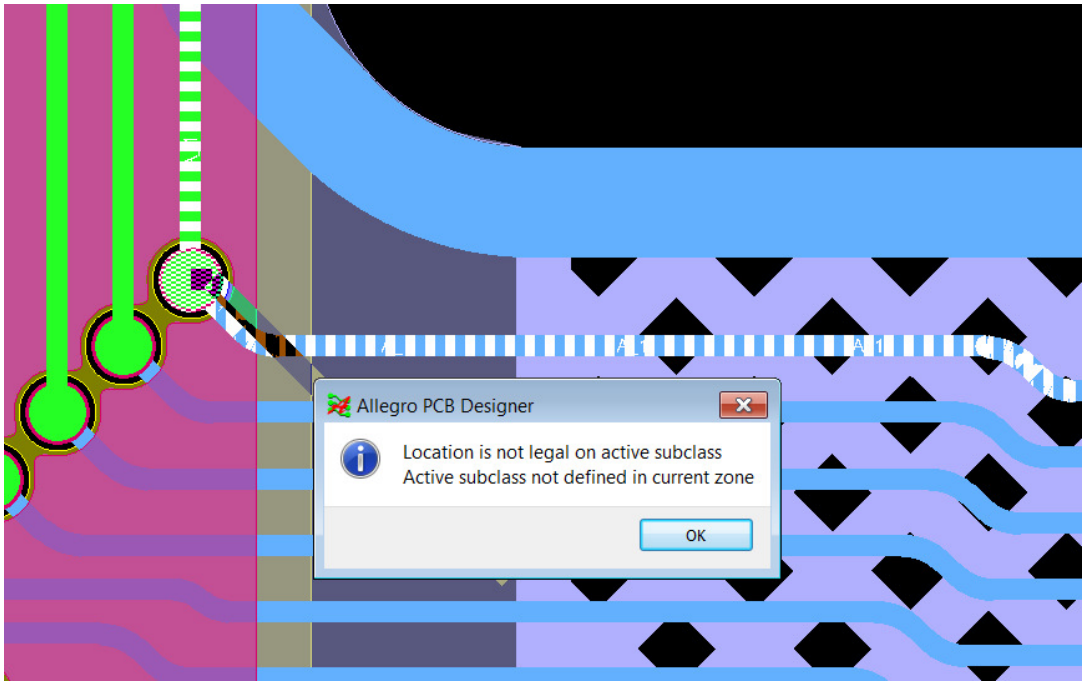
- Rigid-Flex design using today's tools requirement embedded component setup to place components on the flex layer
- These layers are registered inner database layers
- Designer must remember to use RMB – Place on layer function for each component moved
- 17.2 streamlines this process, watch the movie as we moved components from the Top layer of the Rigid to the Top Flex Layer!



Movie

Routing Across Zone Boundaries

- Routing across zone boundaries where Stackups are different may generate this warning if the current routing layer is not supported in the adjacent zone



Inter-Layer Design Rule Checks Rigid-Flex

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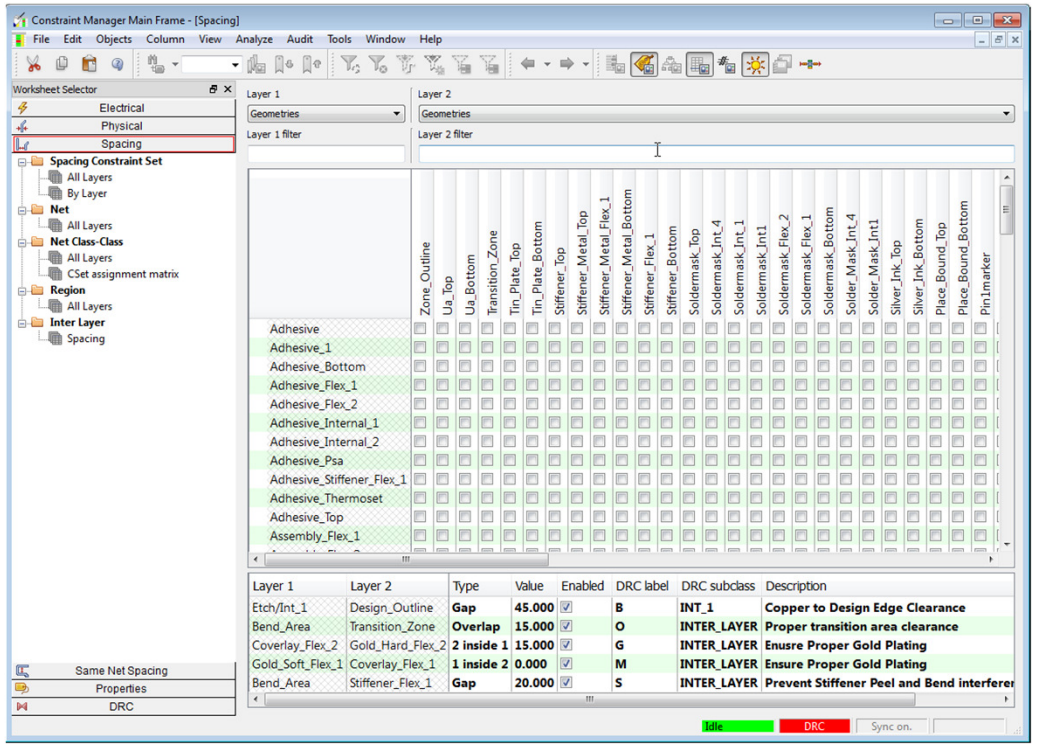
Inter Layer Checks (ILC)

- New DRC Engine checks
  - Mask layer to mask layer
  - Mask layer to surface metal
- Allows checks for
  - Coverlay to pad checks
  - Mask to pad checks
  - Precious metal to coverlay
  - Bend area/line to stiffener, component, pin, and via
- Layer Selection GUI
  - Matrix of applicable subclasses
  - Filtering capabilities
  - User defined DRC 2nd letter ("I" fixed first character)
  - Comment Field

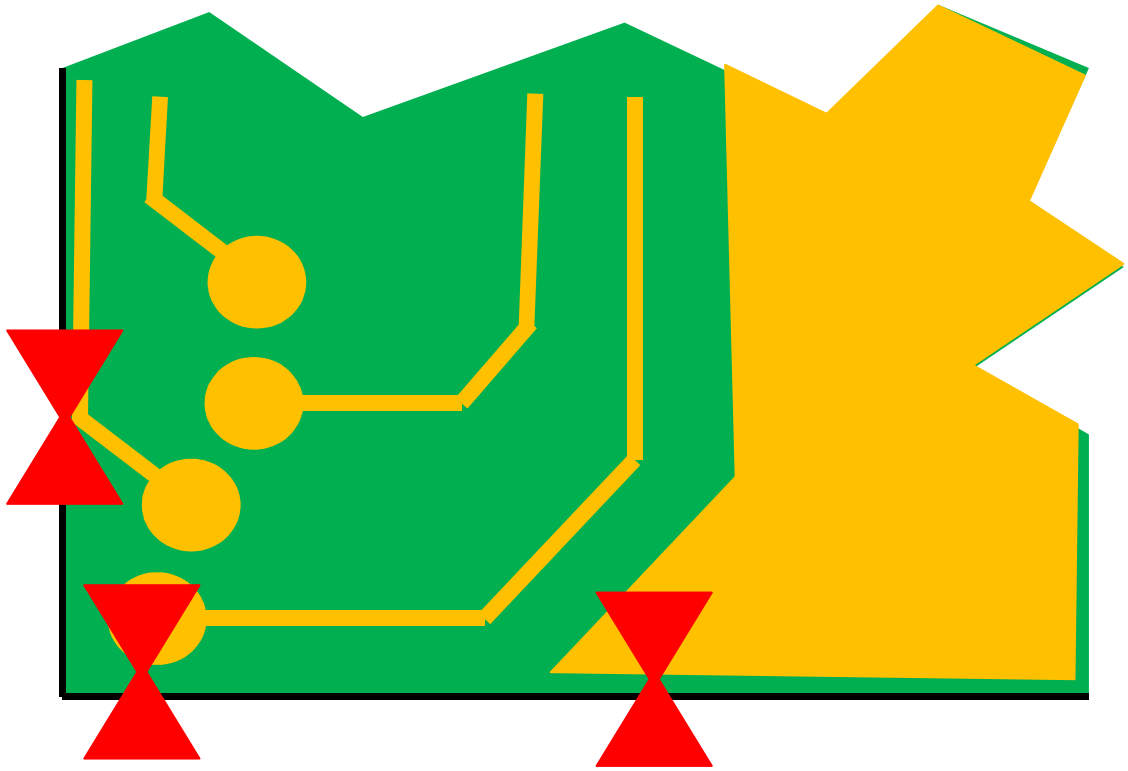


Does NOT Check

- Etch subclass to Etch Subclass
- Same Subclass
- Differential Pins from Vias and Traces from Etch

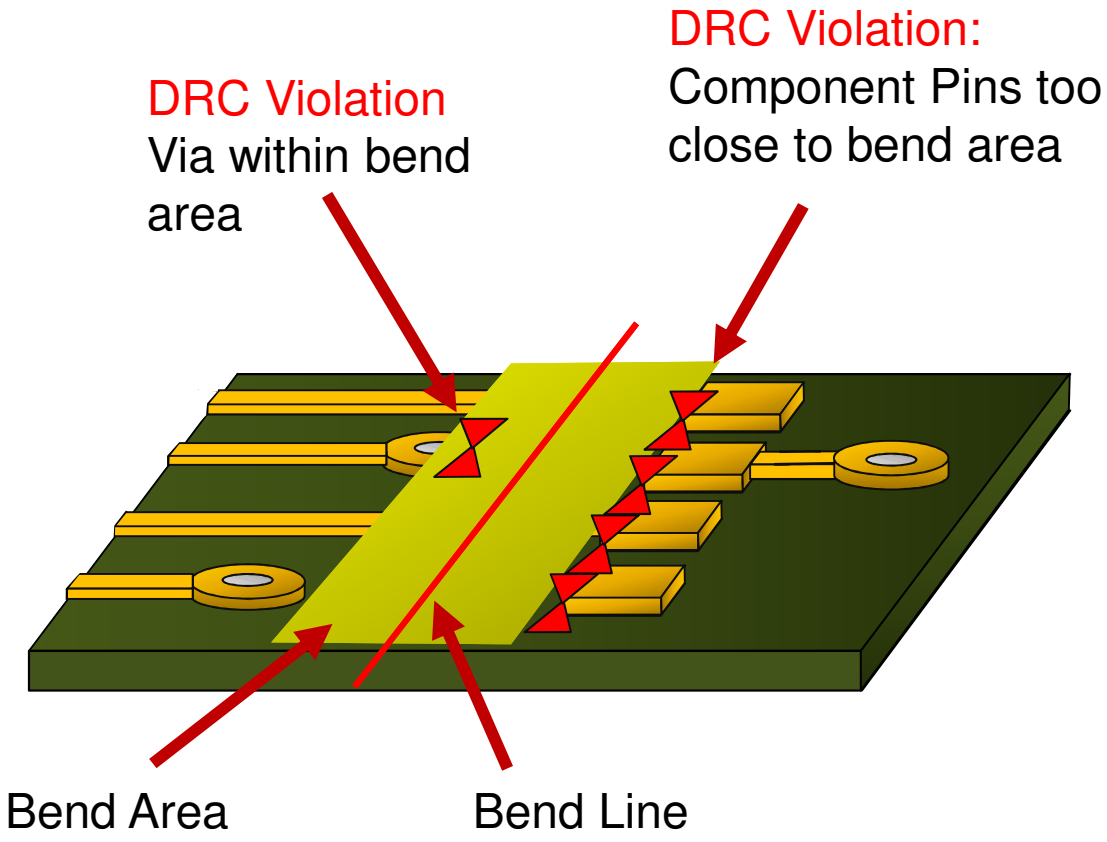
ILC Checks
Gap

- Specifies a spacing between Geometry on one subclass to another subclass



Vias, Pins and Conductors must be 30 mils from Design Edge

ILC Checks
Gap



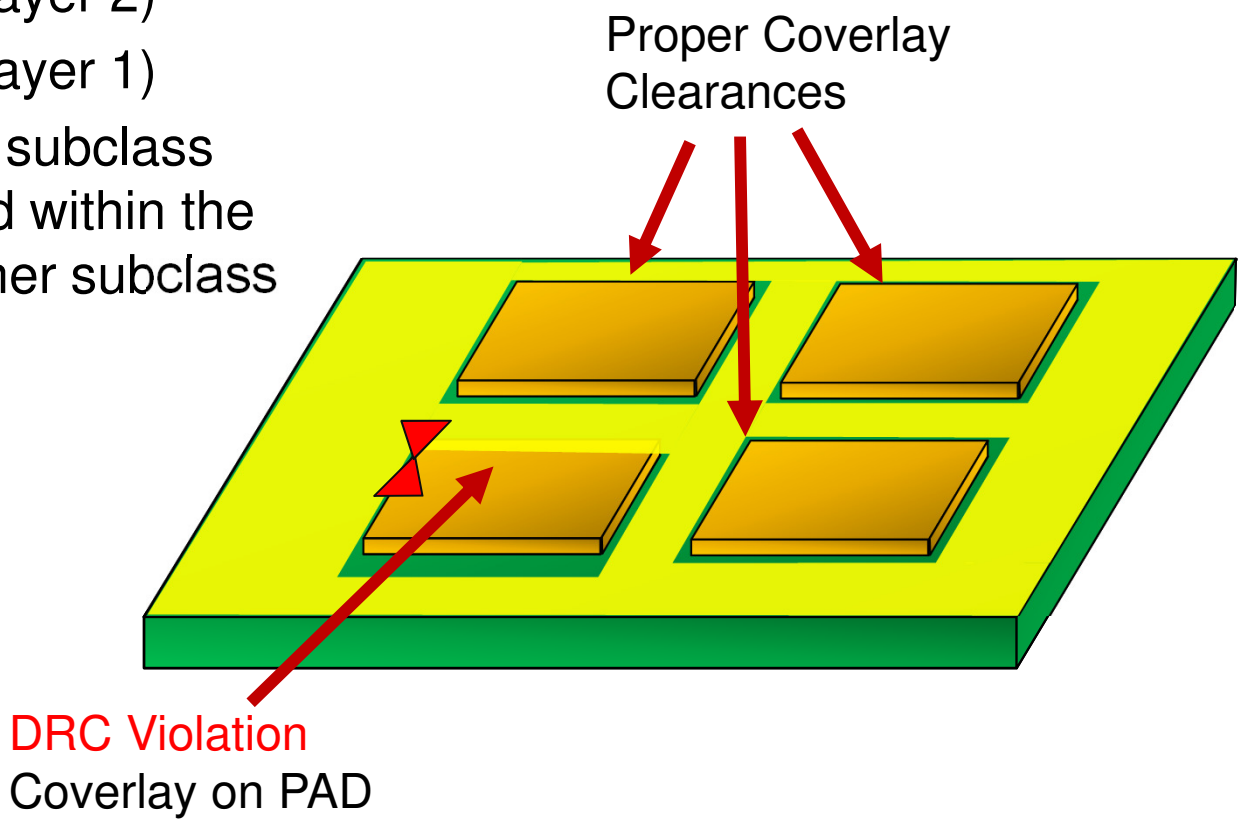
ILC Checks
Overlap

- Specifies a minimum overlap of two geometries on different subclasses

Transition zone must overlap bend area by 15 mils.

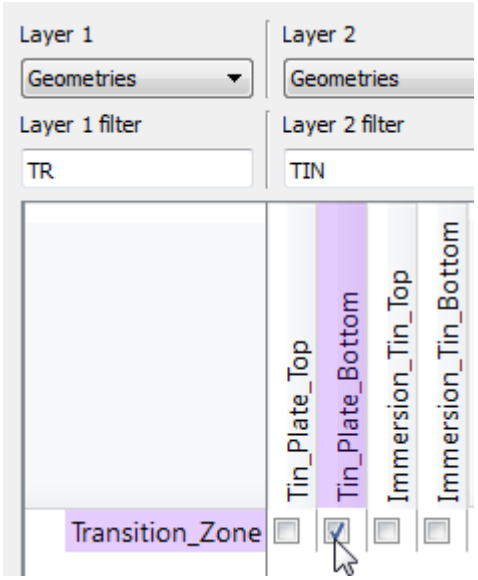
ILC Checks
Inside Rule

- (Layer 1) inside (layer 2)
- (Layer 2) inside (layer 1)
- Geometry on one subclass must be contained within the geometry of another subclass geometry



Creating Inter Layer Rule

- Select Subclass
  - Select checkbox in layer Matrix
- Select Rule
  - Choose one of three
- Set Value
- Enable



- Define Label
  - First character is defined as I
  - Define 2nd character
  - 1 character limited to A-Z, a-z, or,0-9
- Set DRC Display Layer
  - New DRC display layer: INTER_LAYER
- Add Description
  - Add description for rule

Layer 1	Layer 2	Type	Value	Enabled	DRC label	DRC subclass	Description
Transition_Zone	Tin_Plate_Bottom	**Overlap**	**25.000**	☑	**O**	**INTER_LAYER**	**Prevent Tin Plate Peeling**

Preserving Rules: Constraint Manager Export > Constraints

Shape Editing Update

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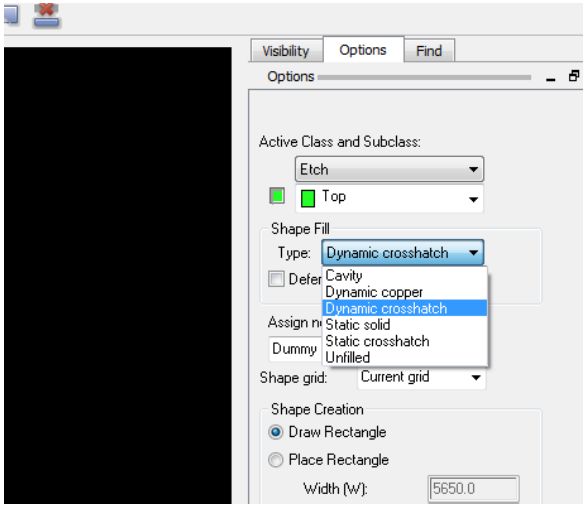
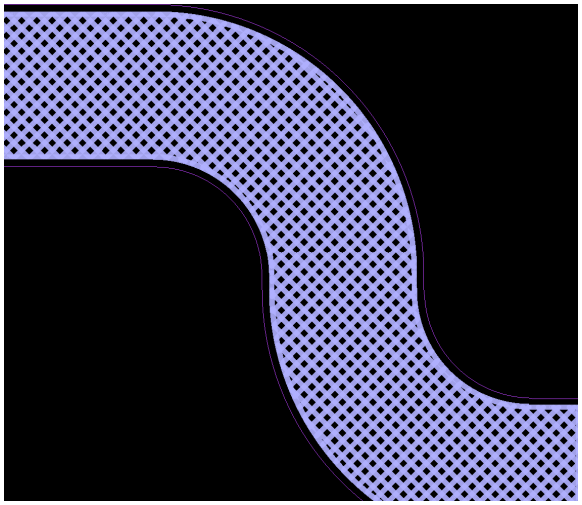
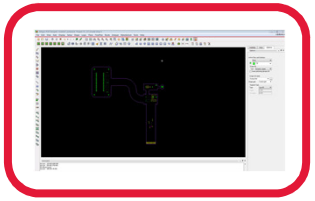
Cross Hatch Shapes

- Usability update
  - Cross Hatch (Xhatch) shapes are common with Flex Designs
    - Lighter in weight
    - Adheres better, less prone to cracking at bend areas
    - Dynamic option for cross hatch now available in the shape-add pull-down menu
    - Streamlines the creation flow eliminating several extra steps



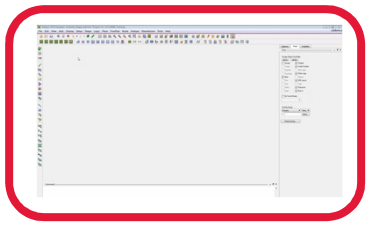




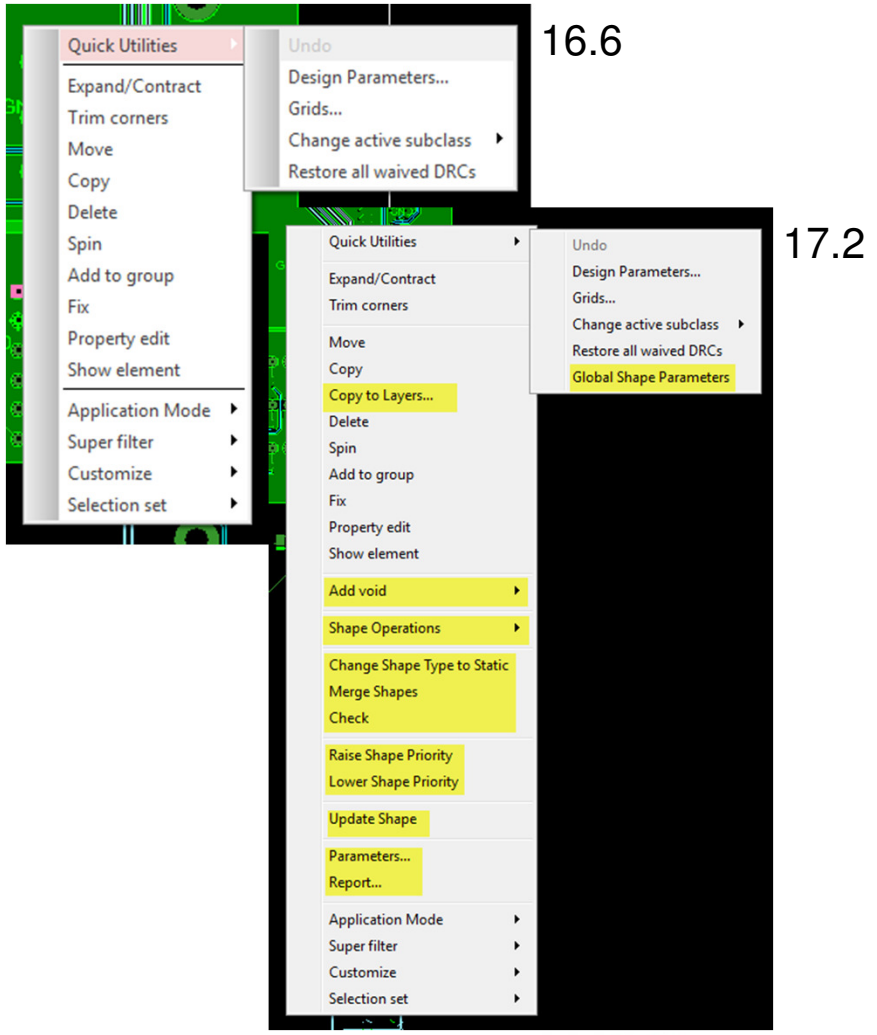
Movie

Shape Edit Application Mode Update

- Shape App Mode introduced in 16.6-2015 release
- Preferred environment for editing shape boundaries
- 17.2 adds support for additional context sensitive edit commands
  - Use the RMB to access popular commands like ***Copy to Layers***, ***Raise Priority***, ***Merge*** and others
- Movie shows new shape Boolean operations (OR, ANDNOT)

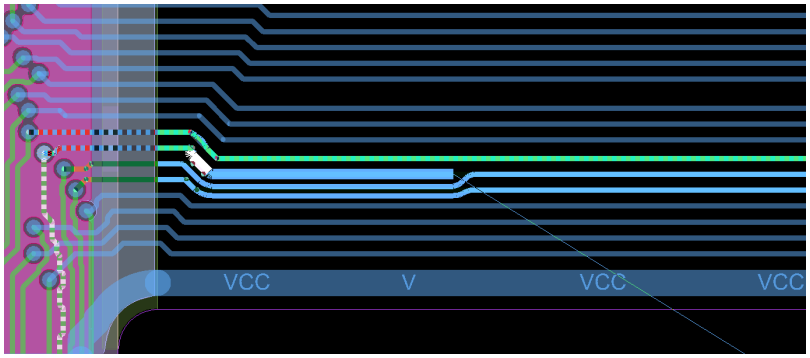


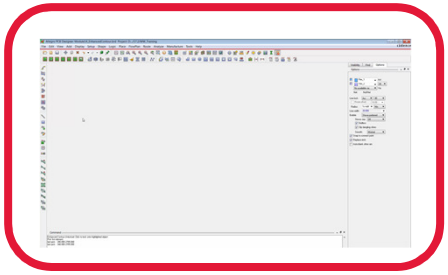
Movie



Routing Enhancements
(Flex Designs)

- Enhanced Contour Routing
  - New prototype feature improves methods to contour to adjacent connect line or route keepin
  - Improved use model, less dialog clicks
  - While “locking” on to contour trace, push & shove of traces in the opposite direction is possible
  - Watch movie!
- Arc Routing Updates





Movie

Embedded Component Design Updates

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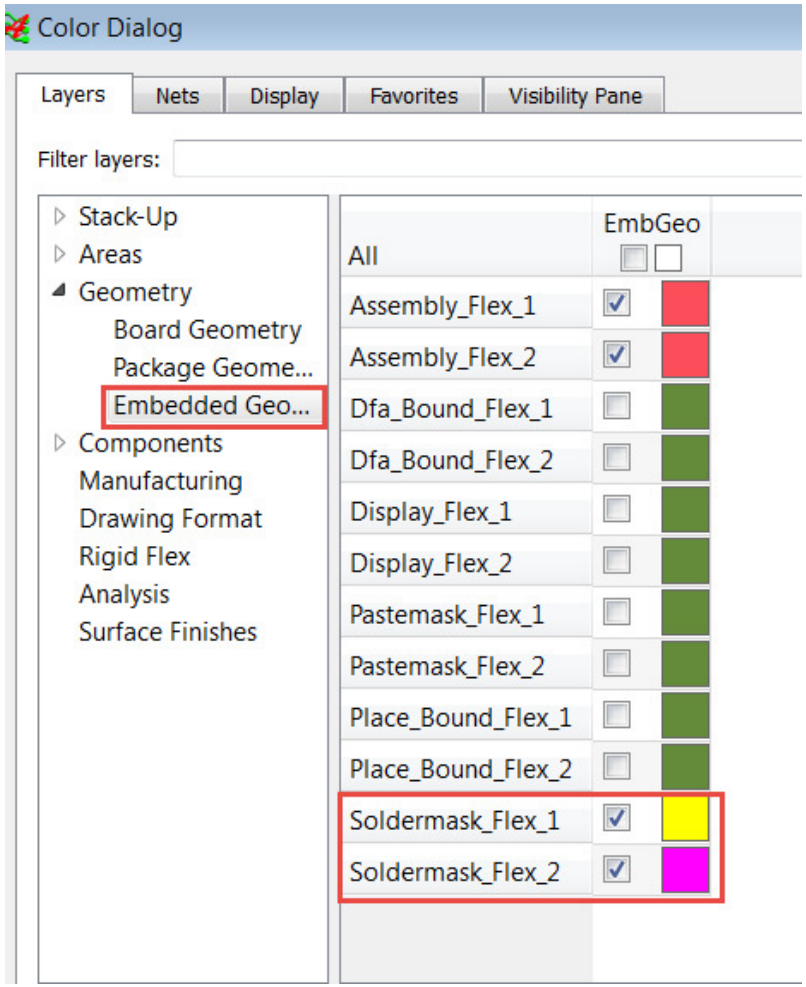
Embedded Component Design

- **Copy** command can be used to copy placed embedded symbols
  - Typically done in advance of the incoming netlist to reserve space for anticipated changes
- **Swap Components** command is now supported for embedded components
- **Soldermask Support**
- **User Defined Entries in Embedded_GEO Class**



Color and Visibility

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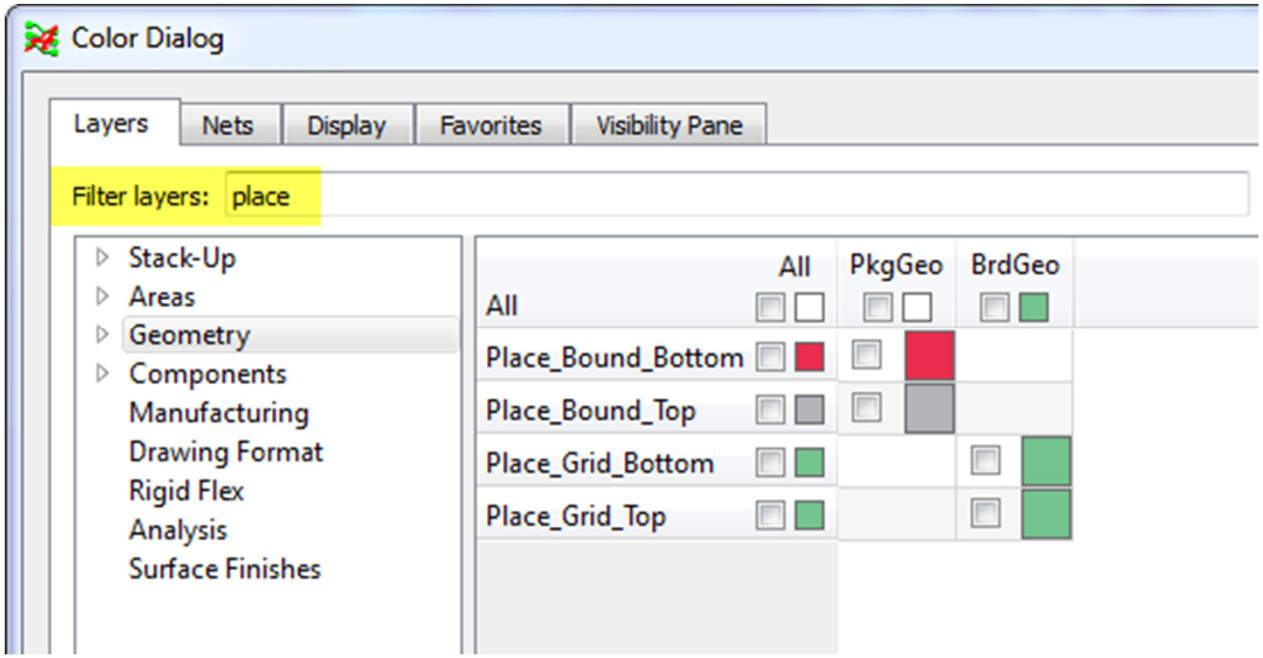
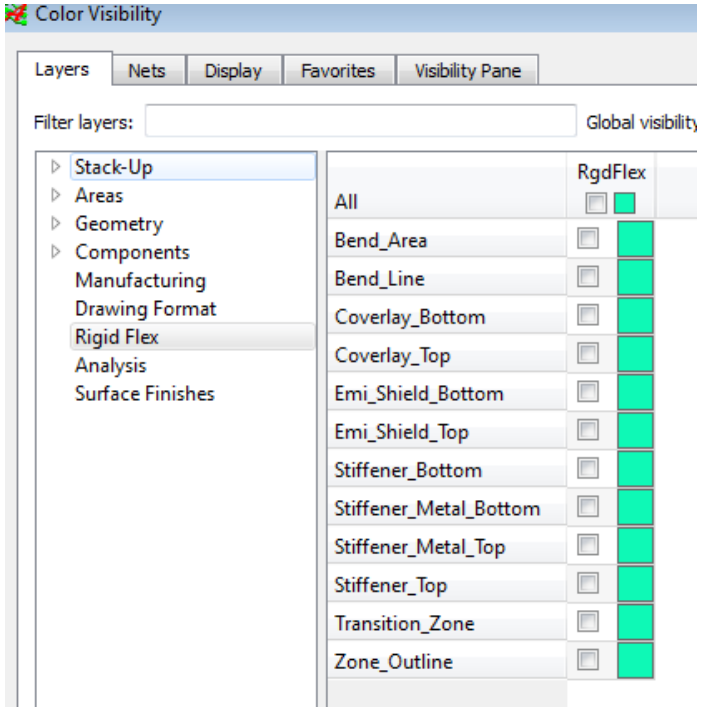
Color Dialog Overview

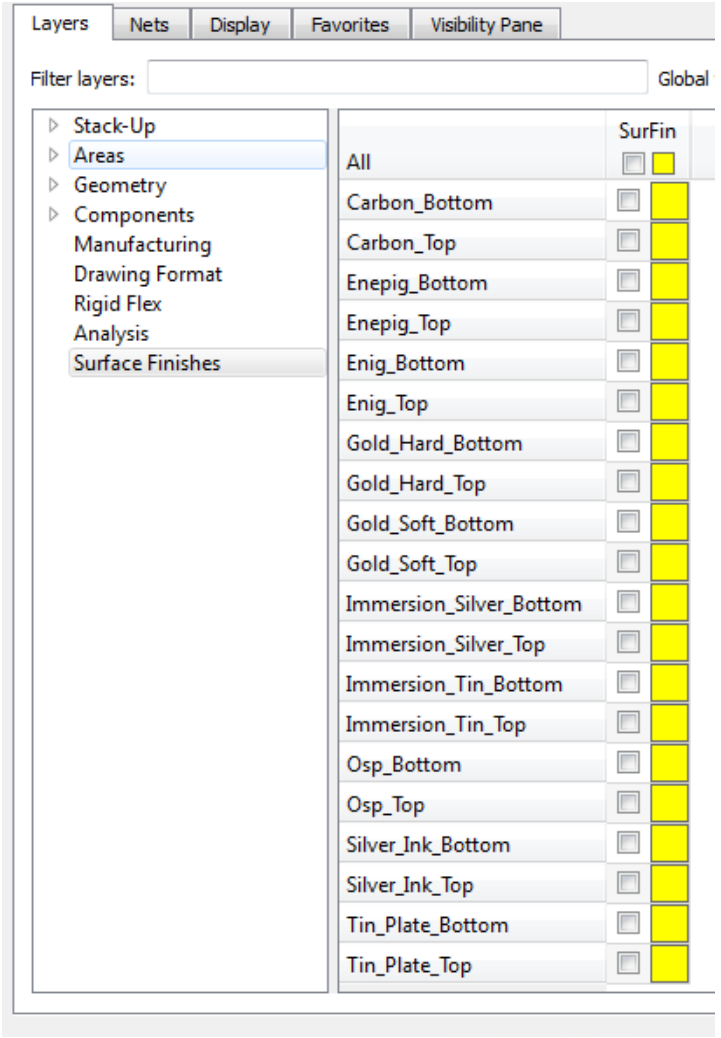
- Functional Tabs across top of User Interface
- New Filtering field
  - Quick method to locate layers



Color Dialog Overview

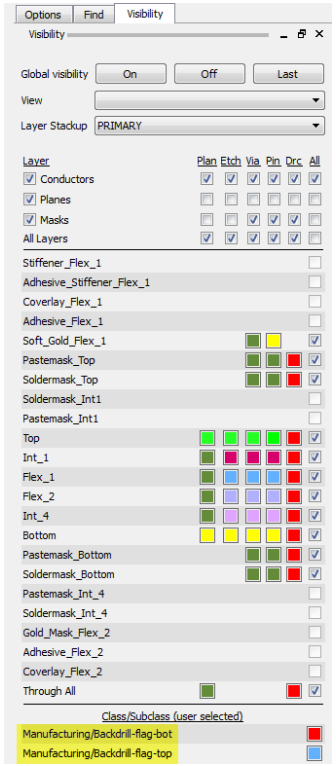
- 2 new Database Classes
  - Rigid Flex
  - Surface Finishes

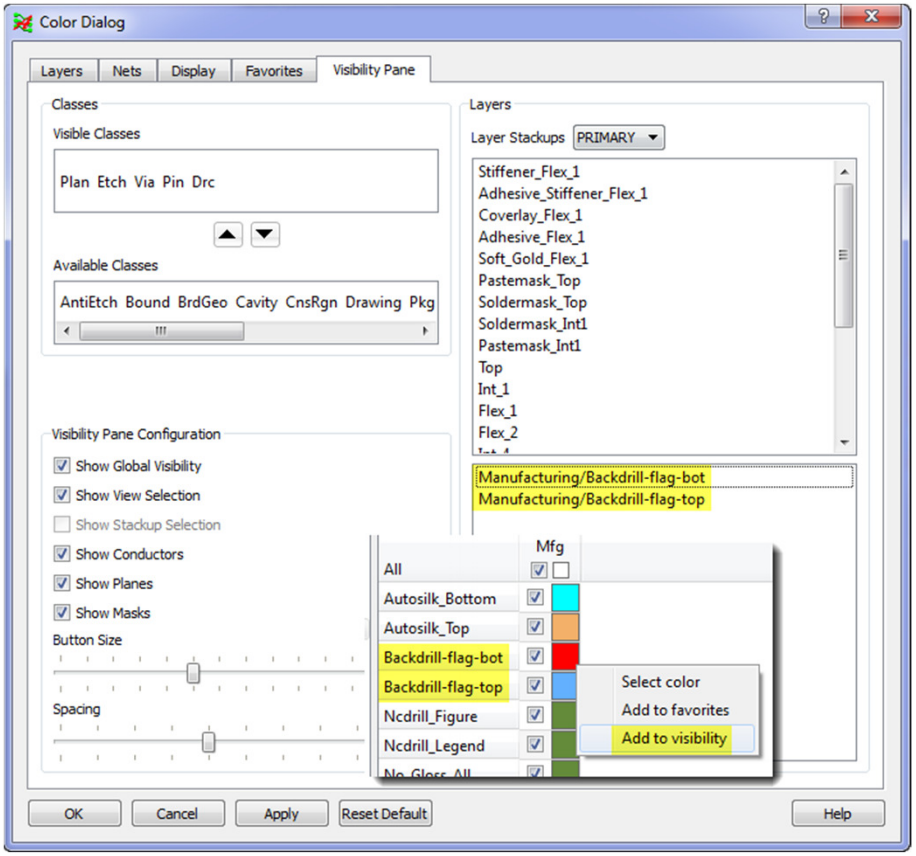




Color Dialog Overview

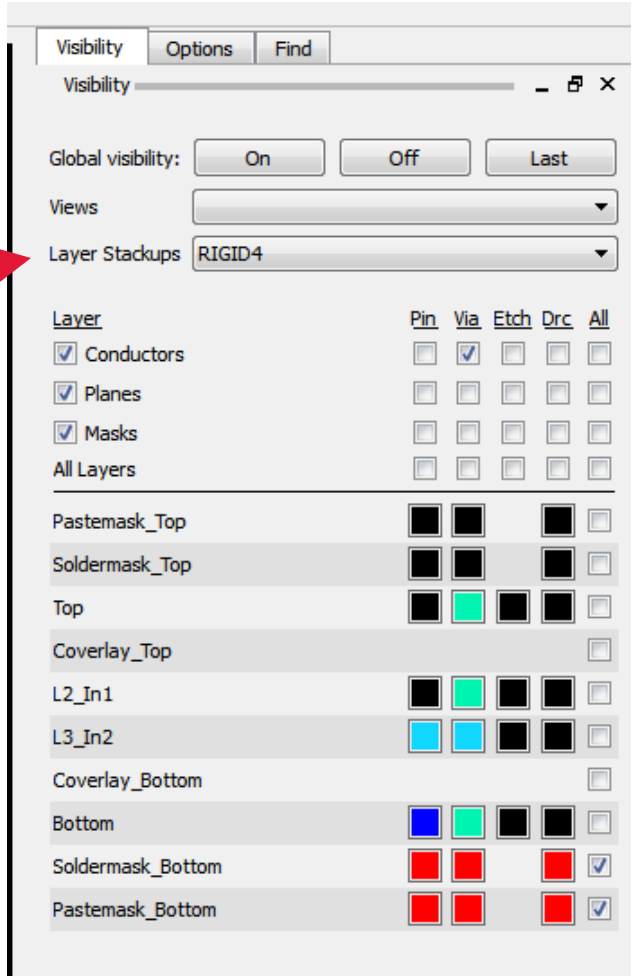
- Visibility Pane Configuration
  - Customize Class Headers
  - Add custom layers to Pane
  - Configuration options:
    - Global Visibility
    - View Schemes
    - Conductors
    - Planes
    - Masks
    - Button size
    - Button spacing

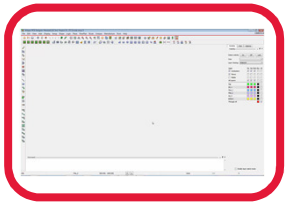




Visibility Pane Updates

- Display of Mask Layers
  - Provides quick access to Mask/Coating Layers defined in Cross Section
- Layer display by stackup
  - Filter list of layers displayed to align with one of the defined stackups
- Quick access to Global visibility settings
- Legacy Horizontal Tabs Restored
  - Visibility; Options; Find

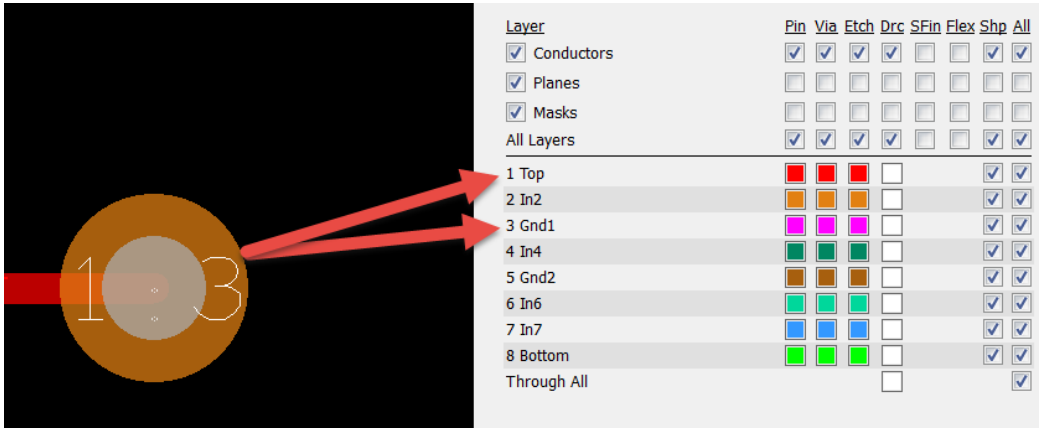




Movie

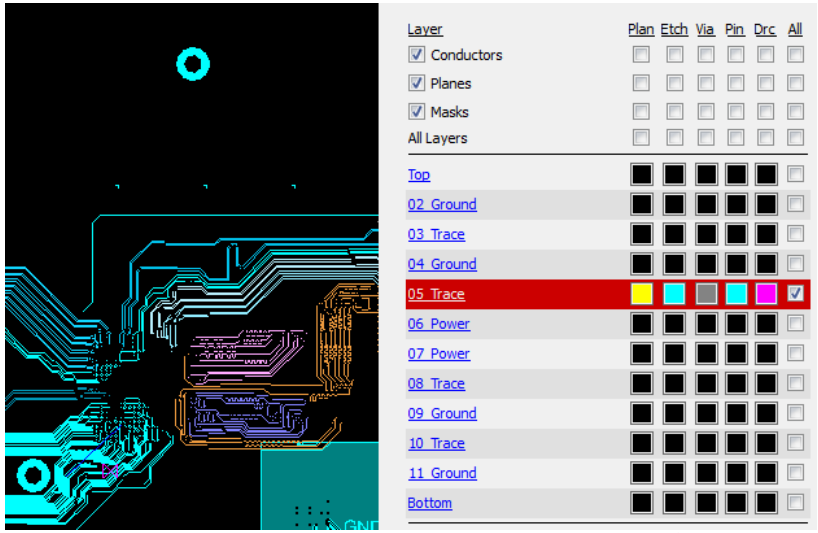
Productivity Enhancement
QIR5 Addition

- Via Label Enhancement
  - Increasing trend in BB via usage
  - Via labels display begin/end layers (typically 1 to N)
  - Labels not always aligned with actual layer names
    - Example: label 3 = Gnd1
  - Enable label column in Color Dialog – Visibility Pane Tab
    - "Show Layer Numbers"

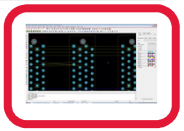


Visibility Pane
Layer Select Mode

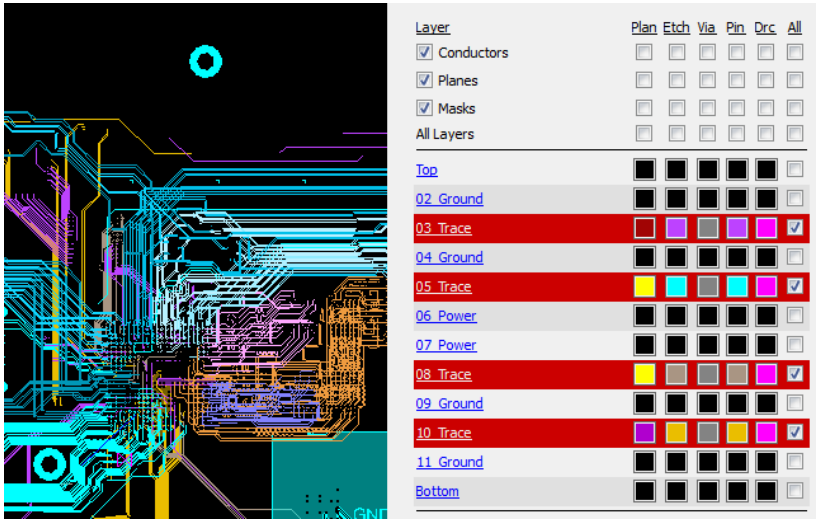
- Quick method to change layer visibility
- Layers become HTML linked in this mode
- Simply click on any layer to change the display
- Use Control key to extend selection to multiple layers



Single Layer Mode



Movie



Multiple Layer Mode

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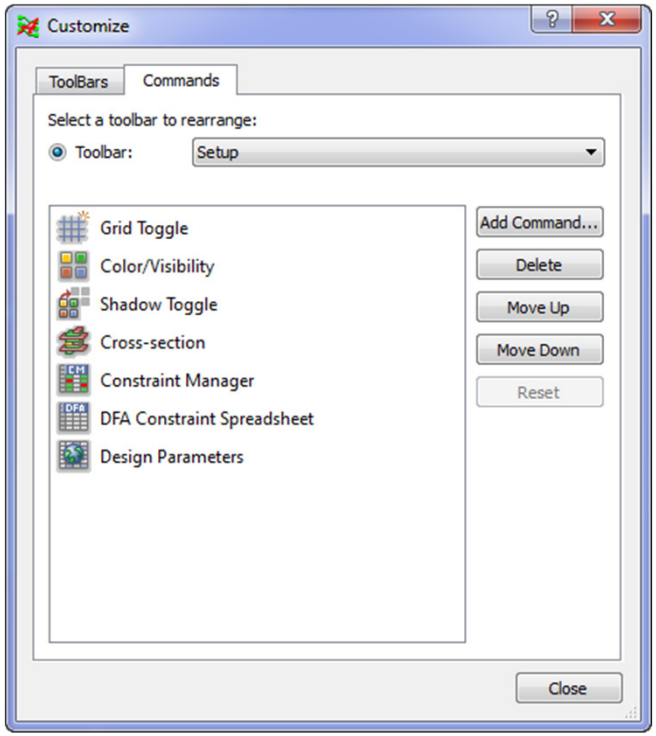
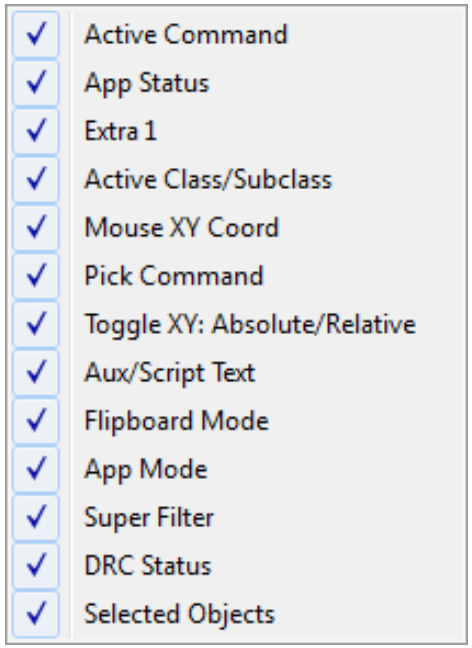
Canvas Enhancements

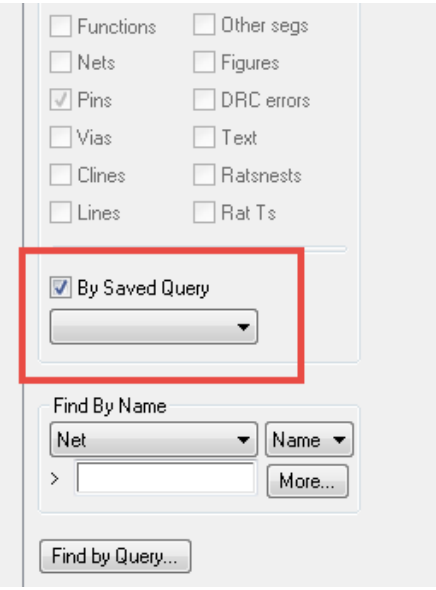
- Customizable Toolbars
- Status Bar – Show/Hide Selections

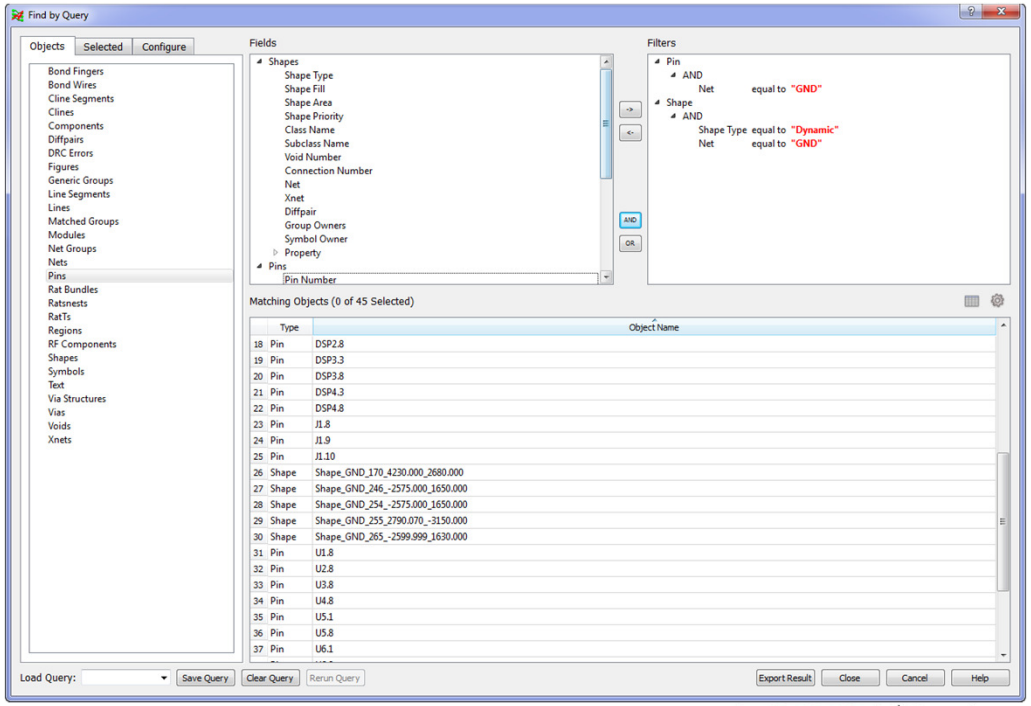


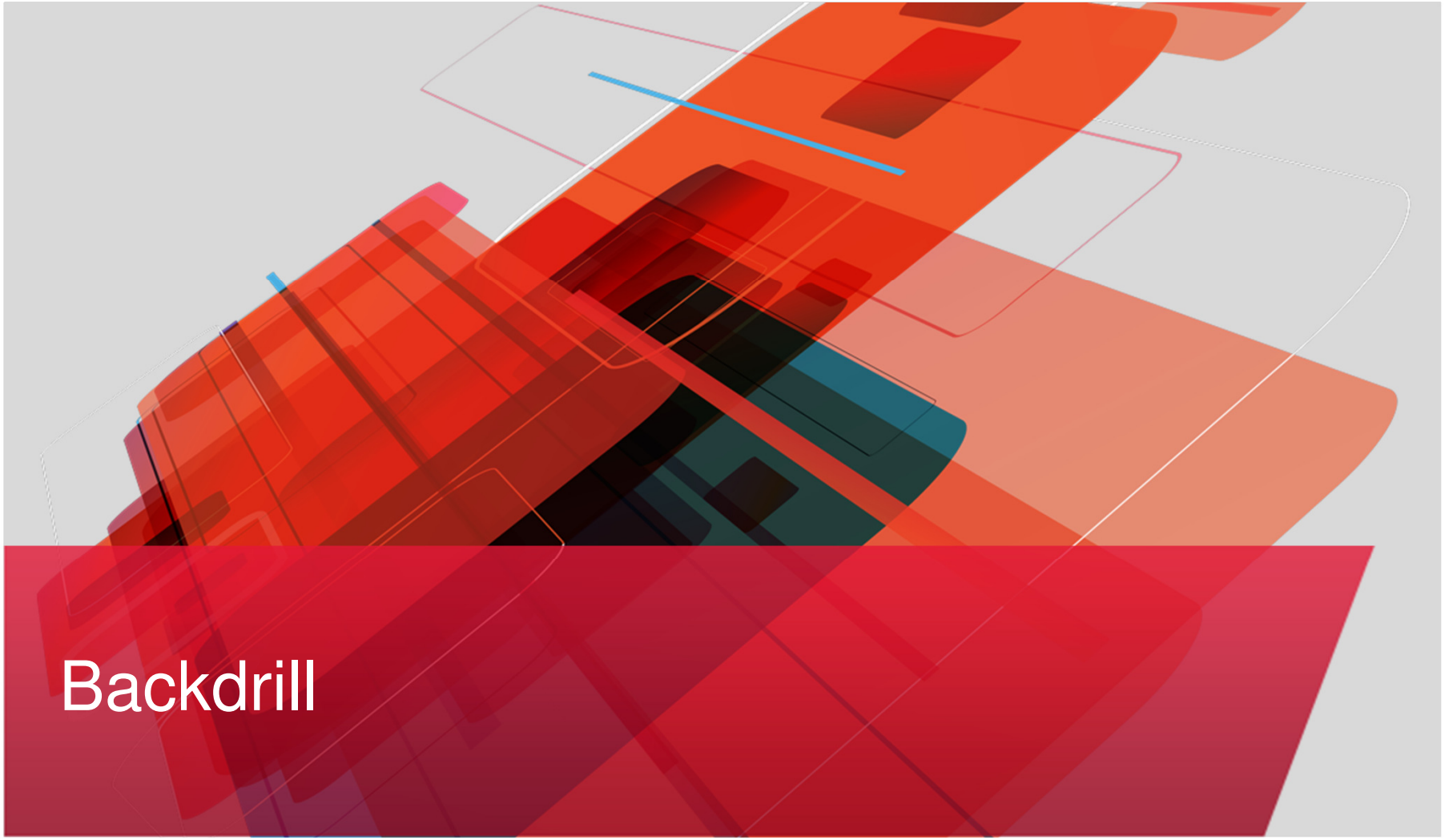


Find
Find By Query

- Completely re-designed with access to all Objects
- Create, Save, Edit, Re-Use, Rerun, Export
  - Powerful when used in conjunction with Edit commands
- Find using “By Saved Query”







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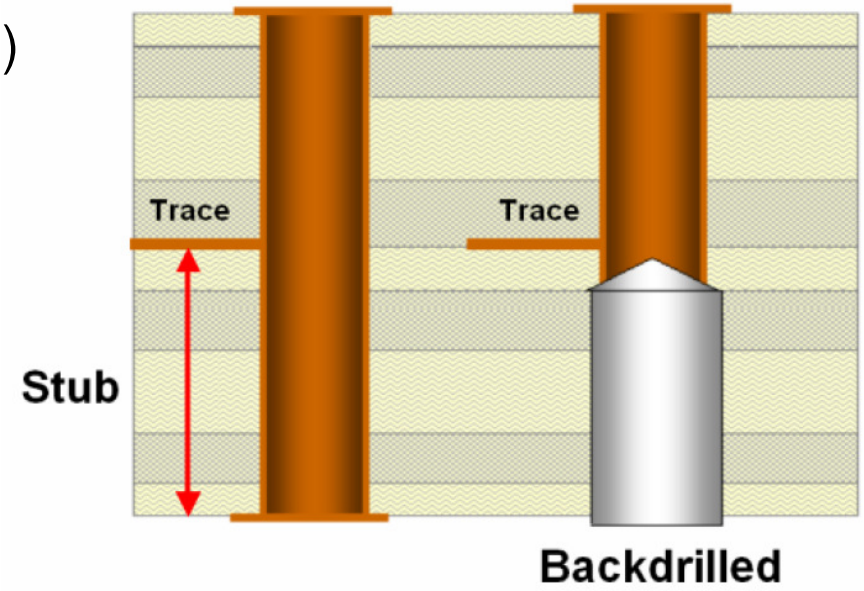
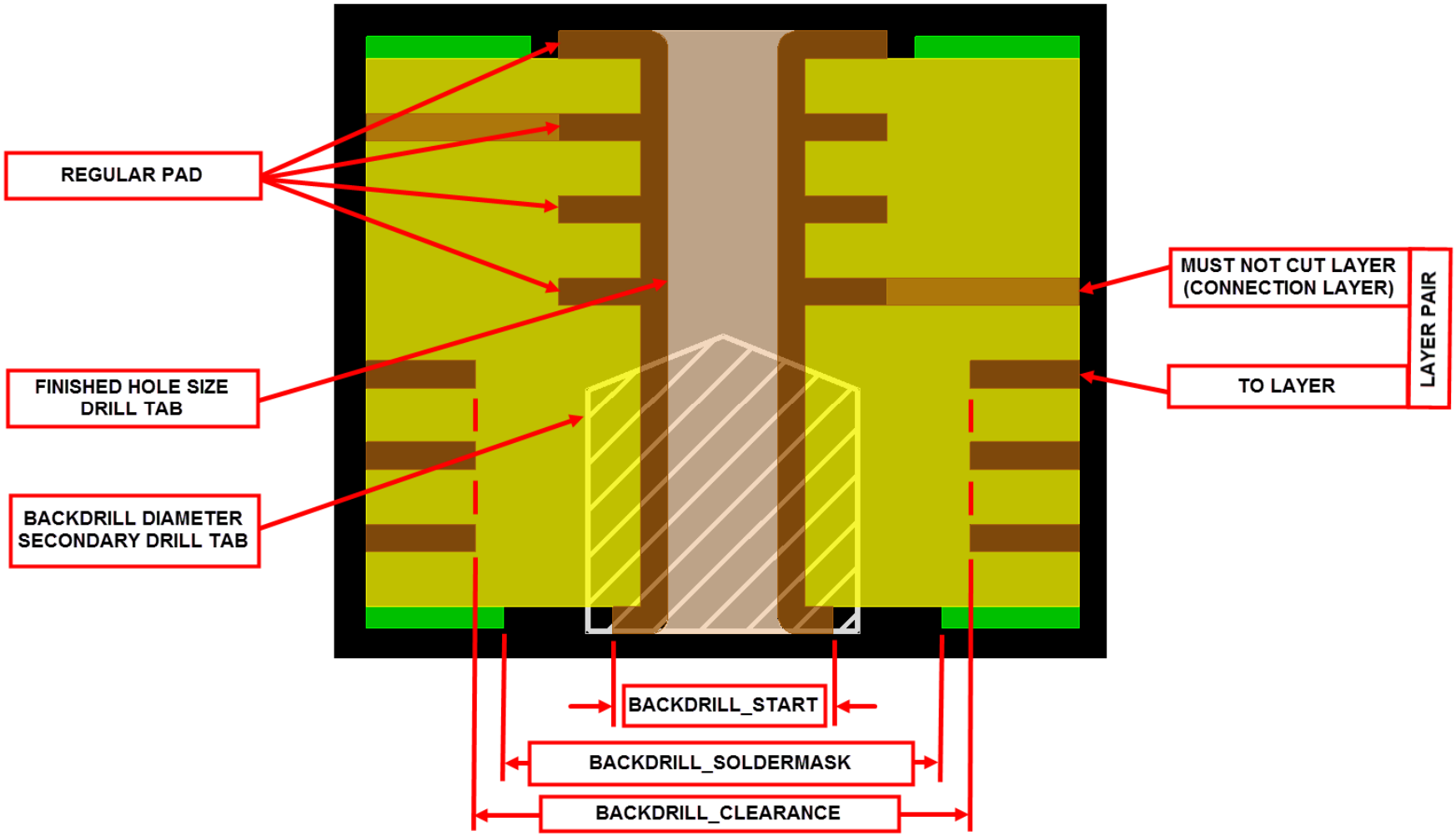
Backdrill Overhaul

- Backdrill introduced in 15.7
- Later enhanced to support any layer to any layer backdrill
  - Typically Core vias
- Usage trends increasing across Design community
- Two available flows to consider
  - Library Driven Flow (Preferred)
  - Design Quick Utility

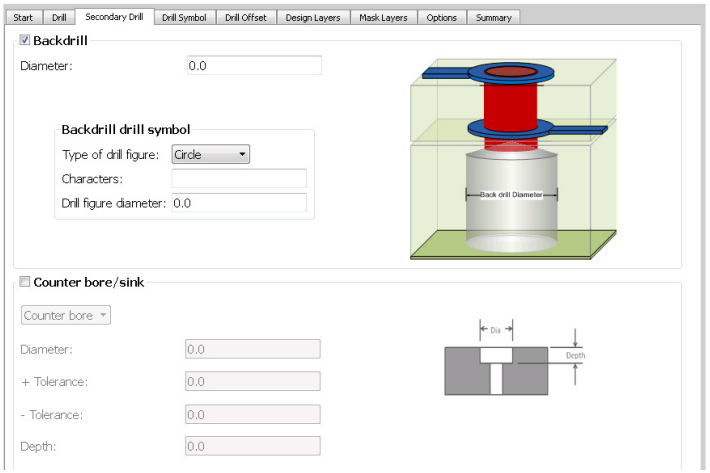


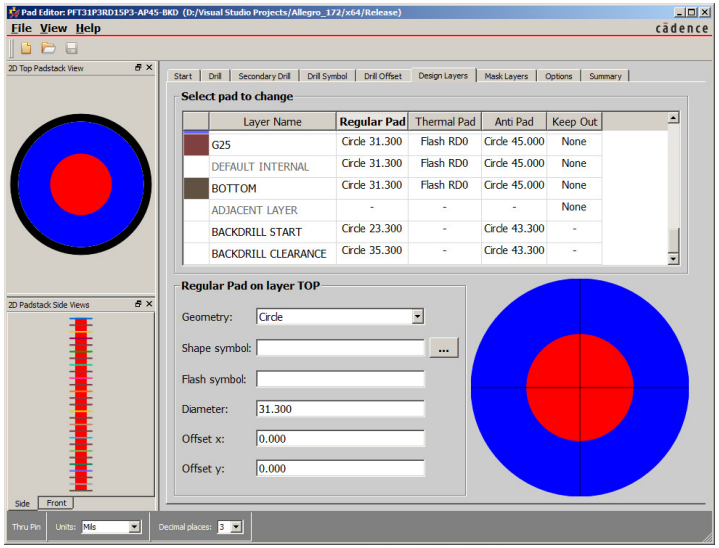
Backdrill
Parameters



Backdrill
Library Driven Flow Model

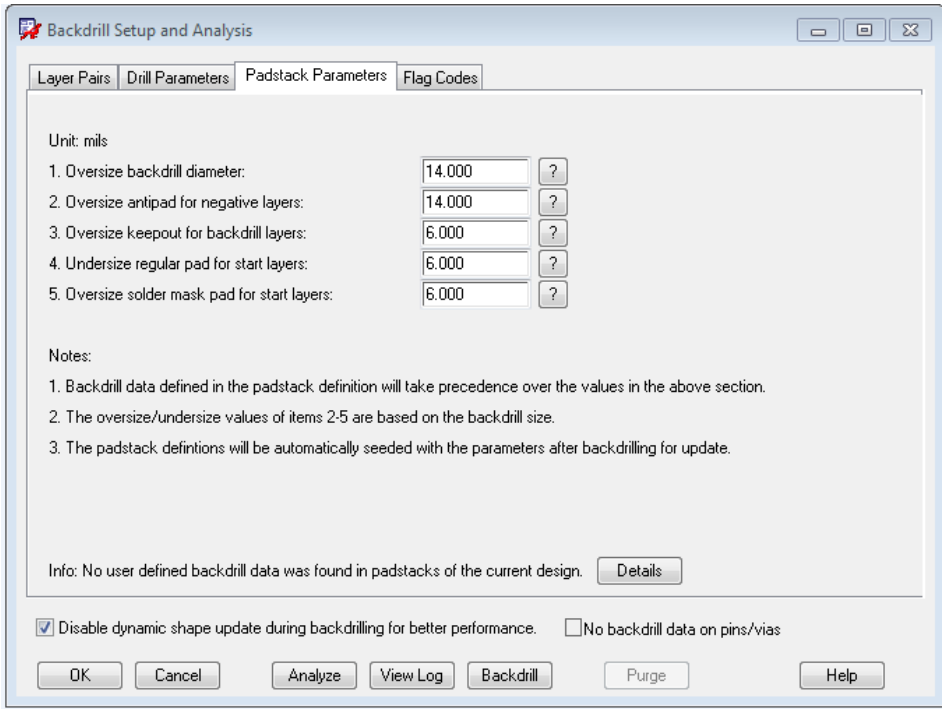
- Pad Definition now supports
  - Backdrill tool diameter
  - Figure & characters for legend
  - Keepout pad
  - Start layer pad/mask
- Backdrill Analysis to replace regular pads with backdrill defined pads/clearances on backdrill path
- Improved Analysis to help make decisions on layer pair strategy





Backdrill
Quick Design Utility Option

- Does not require Library driven data model
- Parameters to oversize backdrill hole, anti-pads, clearance pads on signal layers
- Undersize start layer pad and mask
- Click “Details” to review list of plated padstacks with backdrill info

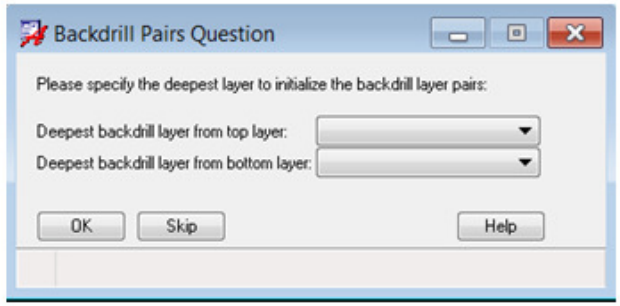


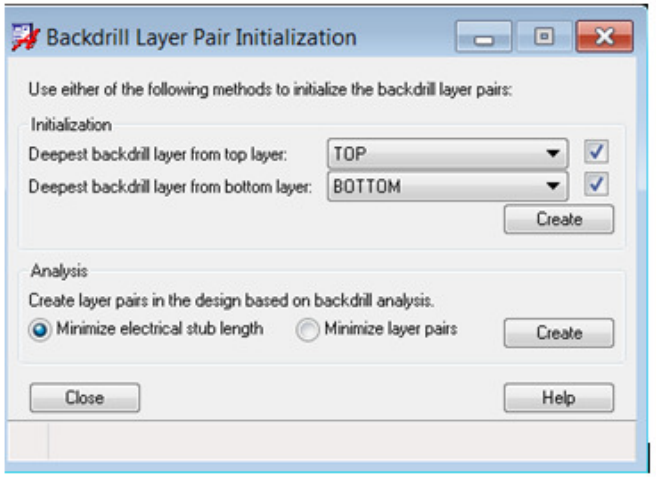
Setup and Analysis

- Setup and Analysis form continues to be the primary interface to setup Layer Pairs (formerly called passes)
- New controls help users determine best strategy based on qualifiers
- **Layer Pair Initialization**

  Choose from three qualifier options:

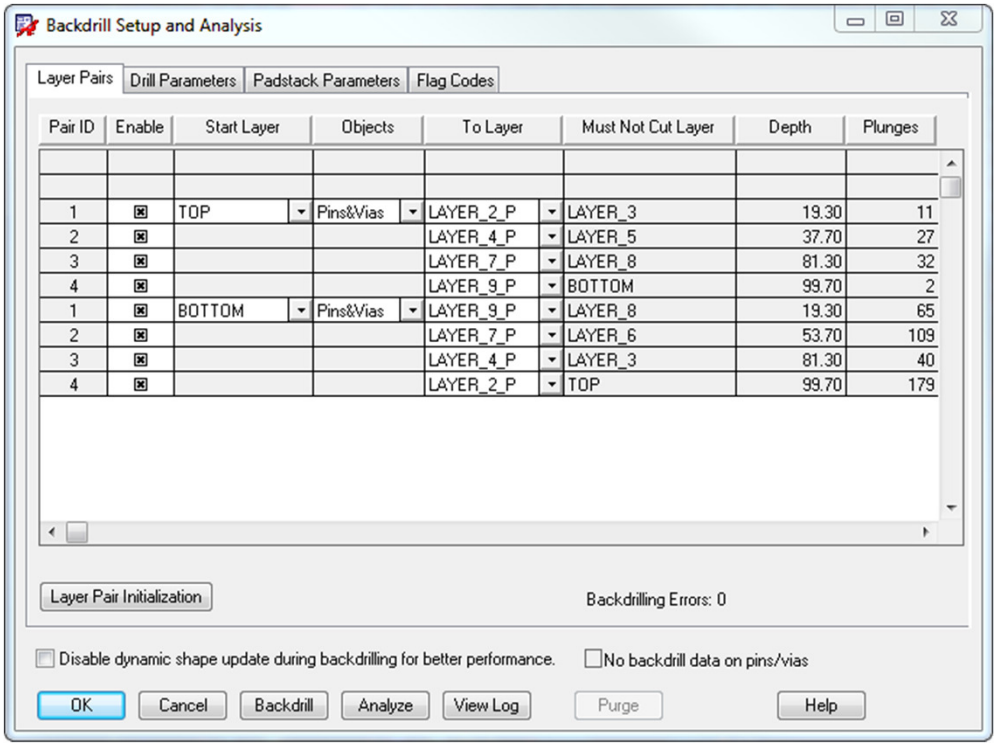
  1. Deepest Backdrill Layer from Top and Bottom Layers (all combinations)
  2. Minimized electrical stub lengths (highest performance, shortest stubs)
  3. Minimize layer pairs (cost efficient, least amount of layer pairs)





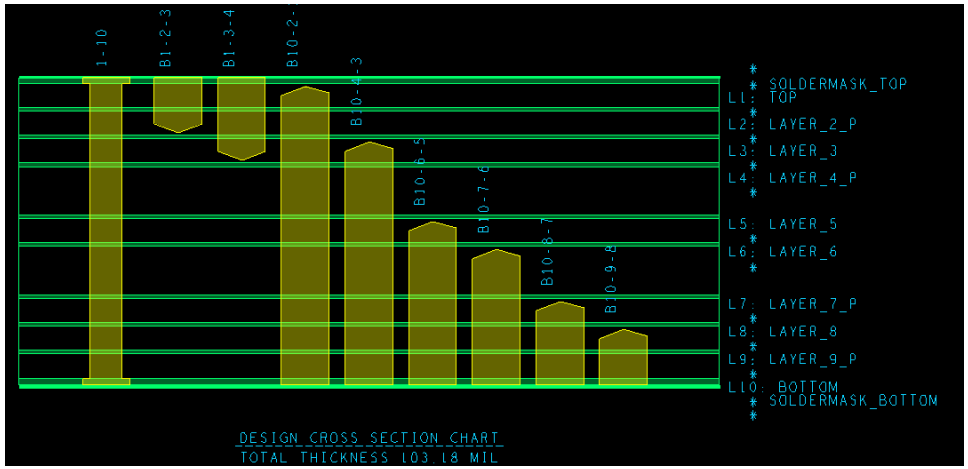
Layer Pairs Tab

- Terminology change
  - Passes (16.x) to Pairs (17.2)
- New Must Not Cut Layer Column
  - Connection Layer
- New Plunges Column
  - Lists backdrill quantity for respective layer pair



Backdrill
Manufacturing Output

- NC Legend Updates
  - Terminology updates
    - Must Not Cut
  - Manufacturing Stub (backoff tolerance)
  - Depth
- Update to Cross Section chart
- IPC-2581



BACKDRILL: BOTTOM to LAYER_4_P

ALL UNITS ARE IN MILS

FIGURE	BD_SIZE	MNC_LAYER	MAX_DEPTH	MFG_STUB	QTY
•	28.0	LAYER_3	81.3	8.0	3

NOTES:
- MNC_LAYER: MUST-NOT-CUT-LAYER
- MAX_DEPTH: DEPTH FROM START LAYER TO THE SURFACE OF MUST-NOT-CUT-LAYER
- MFG_STUB : MANUFACTURING STUB LENGTH

High Speed Routing Applications

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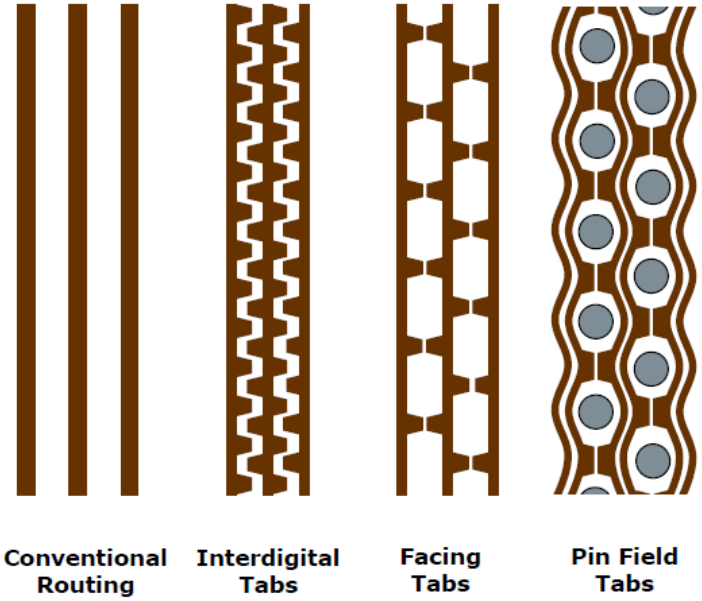
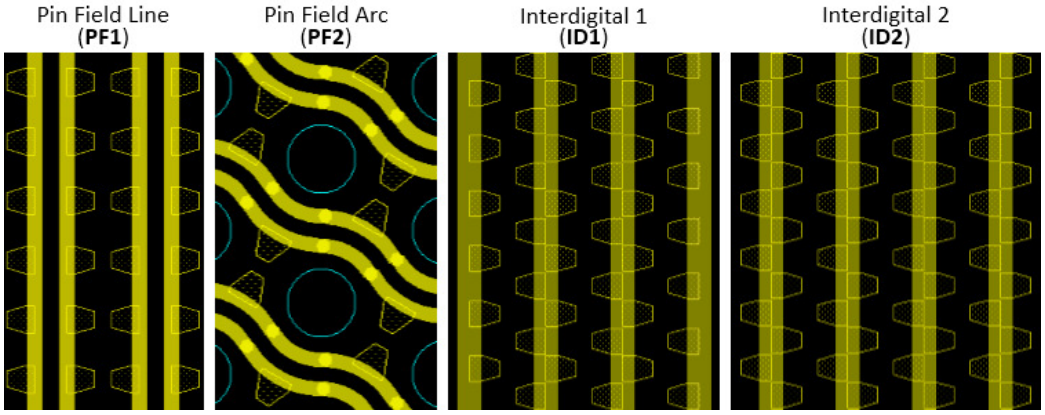
Tabbed Routing

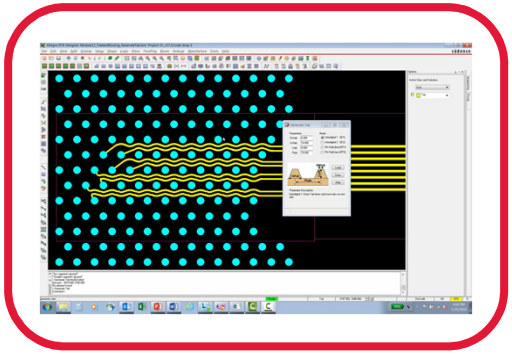
- Tabbed routing is a new customer driven routing strategy
- Trapezoidal shapes (tabs) are added to parallel traces to control impedance in the pin field/breakout region, and Far End Crosstalk in open field region
- Allows longer trace lengths and use of smaller trace spacing
- Available now in 16-6-2015 release
  - Route – Unsupported Prototypes
  - Requires HighSpeed Product Option



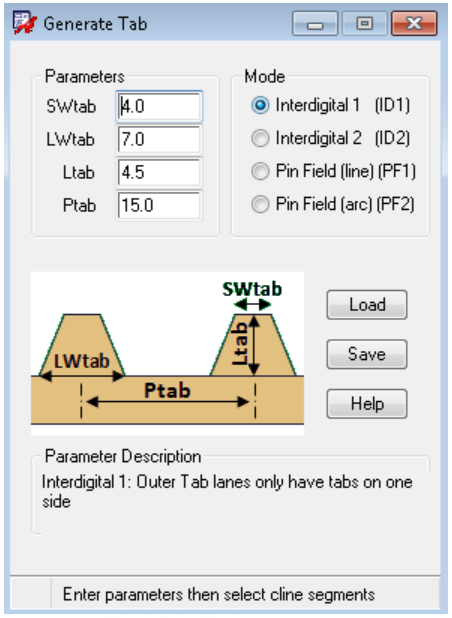
Tabbed Route Generation

- ***Interdigital 1(ID1):***
  - Outer tab lanes only have tabs on one side
- ***Interdigital 2 (ID2):***
  - Both inner and outer tab lanes have tabs on both sides.
- ***Pin Field Line (PF1):***
  - Used in CPU pin field breakout region. These are tabs directly opposing each other between two track routing lines
- ***Pin Field Arc (PF2):***
  - Used in CPU pin field region with arc routing. These are tabs directly opposing each other between two track routing lines.



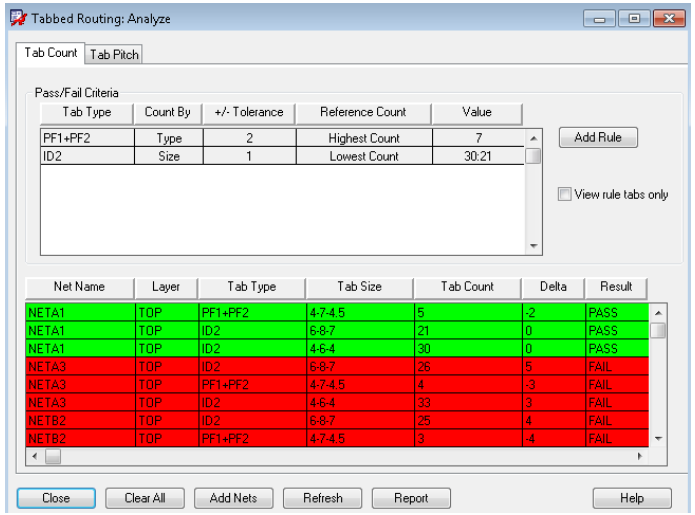


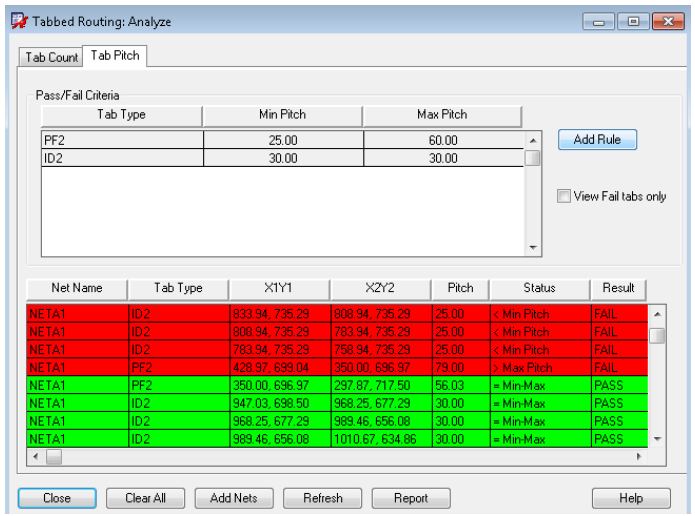
Movie



Tabbed Route Analysis

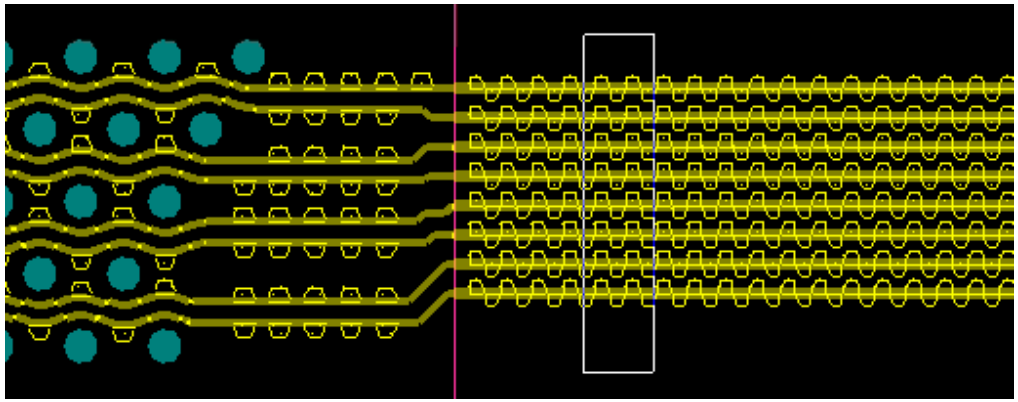
- Validate Tab count and pitch
- Create custom rules for pass/fail criteria
- Cross Probe to location in Canvas
- Generate custom tab count and pitch reports

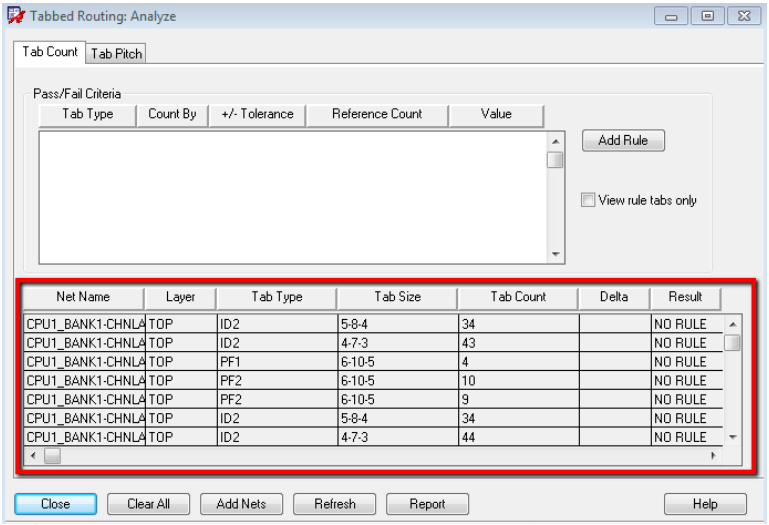




Tab Count Validation

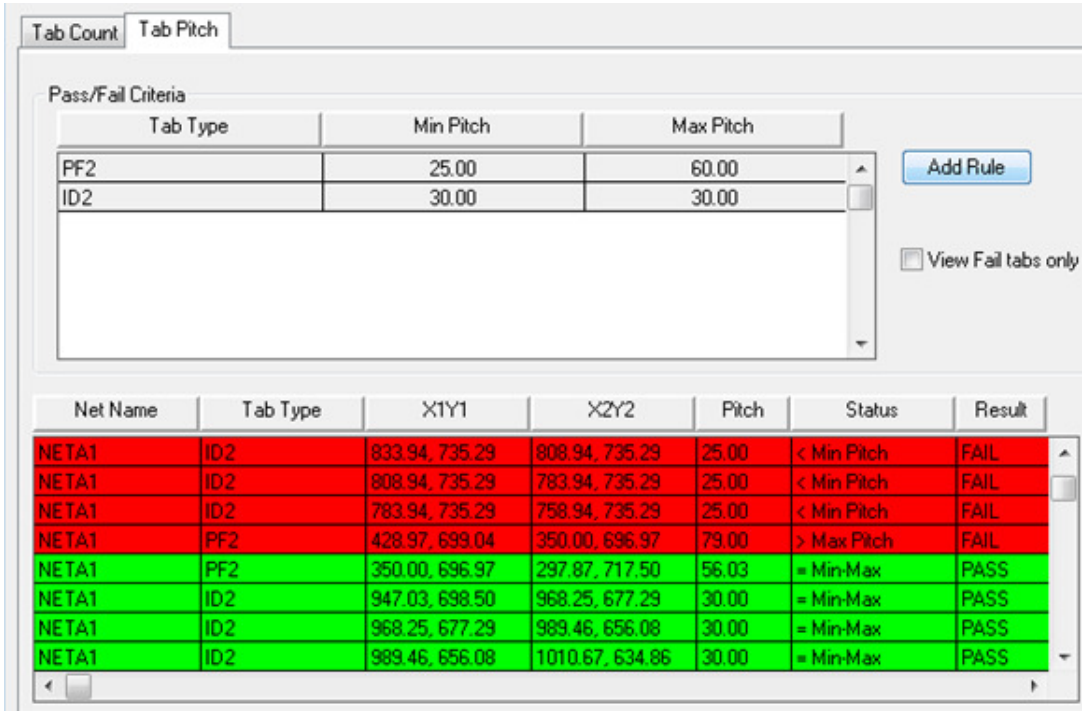
- Checks tab count difference between bits in same byte
  - Not more than 1 or 2 to maintain same flight time and achieve crosstalk cancellation
- Checks that tabs are added to the correct layers
  - By using the Layer Column, users can check that tabs are on the correct layer for selected nets (i.e. Tabs applied to external layers only)
- Checks that tab sizes used are correct and the same for each type
  - By using the Tab Size Column, users can check if different tab sizes are used for each tab type on same net (Different tab sizes are listed for each net and tab type)





Tab Pitch Validation

- Check if Min and Max Tab Pitch Requirements are met for each tab type
- Detect Overlapping tabs



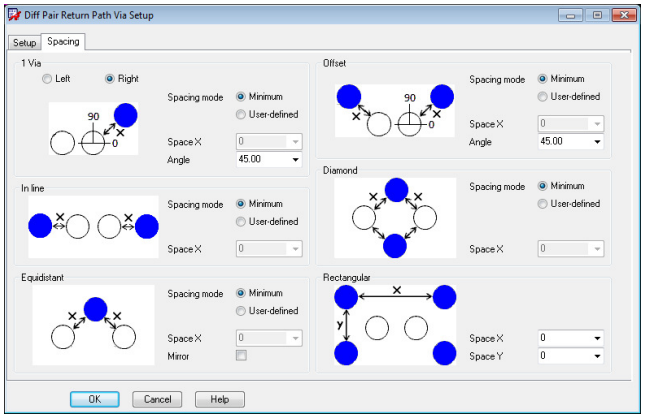
Add Connect Return Path Vias

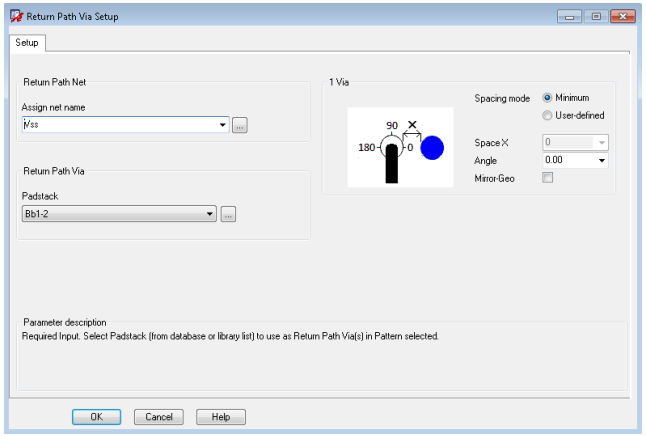
16.6

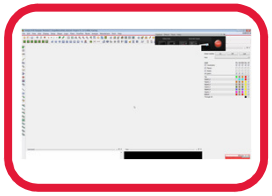
- Differential Pair Support Only
  - Released in 16.6 2015 as new prototype feature
  - Placement of return path vias during diff pair route
  - Provided 6 commonly used patterns
  - Slide differential pair and return path vias together
  - Included limited Via Structure support (target use case: stacked blind-buried return path vias)

17.2

- Differential Pair and Single Net Support
  - Expanded to support Single Net High Speed Via Transitions
  - Removed Via Structure support.
  - Use 17.2 Via Structures
  - Added additional Mirror Options for differential pair pattern offset and 1 Via.



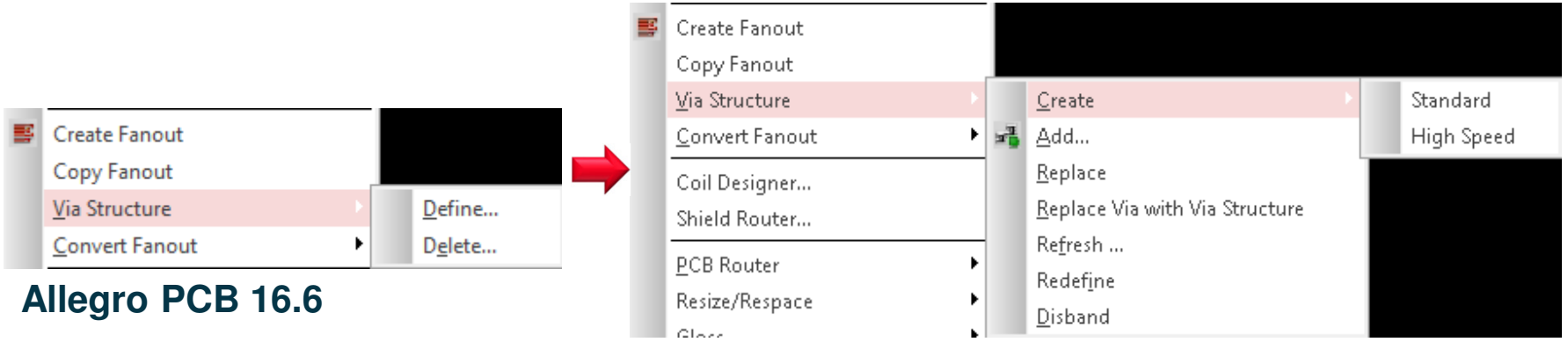




Movie

Routing Enhancements
Via Structures

- Cadence Allegro PCB Via Structure now has the same Via Structure use model as Cadence SiP
  - No longer limited for use with Create Fanout in Allegro PCB
  - New to Allegro PCB: *Create, Add, Replace, Replace Via with Via Structure, Redefine, Refresh and Disband* Via Structure Commands



Allegro PCB 16.6

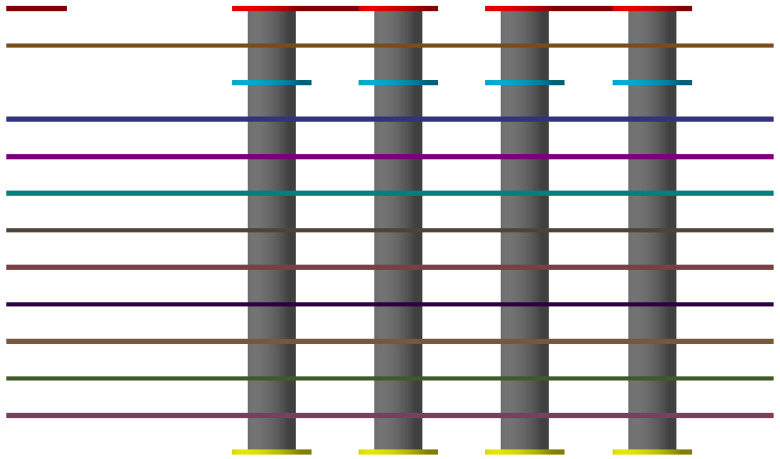
New

  - Via Structures are defined as Symbols in database
  - Supports Import and Export of XML files containing Via Structure Definition

Via Structure Commands
Standard

Current SiP Via Structure

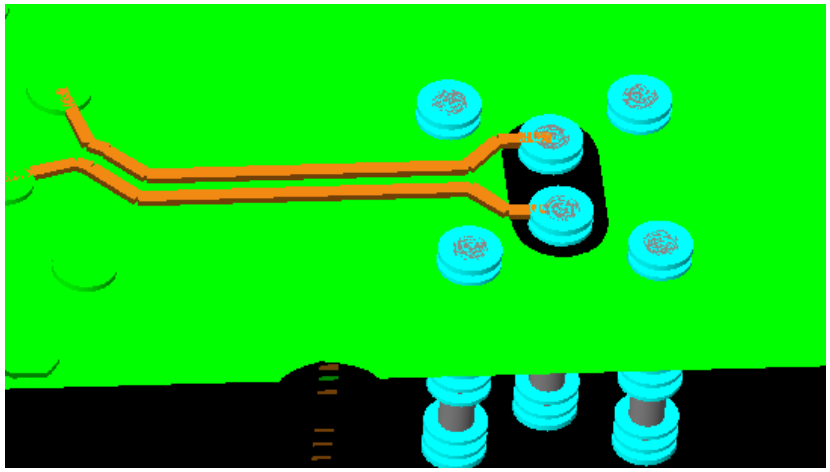
- Target Use Model:
  - Simple single net trace/via structures
  - Fan-out
- Supported Objects
  - Traces, Vias
  - Need to be physically connected (single net)
- Enhancements for 17.2
  - Supports Arced Traces
  - Supports new 17.2 Pad Changes (i.e. back drill, counter bore/sink, pad shapes, adjacent keep out)
- Unencrypted XML
- No special license required

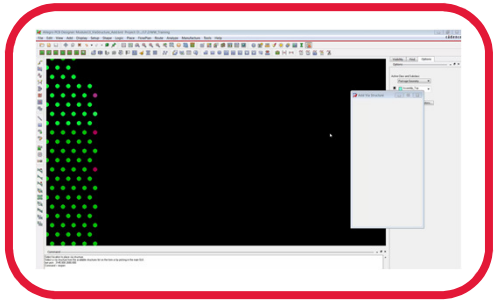


Via Structure Commands
High Speed

New High Speed Via Structure

- Target Use Model:
  - High Speed Via Transitions with Return Path Vias and custom voids
  - **Integration with Sigrity**
- Supported Objects
  - Traces, Vias, ***Static Shapes, Route Keep out***.
  - ***Multi net***
  - Supports arced traces and new 17.2 Pad Changes (i.e. back drill, counter bore/sink, pad shapes, adjacent keep out)
- Encrypted XML
- High Speed Option/ SiP XL license required





Movie

Constraint Manager Updates

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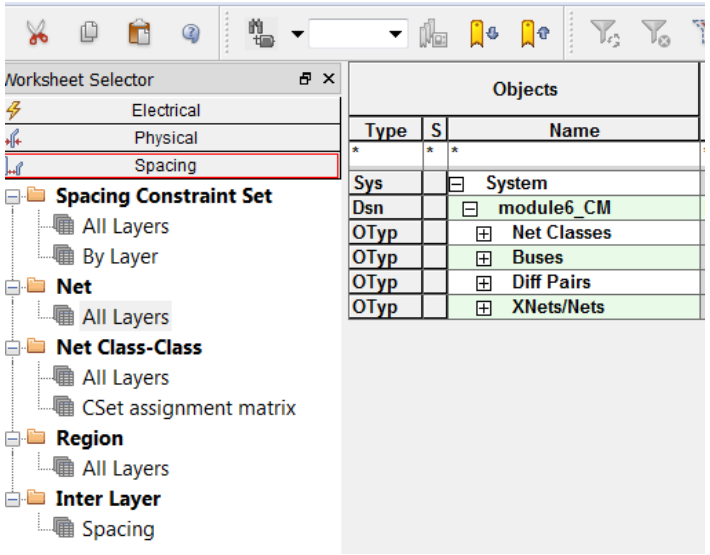
Constraint Manager
Data Compression

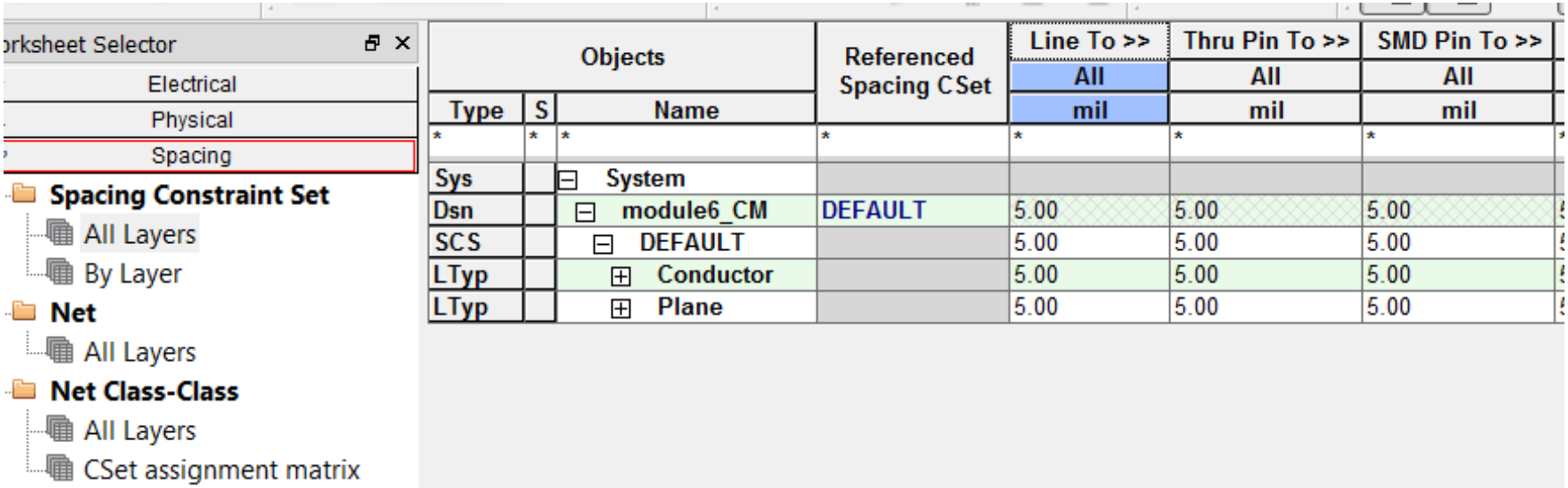
- Efforts made to reduce the amount of data in the User Interface
- Customers say “Too much data in my face, difficult to manage”
- Objects now default to higher level “Object Type” categories (Net Class, Diff Pair, Xnets/Nets)
- Constraint Types collapsed
  - Click >> to expand



Line To >>	Thru Pin To >>	SMD Pin To >>	Test Pin To >>	Thru Via To >>	BB Via To >>	Microvia To >>
All	All	All	All	All	All	All
mil	mil	mil	mil	mil	mil	mil
*	*	*	*	*	*	*
5.00	5.00	5.00	5.00	5.00	5.00	5.00

Constraint Manager
Data Compression

- Constraint Sets (CSets) default to Layer Type categories
  - Conductor
  - Plane
- Effective when all layers of that category have similar constraint values
- Reduction of 30-50 rows possible (varies by stackup)



New “ALL” Super Attribute

- Super attribute “All” created for each constraint category
- Controls all <object>-to-<all other object type> spacing values within that constraint category
  - “Line To All” column is the super attribute for all LINE_TO_<object type> spacing constraints
- “All” Cell will display, ***, if any related constraint values are different

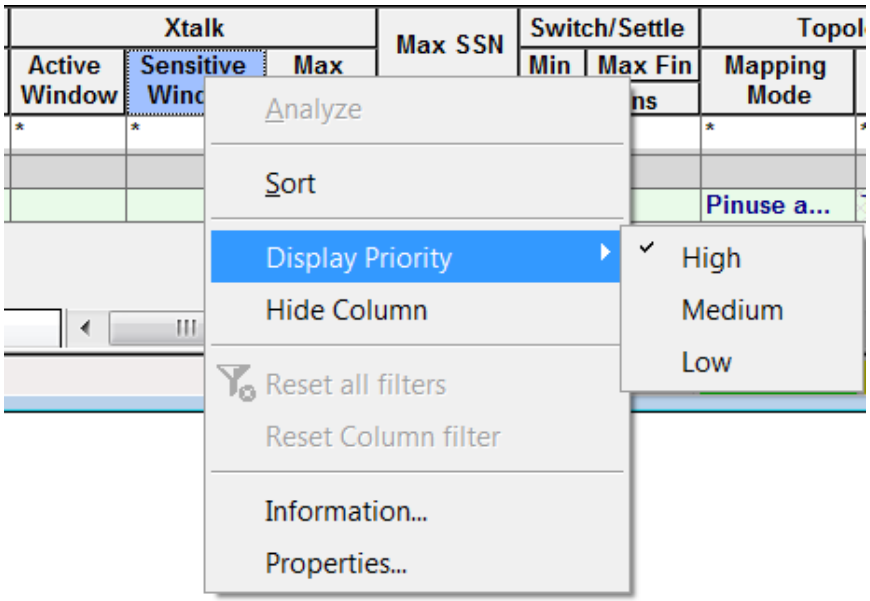
Objects			Referenced Spacing CSet	Line To >>
				All
Type	S	Name		mil
*	*	*	*	*
Sys		System		
Dsn		module6_CM	DEFAULT	5.00
SCS		DEFAULT		5.00
LTyp		Conductor		5.00
LTyp		Plane		5.00
SCS		12MIL		12.00

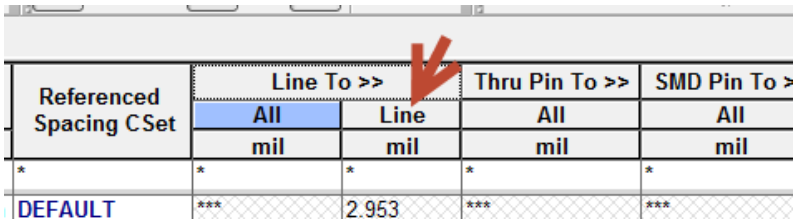
Set here
Apply Range

Objects			Referenced Spacing CSet	Line To >>											
				All	Line	Thru Pin	SMD Pin	Test Pin	Thru Via	B Via	Test Via	Microvia	Shape	Bond Finger	Hole
Type	S	Name		mil	mil	mil	mil	mil	mil	mil	mil	mil	mil	mil	mil
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Sys		System													
Dsn		module6_CM	DEFAULT	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00
SCS		DEFAULT		5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00
LTyp		Conductor		5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00
LTyp		Plane		5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00
SCS		12MIL		12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00
LTyp		Conductor		12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00
LTyp		Plane		12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00

Show Less/More
Column Display Priority

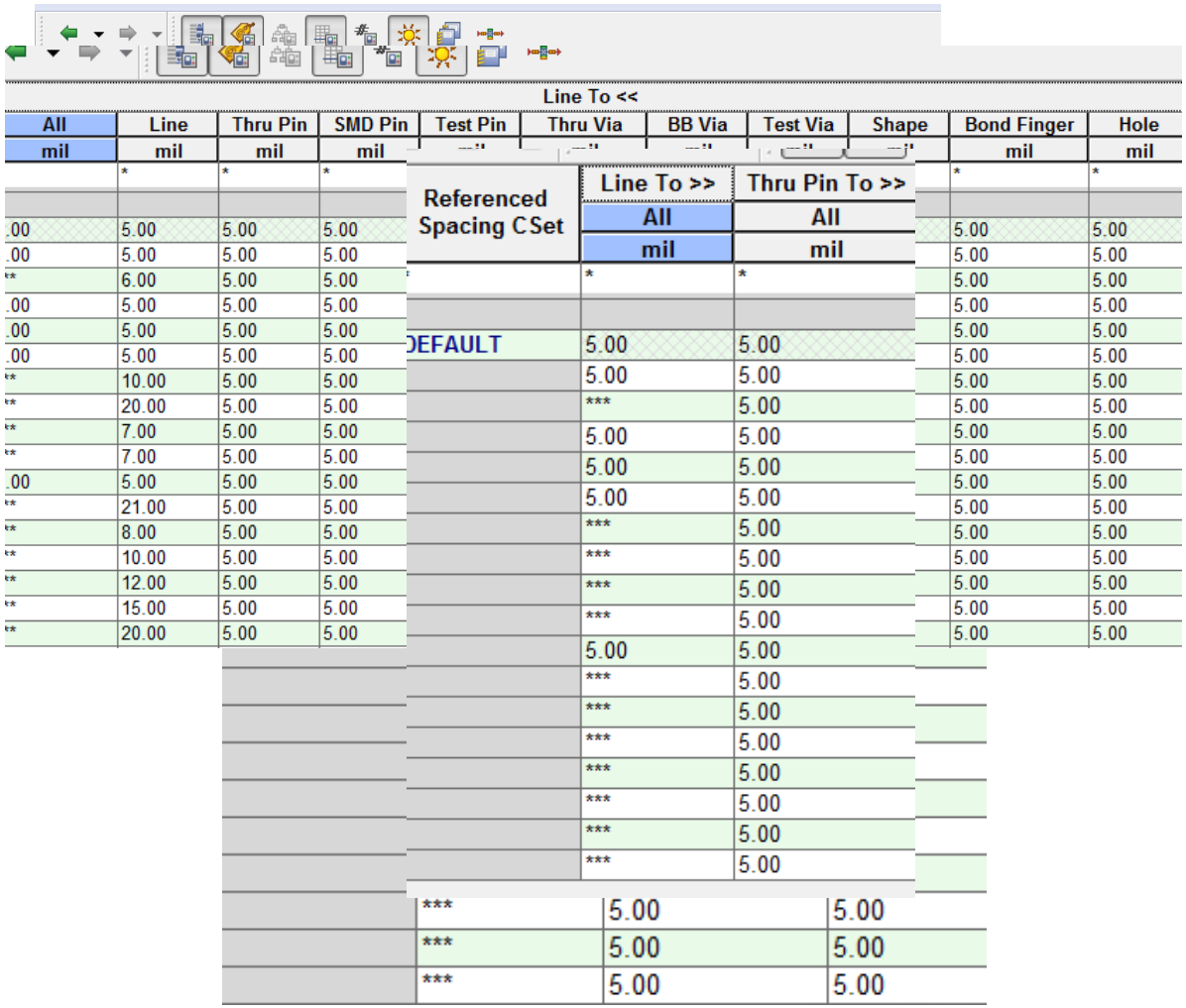
- High, Medium, or Low settings control: less ➔ more
- Display Priority can be set for any column header
- If columns have different priorities then “>>” or ”<<“ may be doubled-clicked in the column header to display more or less
- Stack-up Editor and Spacing Worksheets will utilize display priorities





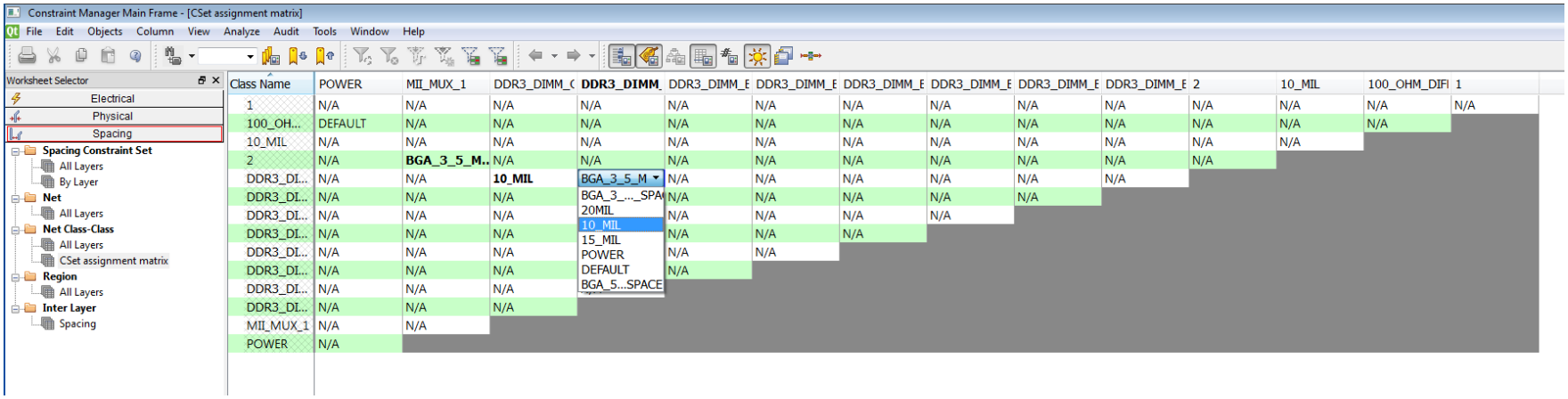
Display Priority Example
Lower Bondfinger Priority

- Hover over Bondfinger then RMB – Display Priority
- Select “Low”
- Double Click Line to >>
- Column expands, Bond Finger is Hidden
- Double Click >> again and Bond Finger Appears
- Double Click << to reset to default settings



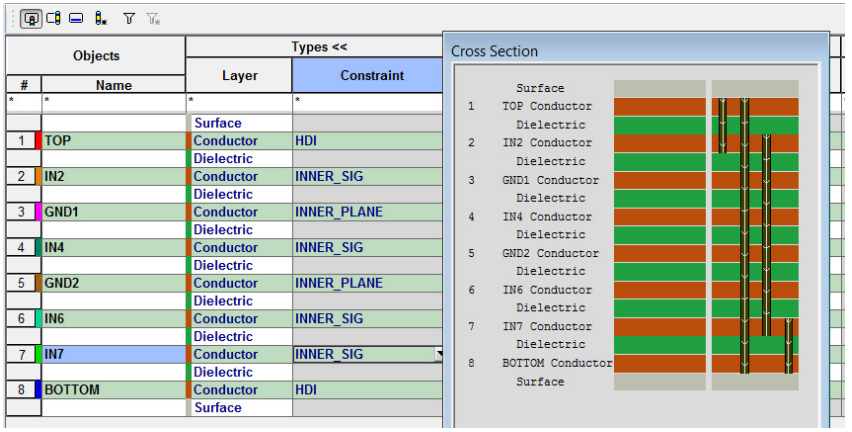
Constraint Manager
Class to Class Matrix

- Simple Matrix to manage Net Class Relationships
- Legacy model seen as confusing and redundant
- Dropdown supports list of Spacing Csets

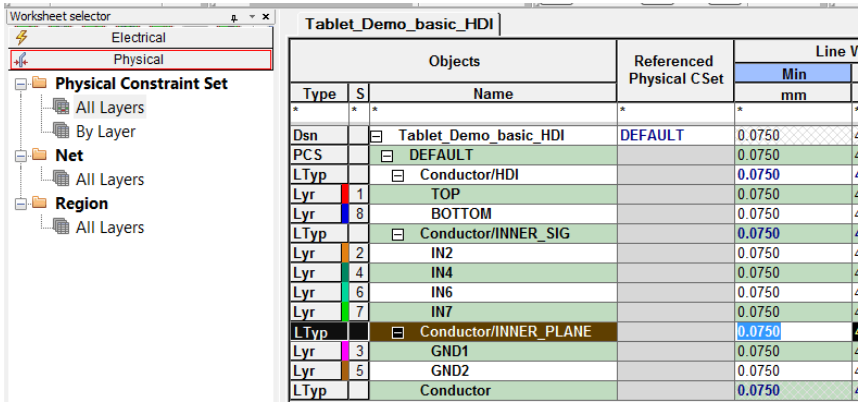


Generic Techfiles

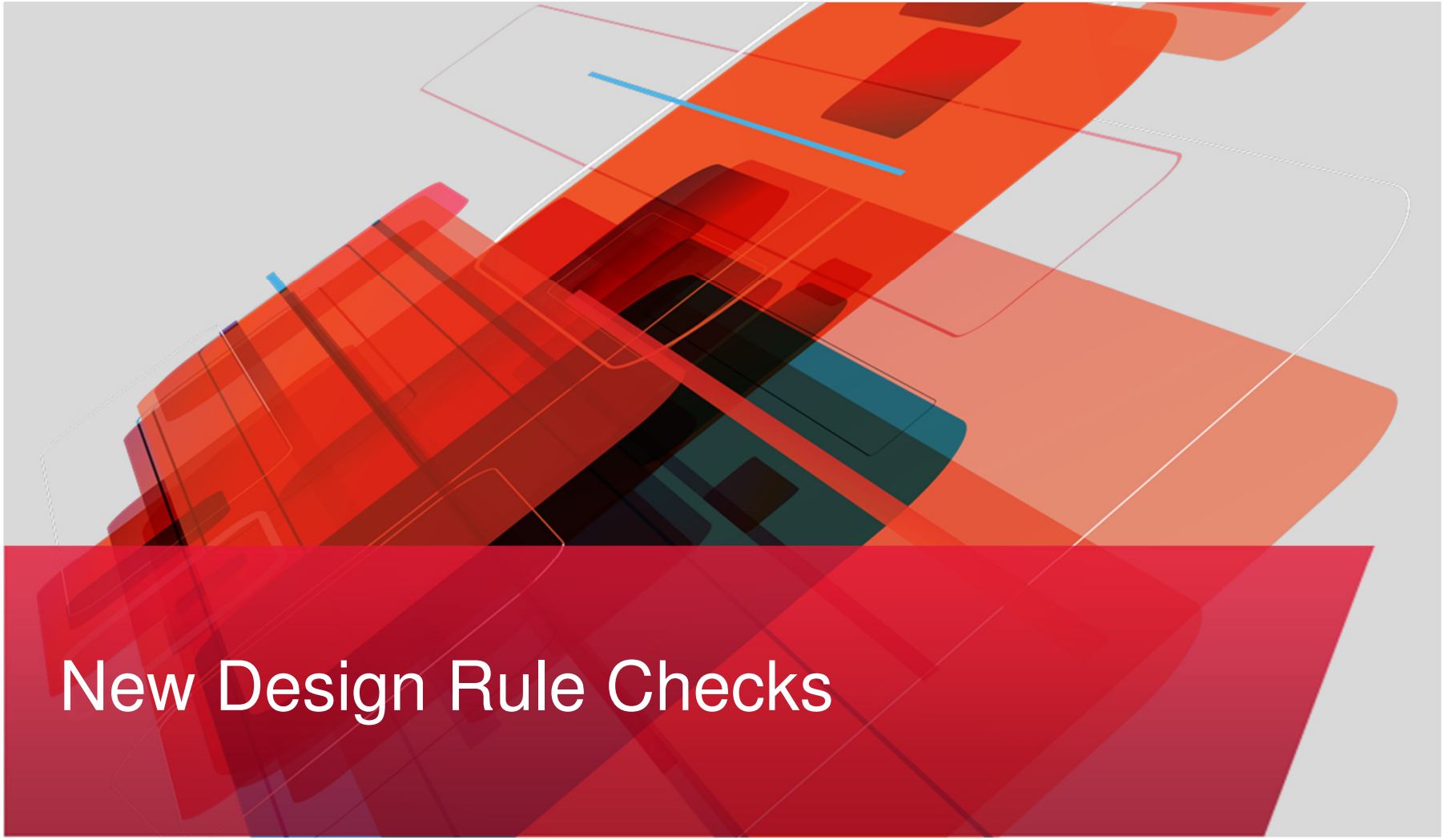
- Generic Tech Files (16.6)
  - Generic Tech Files introduced in 16.6.
  - Allows constraints to be mapped to hierarchical layer names
    - Top, Internal_Signal, Internal_Plane, Bottom
  - Promotes a “stackup independent” tech file flow
  - Same tech file could be used on 4, 8, or 32 layer PCBs
- 17.2 Update (Increased Flexibility)
  - New “Constraint” column in Cross Section Editor provides opportunity for creation of custom “Layer Types”
    - HDI, Core, 100 Ohm, VCC, GND, etc.
  - In CM, assign constraints at Layer Type (parent) level
    - Constraints inherited by “child” layers



17.2 Cross Section UI



Physical Cset Layer Types



New Design Rule Checks

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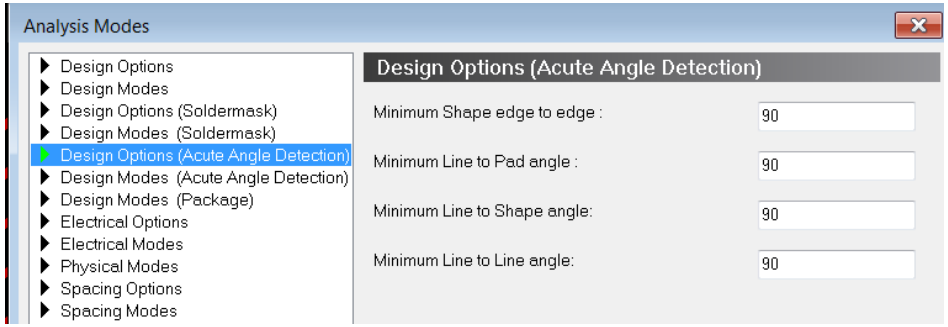
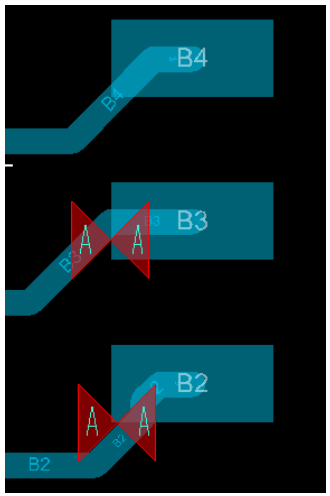
Acute Angle DRC

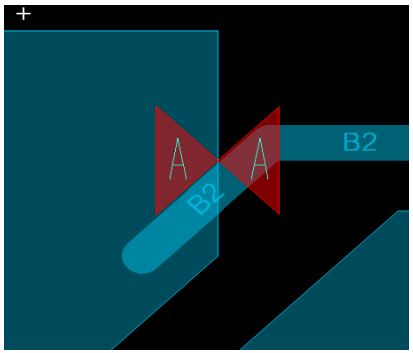
- Four variations of checks
  - Line to Pad
  - Line to Shape
  - Shape Edge to Edge
  - Line to Line



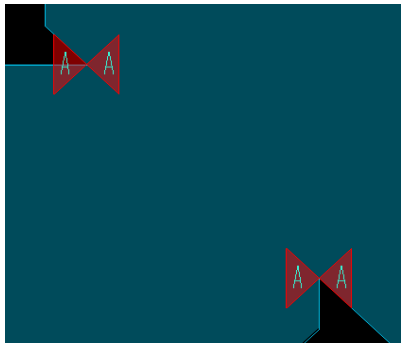
- Default angle set to 90 but user definable



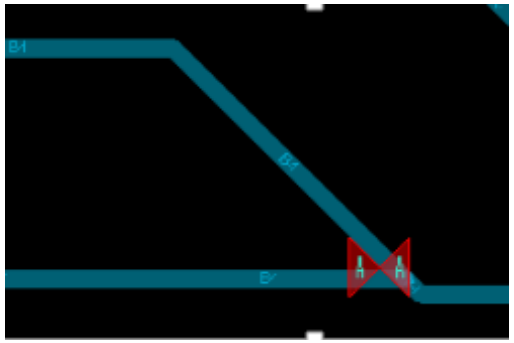
Line to Pad



Line to Shape



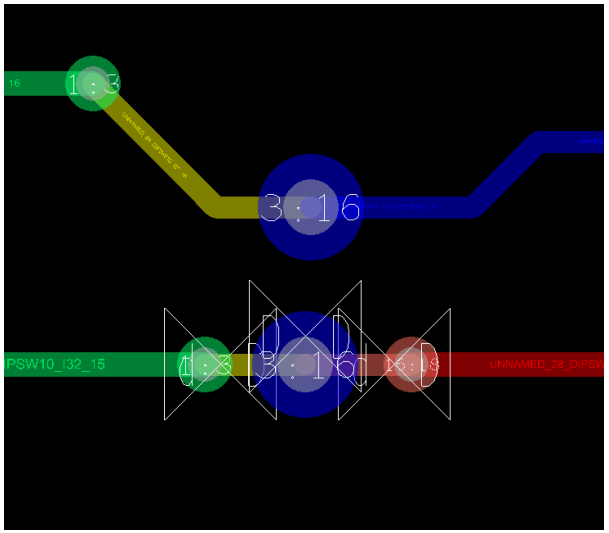
Shape Edge to Shape Edge

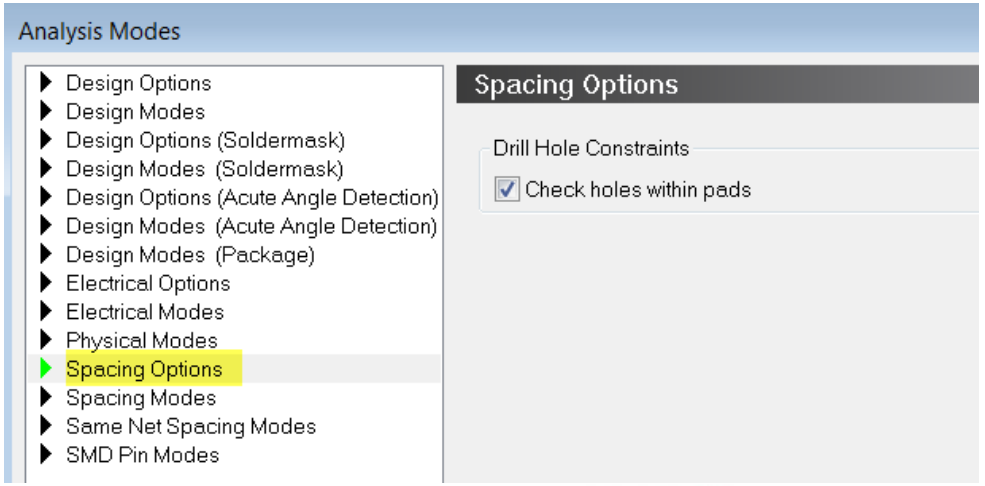


Line to Line

Drill Hole DRC

- Introduced in 16.2
  - To support unused pad suppression
- Now can check to holes with, or without pads
- New Spacing Options added to Analysis Modes
  - **ON** = Drill-hole checks are run whether or not pads are present (Pad size not relevant in DRC calculation).
  - **OFF** = Drill-hole checks are run only when pads are not present (Default configuration)





Miscellaneous Productivity Features

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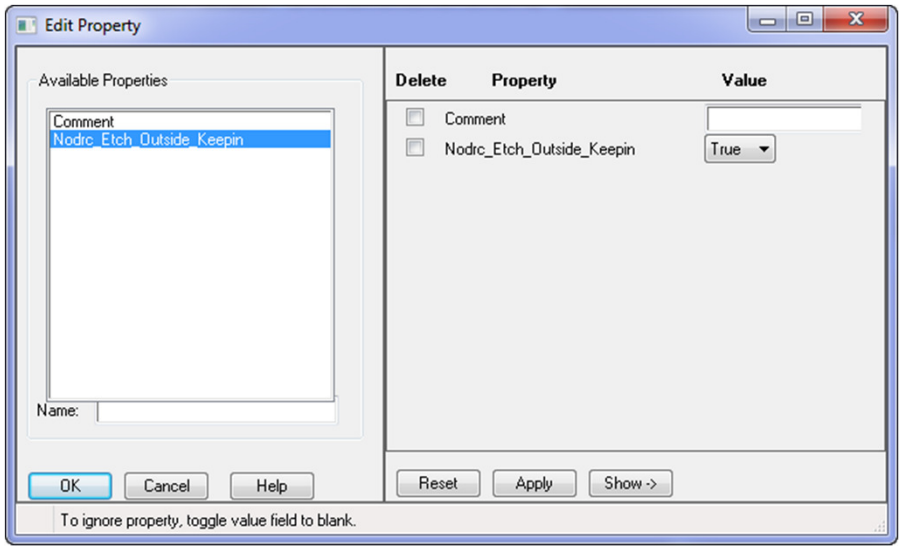
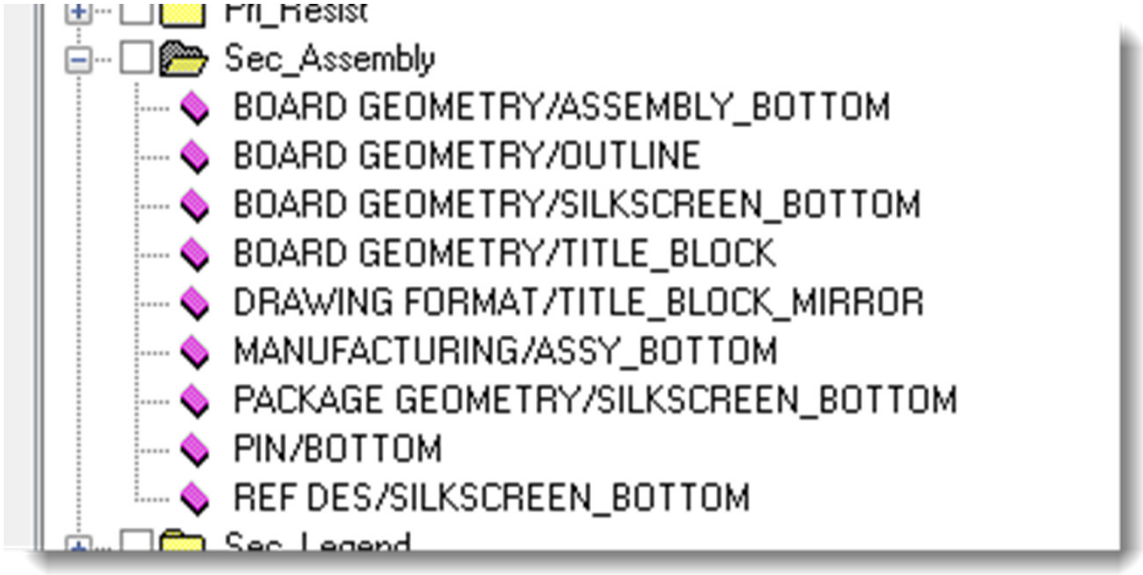
Text

- Nodrc_Etch_Outside_Keepin
  - This property has been enhanced to include Text elements
  - Previous to V17.2 this property was only applicable to etched lines
- Comment
  - Text has been enhanced with the ability to add user defined properties
  - Example: Assigning the layer name the text resides on. This would then make it easier for designers to locate specific text



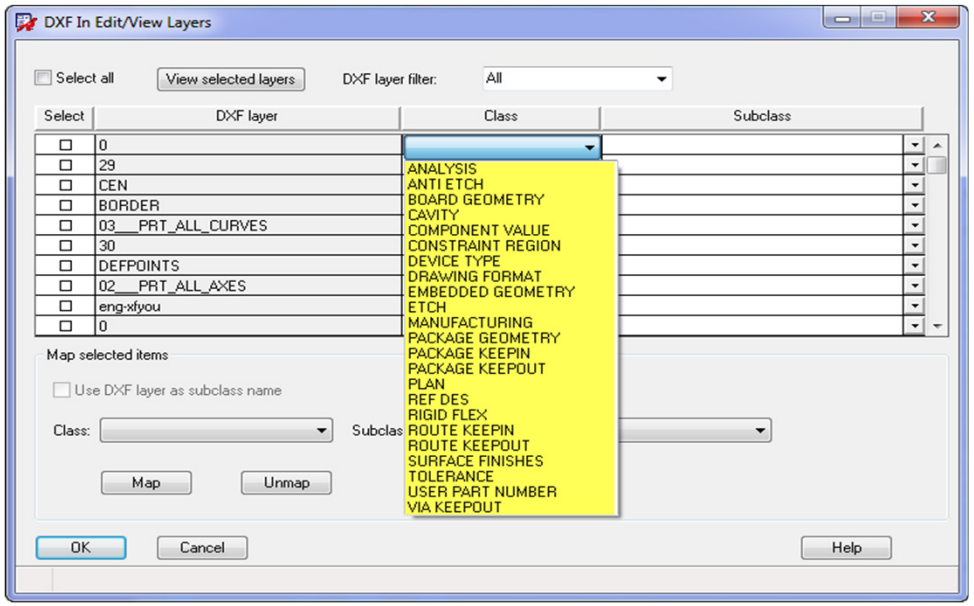
Film Elements Sorted Alphabetically

- Elements (Class/Subclass layers) that make up a Gerber film layer are now sorted alphabetically as shown below



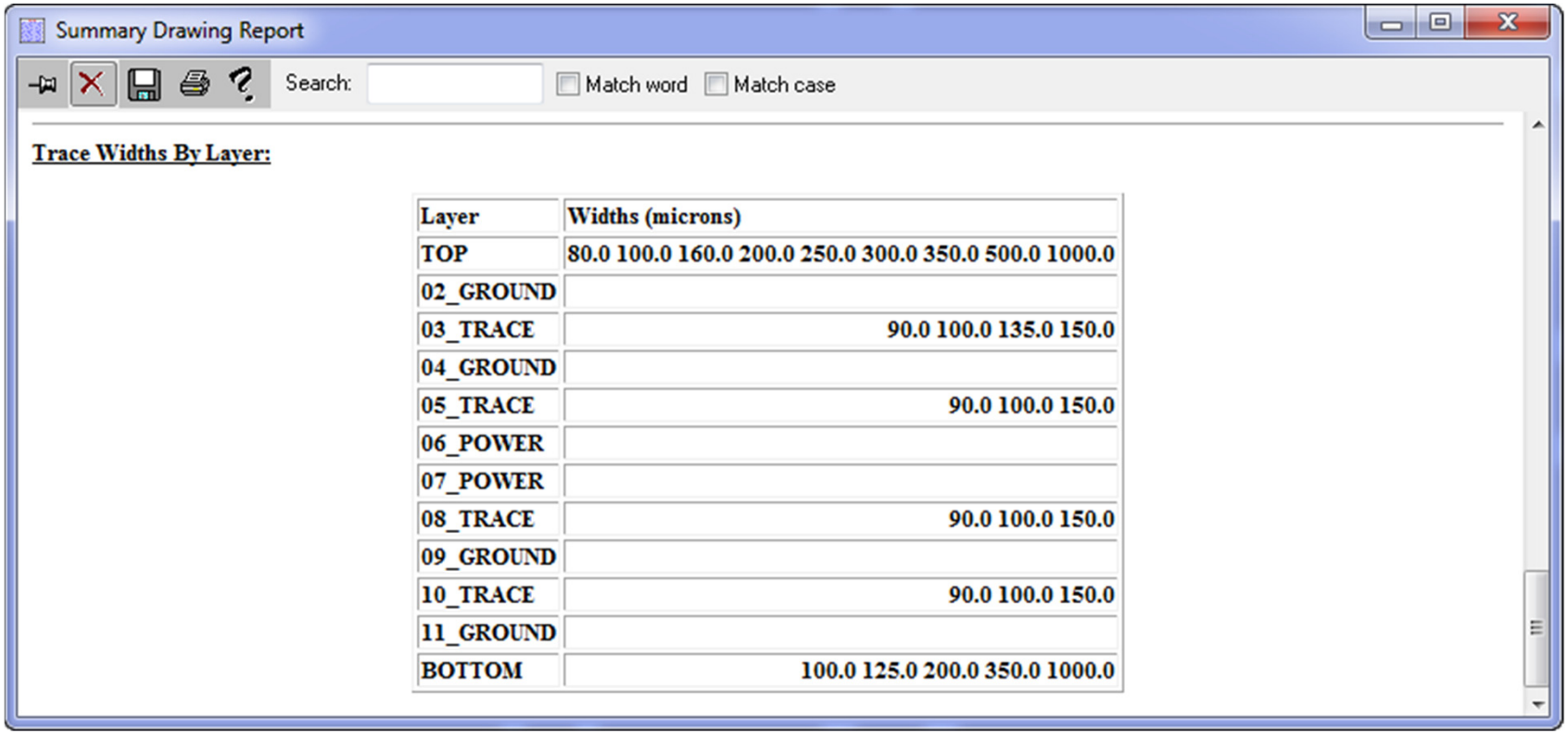
DXF In
Alphabetical Sorting

- Class and Subclass names in the DXF In dialog are now alphabetized for easier locating



Summary Drawing Report

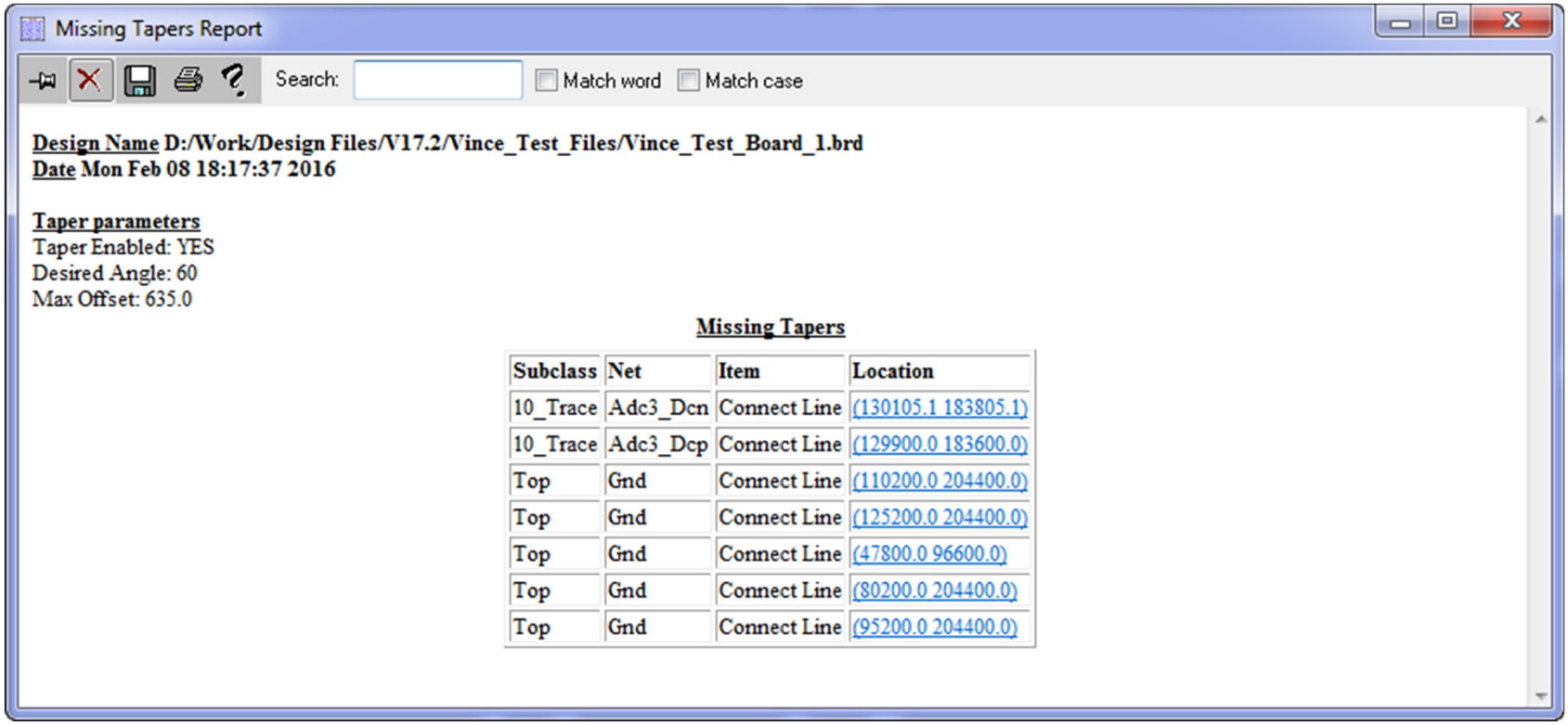
- The Summary Drawing Report now contains a new section showing “Trace Widths by Layer”



Layer	Widths (microns)
TOP	80.0 100.0 160.0 200.0 250.0 300.0 350.0 500.0 1000.0
02_GROUND	
03_TRACE	90.0 100.0 135.0 150.0
04_GROUND	
05_TRACE	90.0 100.0 150.0
06_POWER	
07_POWER	
08_TRACE	90.0 100.0 150.0
09_GROUND	
10_TRACE	90.0 100.0 150.0
11_GROUND	
BOTTOM	100.0 125.0 200.0 350.0 1000.0

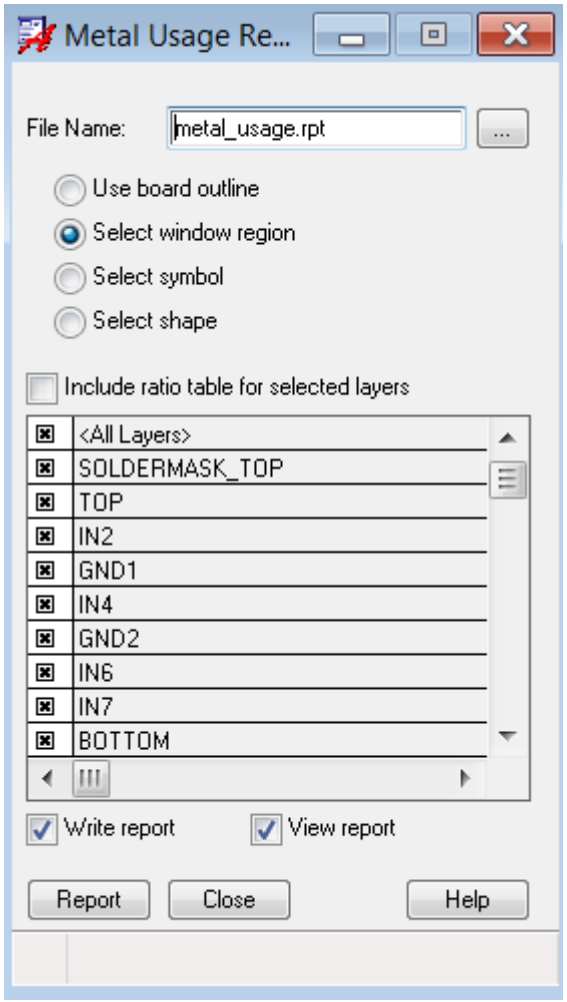
Missing Tapers Report

- In Quick Report, along with the existing Missing Fillets Report, we have now added Missing Tapers Report to ensure smooth trace width transitions



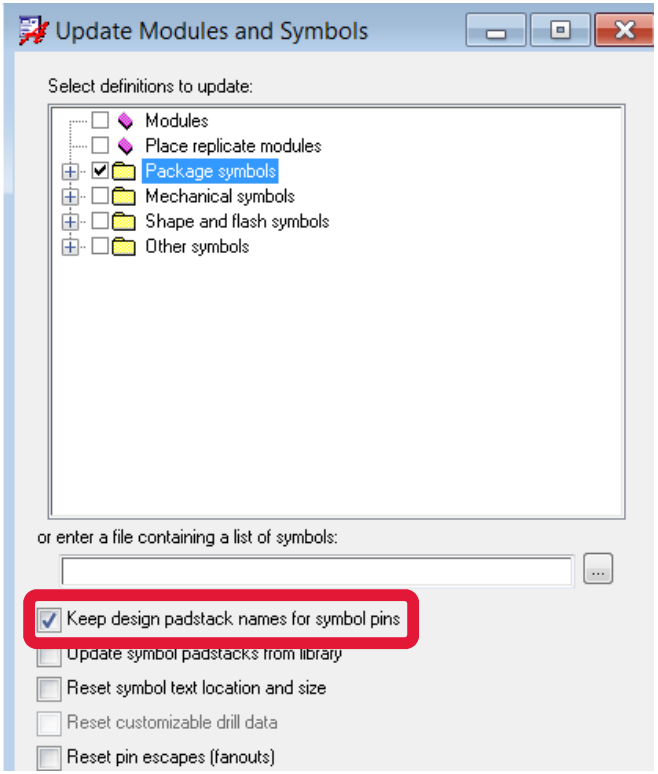
Metal Usage Report

- The APD/SiP based Metal Usage Report is now available in the PCB Editor
- *Tools > Metal Usage Report…*



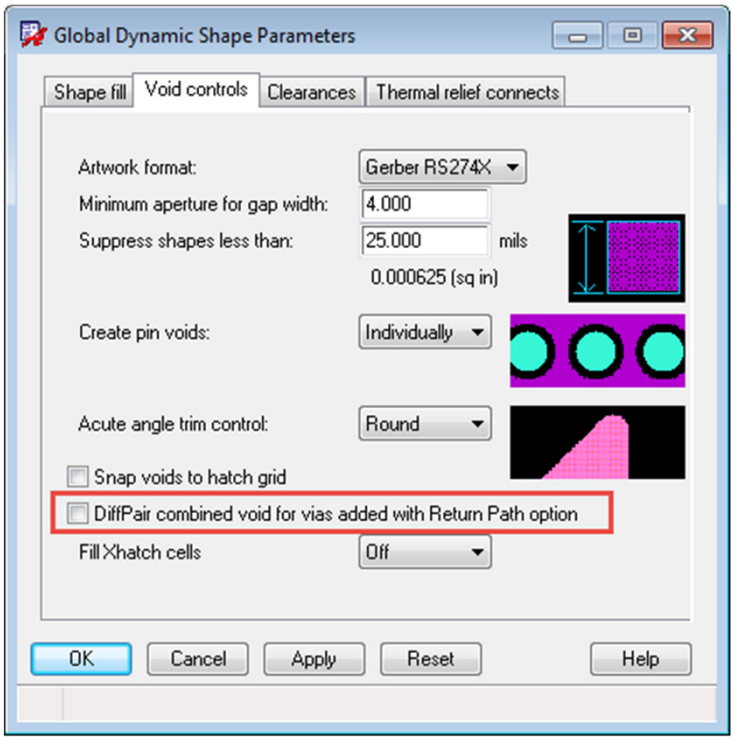
Refresh Symbol Update

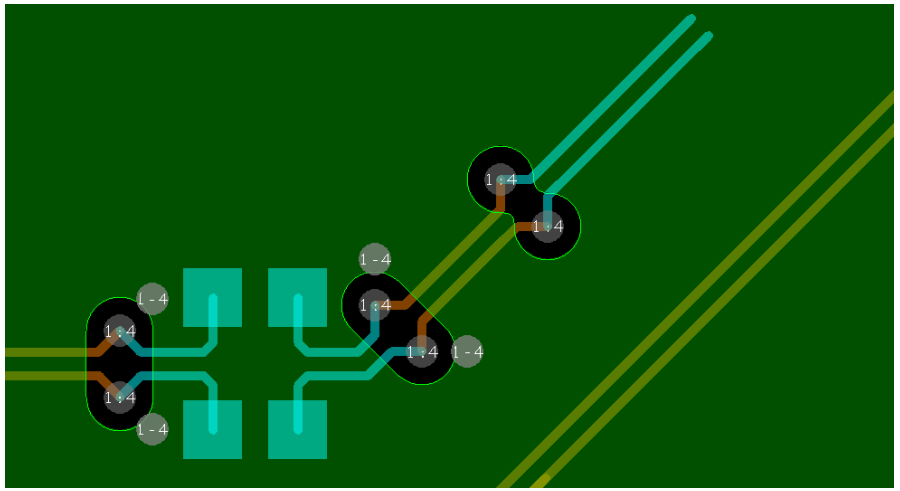
- A new “refresh symbol” option is available to maintain design edited padstacks
- Option is “Keep design padstack names for symbol pins”
- Supported by using the –K option when running the command in batch



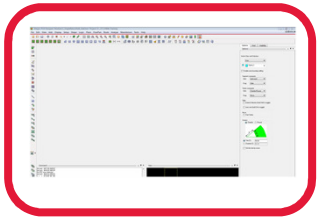
Differential Pair Via Voiding

- The shape parameter form now supports an option to merge differential pair vias into a single entity
- Works in conjunction with Return Path Vias (add connect option)
- Positive Planes Only





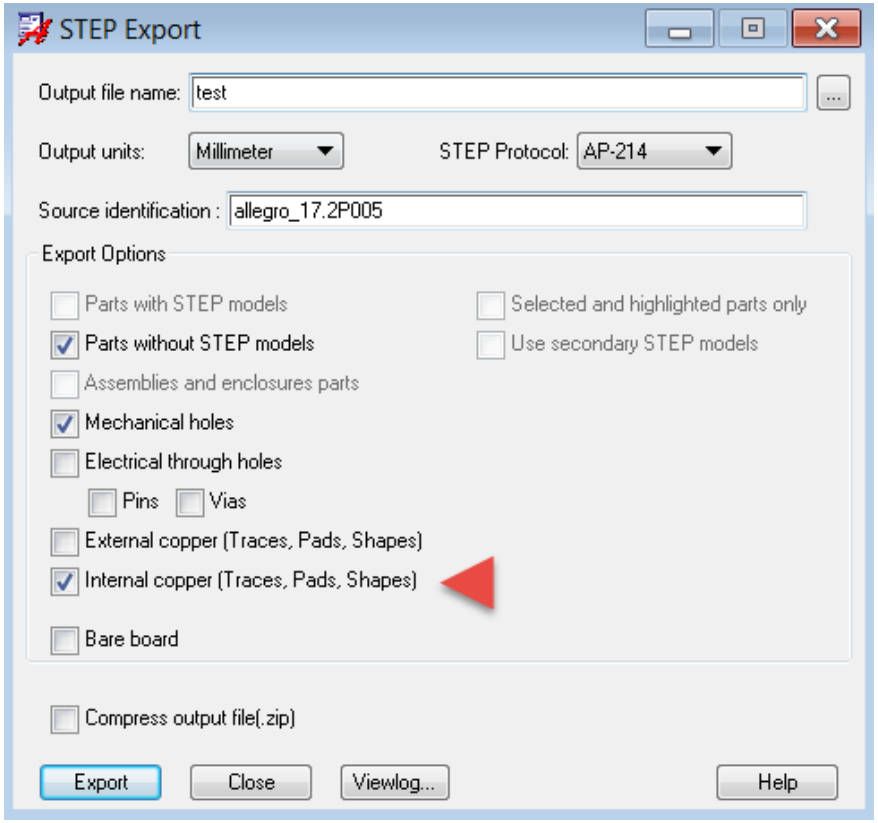
Single Oblong Void Default Behavior

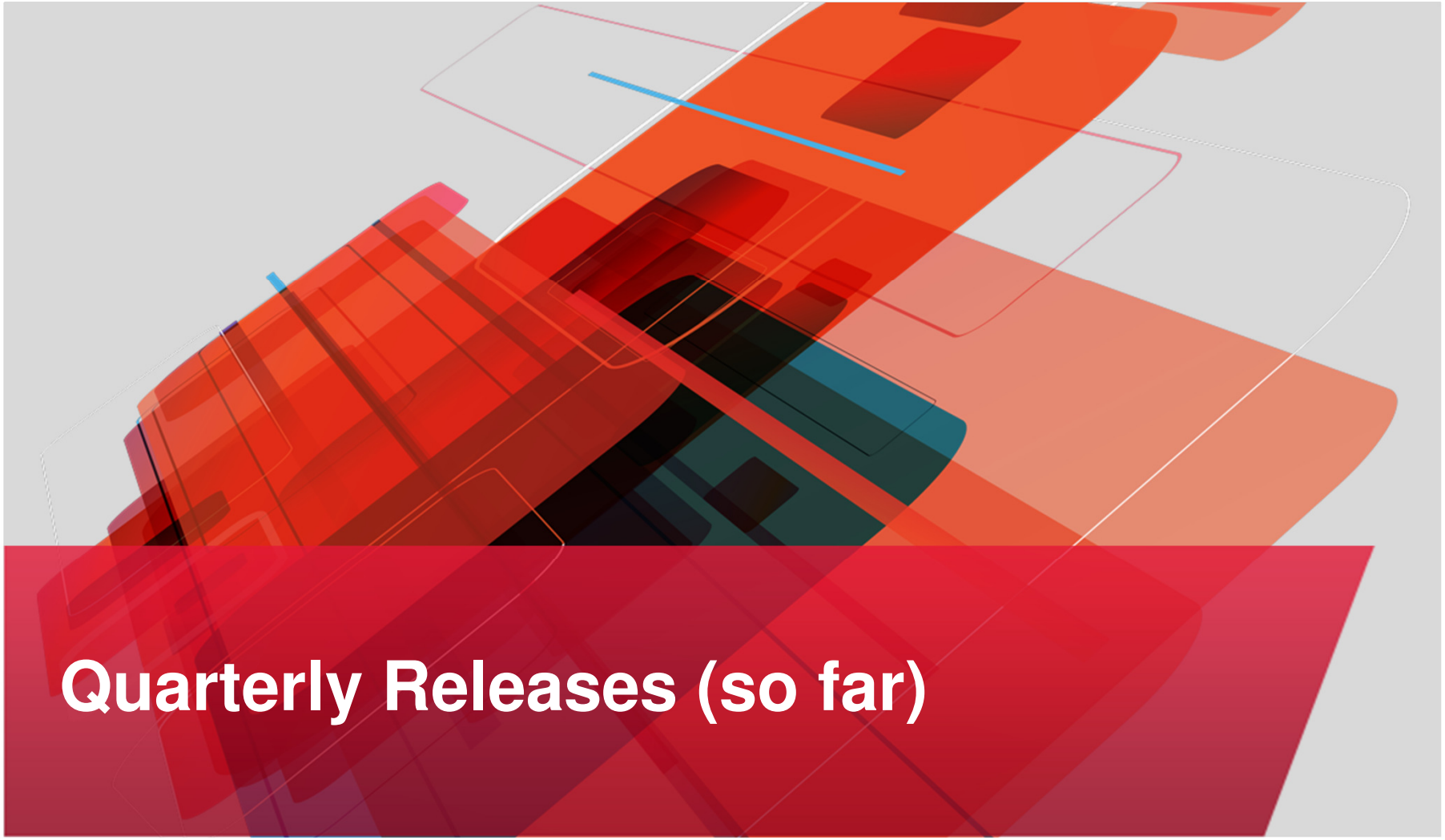


Movie

Step File Export

- New “Internal Copper” option
- File sizes may be much larger





Quarterly Releases (so far)

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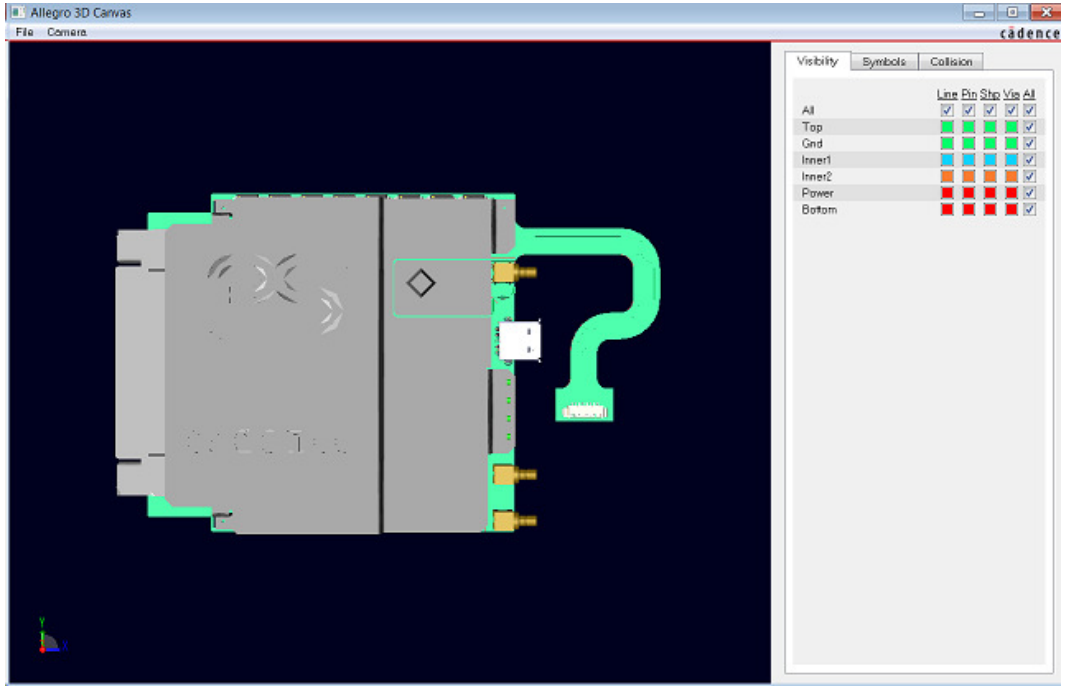
New 3D Interactive Canvas *(Unsupported Prototype)*

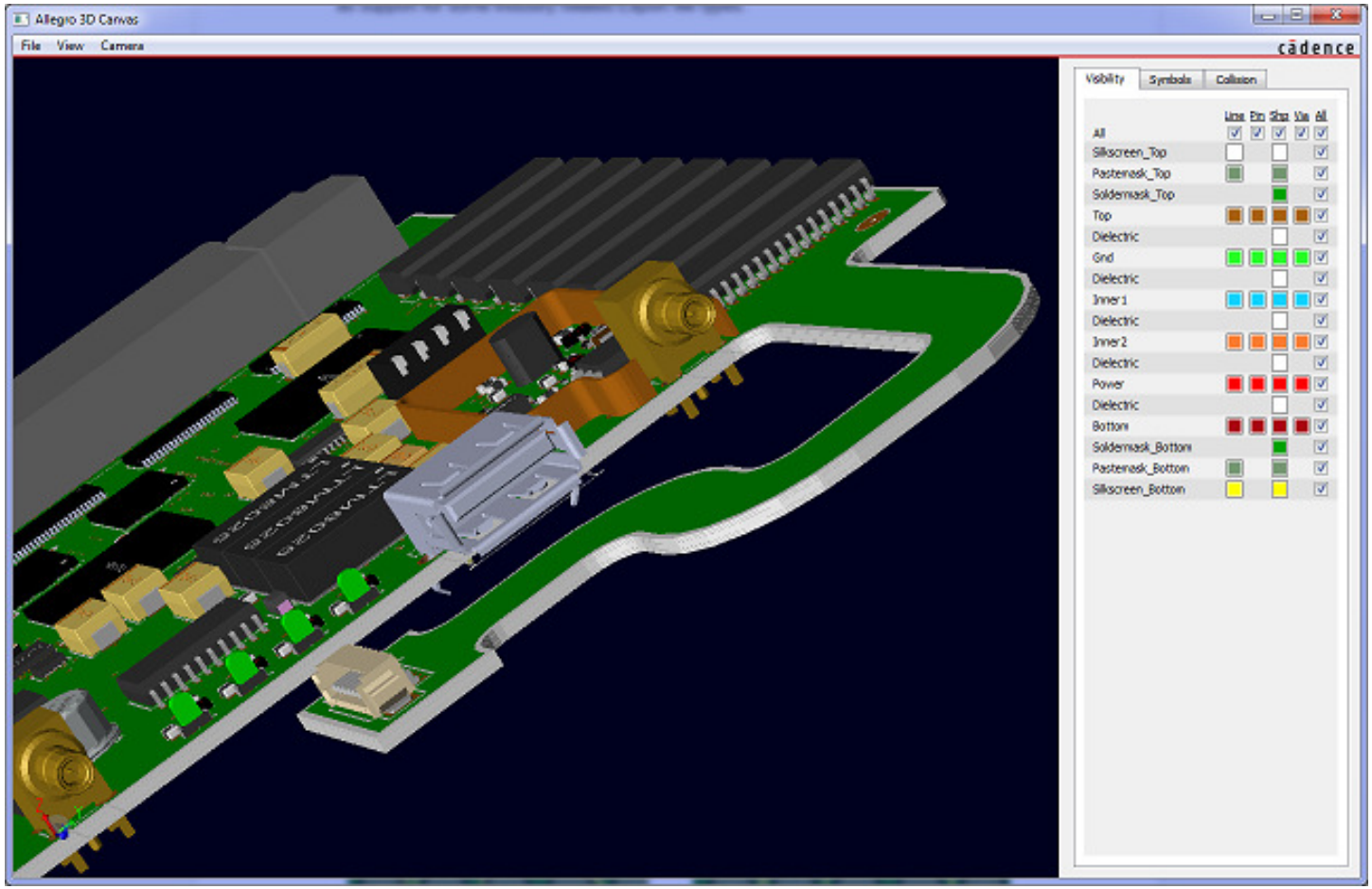
Three New Option Panes

- Visibility – Controls Line, Pin, Shape, Via
- Symbols – Controls Step Model or Placebound
- Collision – Checks Spacing between components



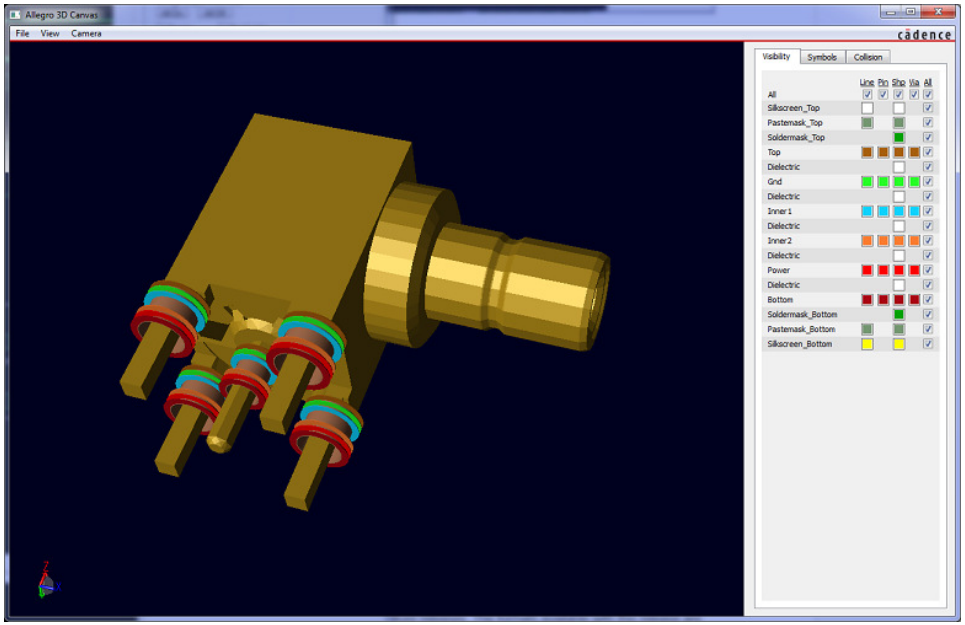
New 3D Interactive Canvas *(Unsupported Prototype)*

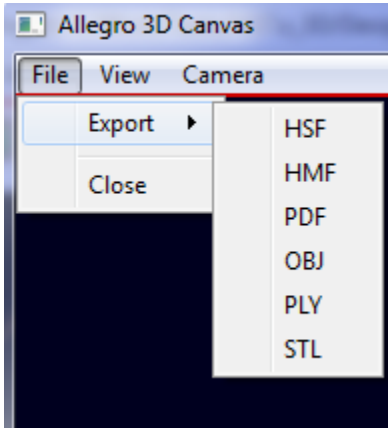
- Full Layer Modeling of Mask, Silk and Dielectric Layers



New 3D Interactive Canvas *(Unsupported Prototype)*

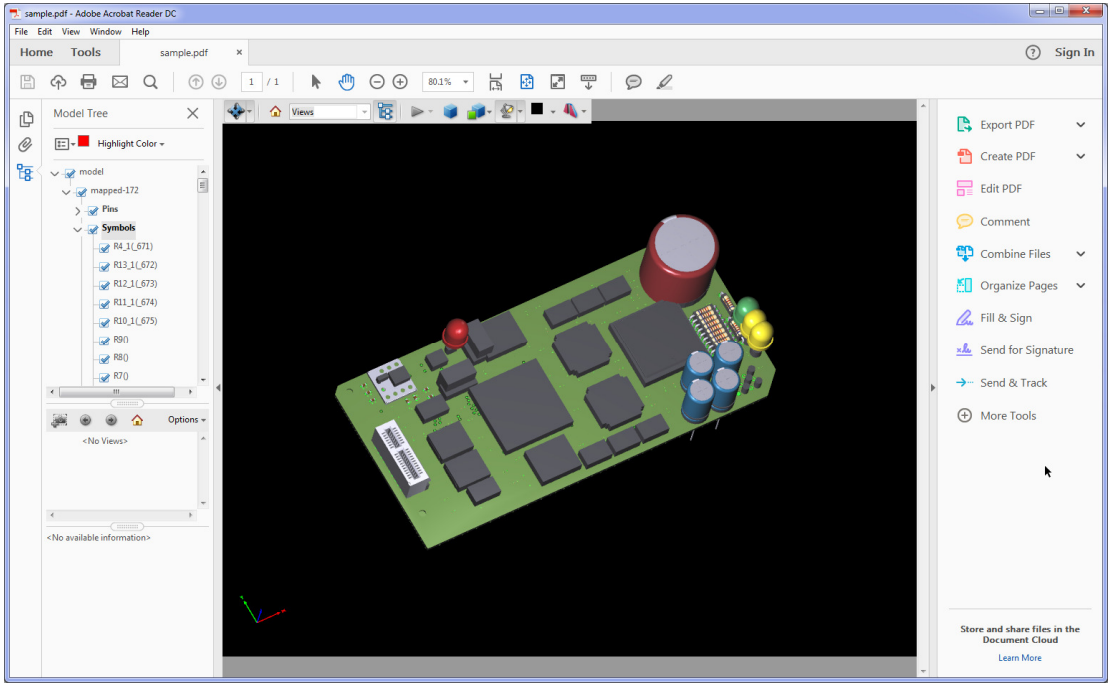
- 2D > 3D Interaction
  - Elements, moved, highlighted, added, deleted in 2D editor show in 3D Canvas in real time.
- Object or Window Select
  - Elements selected in 2D editor may be viewed in 3D canvas.
- File Export
  - HSF – Hoop Steam File
  - HMF – Hoops Metadata File
  - OBJ – Wavefront Format
  - PLY – Polygon File Format
  - STL - STereolLithography





New 3D Interactive Canvas *(Unsupported Prototype)*

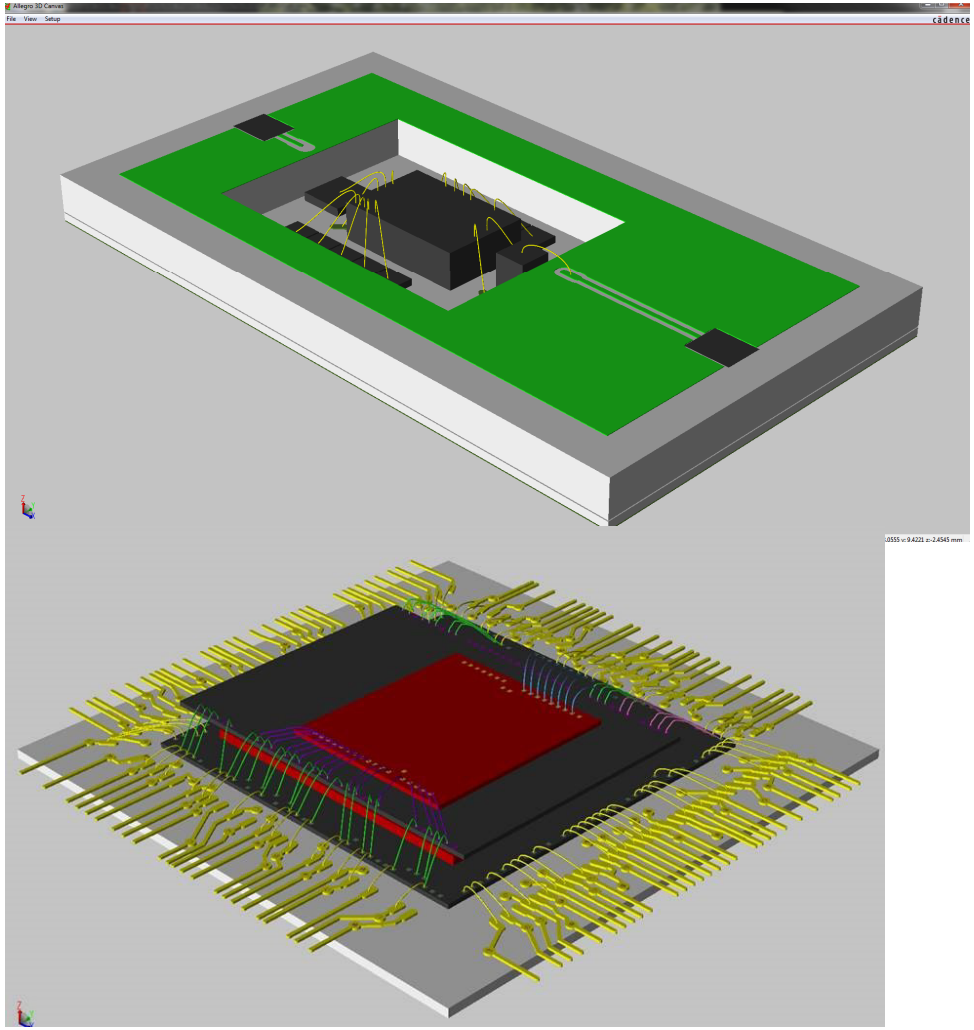
- Additional export controls
  - Export only what's visible
  - Export system in a bent state
- New file formats supported
  - STEP
  - 2D PDF
  - 3D PDF
- 3D PDF
  - Rotate or spin the design
  - Search for Symbols, Pins and other database objects



3D PDF Example

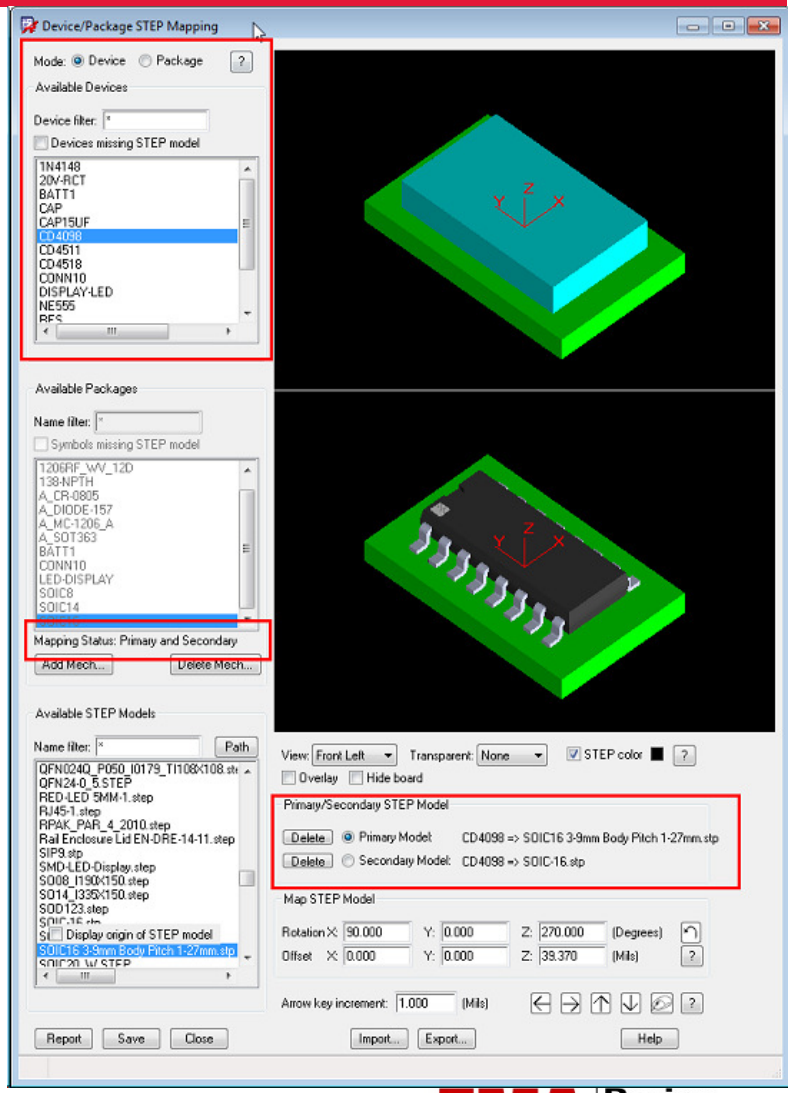
New 3D Interactive Canvas *(Unsupported Prototype)*

- Chip On Board Visualization
- Allegro PCB Editor
  - Simplistic wire bond view
  - Works with cavities
- APD/SiP Editor
  - Enhanced Wire Bond representation



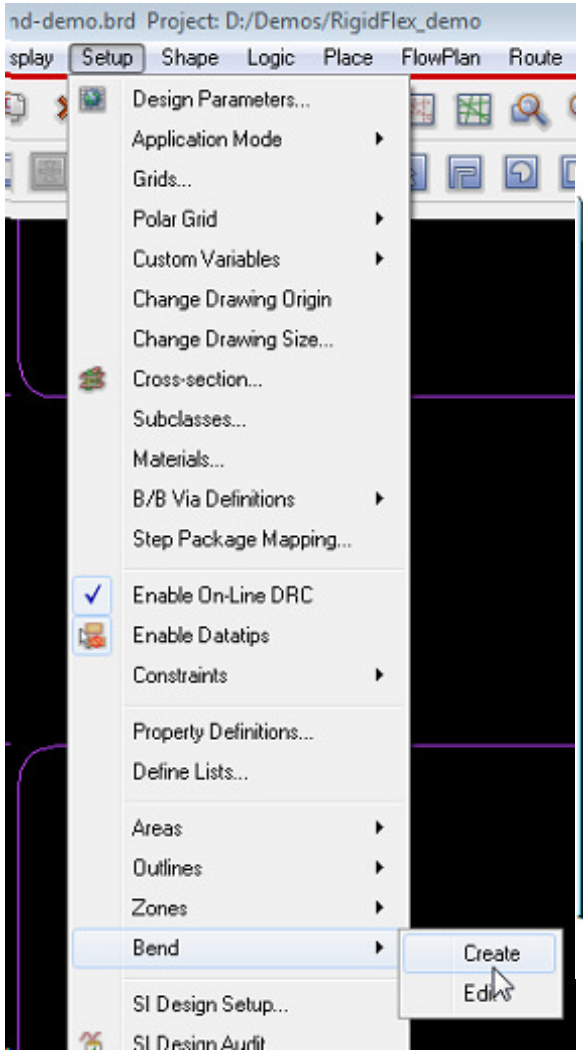
STEP Model Mapping to Devices

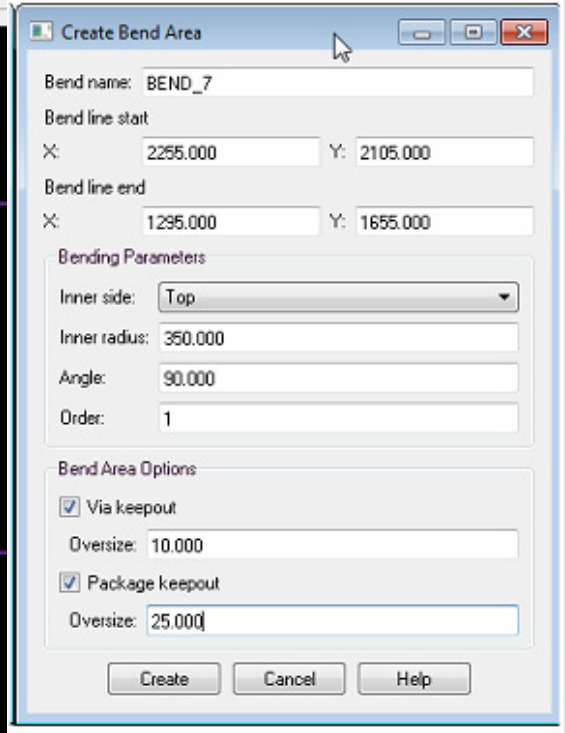
- New Mapping Mode
  - Device
  - Package
- New Information Button “?”
- New Pane
  - Current Devices in Design
- New Mapping Status for Package
  - Primary
  - Secondary

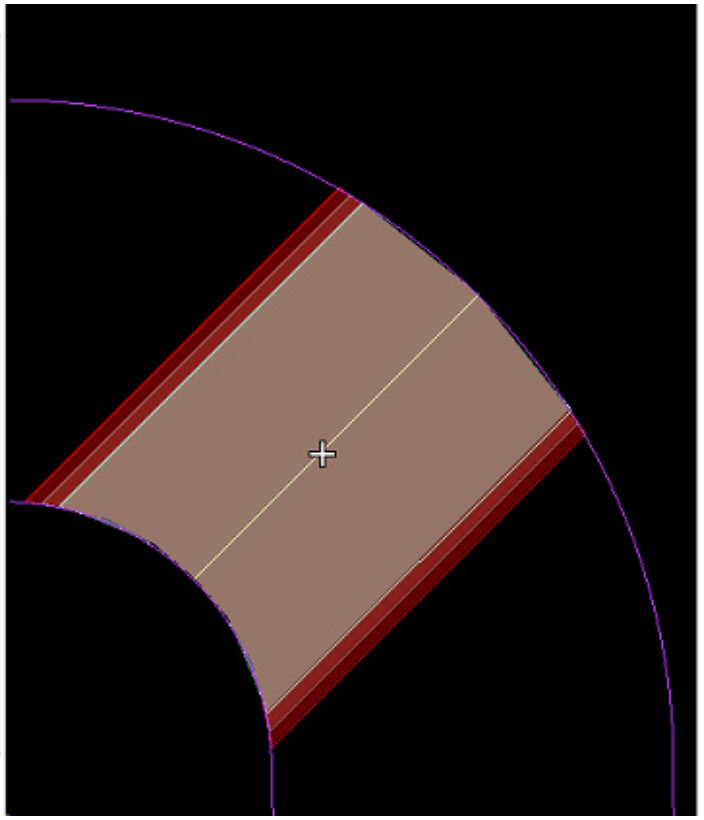


Bend Editor for Flex Design Applications

- Creating Bend Definition

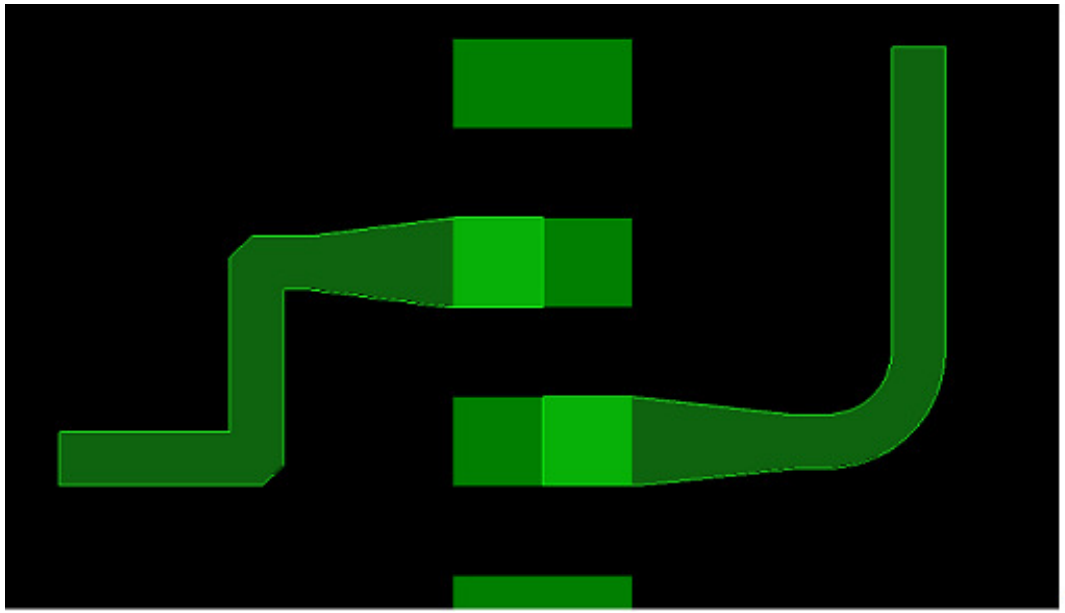


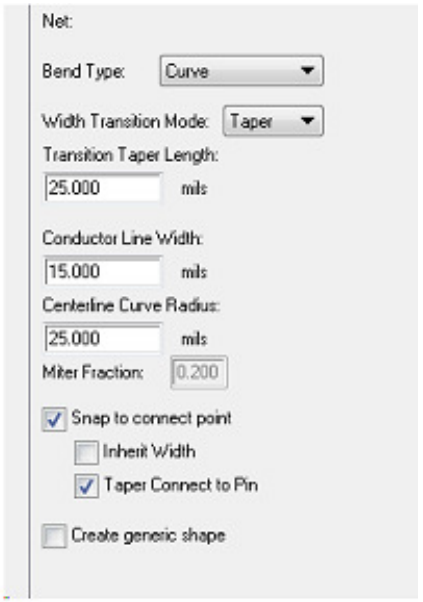




Add RF Trace & Convert RF Trace *(Unsupported Prototype)*

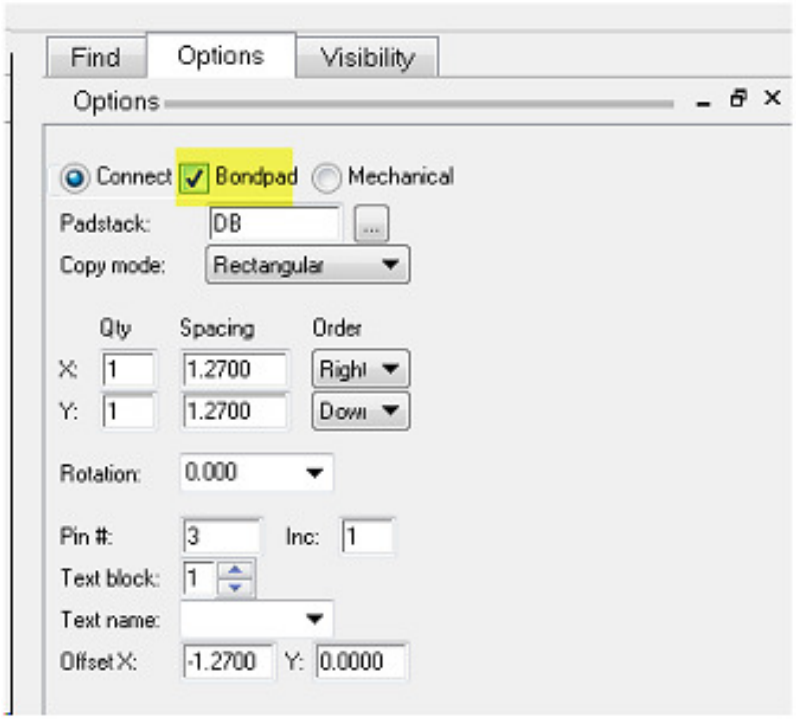
- Three Bend Types
  - Square
  - Mitered
  - Curve
- Width Transition Mode
  - None
  - Round
  - Taper

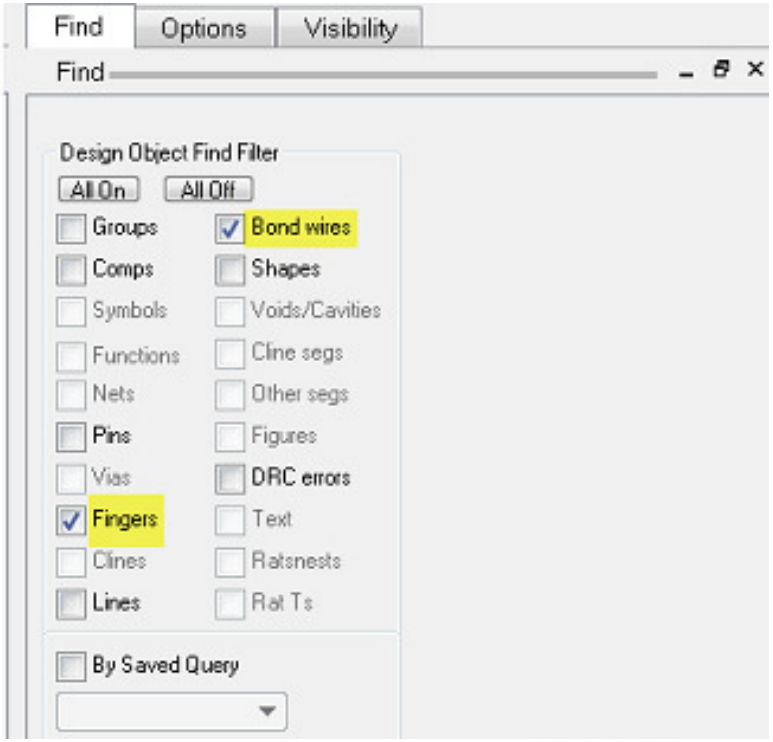




Chip on Board

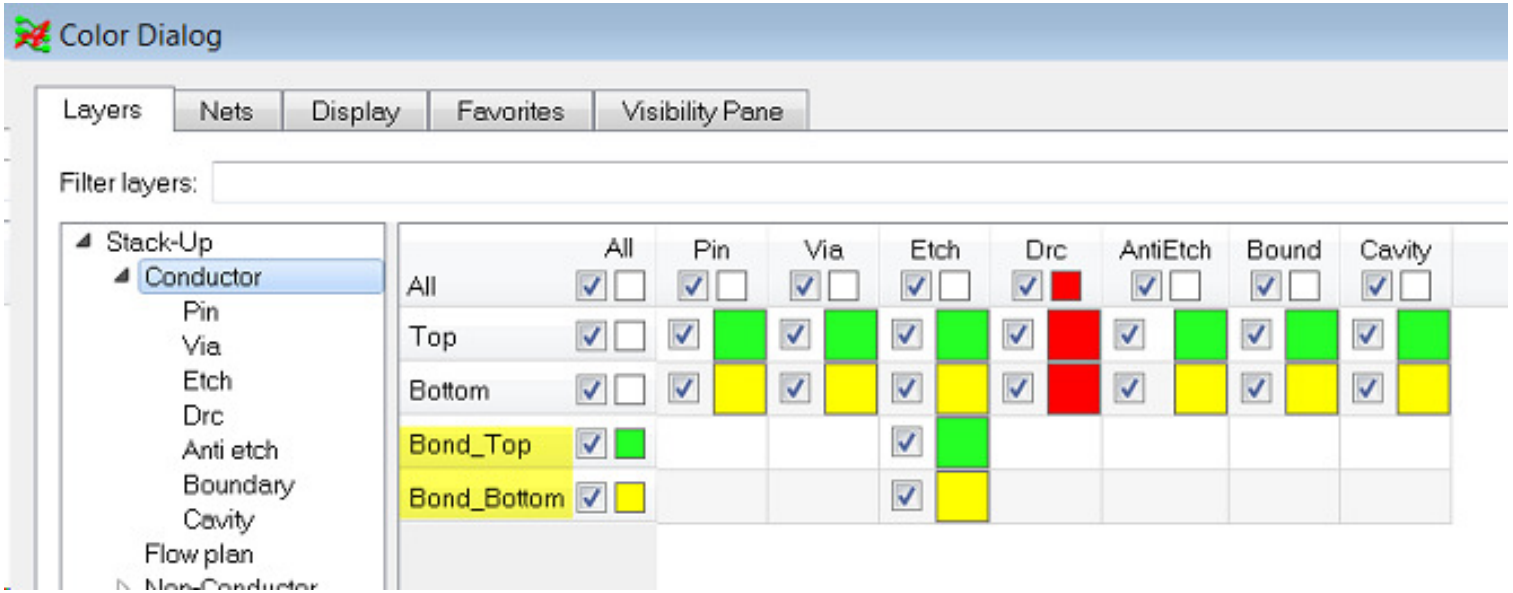
- Allegro PCB Designer Supports Basic Wirebonding
- Must add Bondpad Option in Symbol Editor
- Pins must be added with Bondpad Option





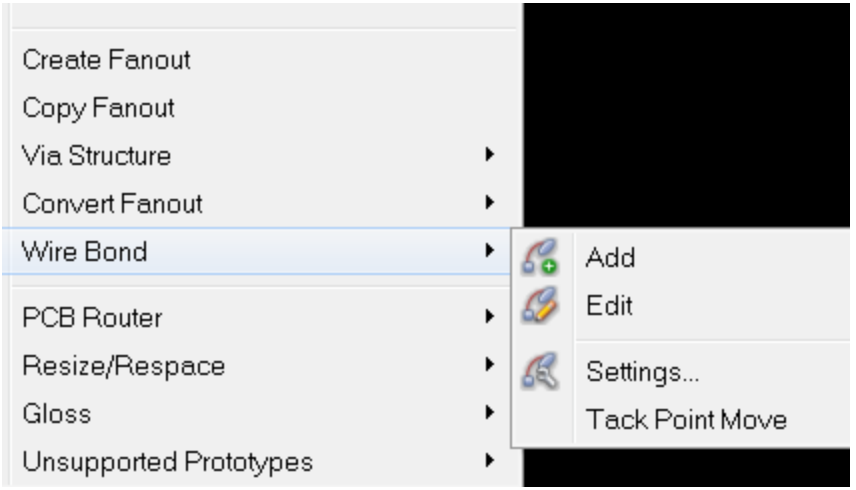
Chip on Board

- Two New Subclasses to support DIE pins
  - Bond_Top
  - Bond_Bottom
- Considered virtual layers
- Not included in Fabrication Packages

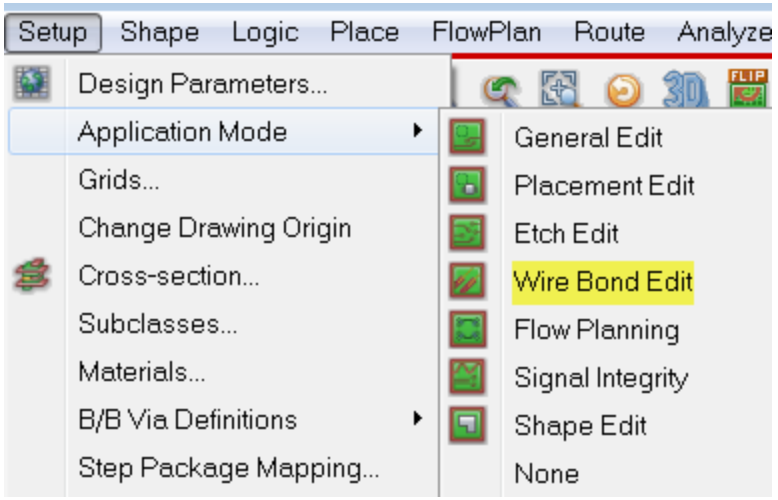


Chip on Board

- Menu Path
  - Route > Wire Bond
    - Add
    - Edit
    - Settings
    - Tack Point Move

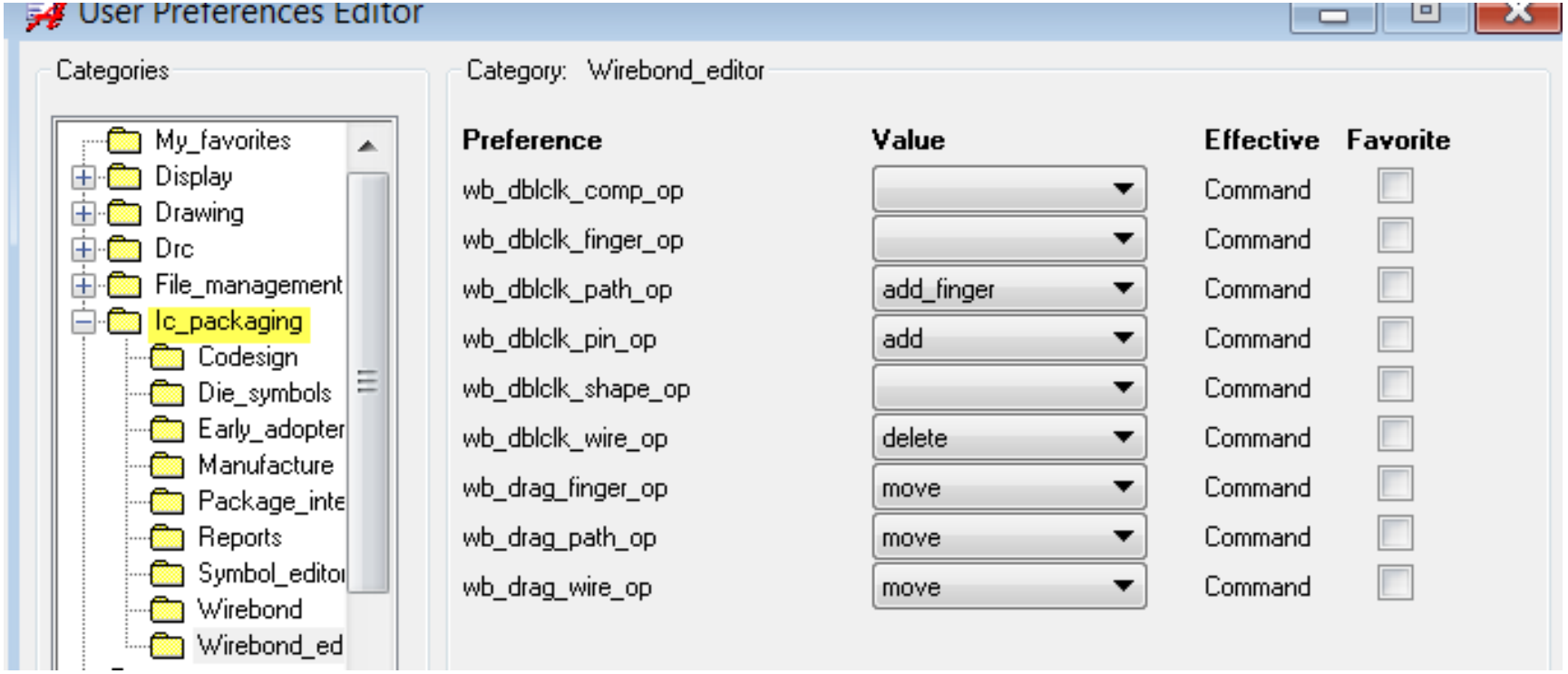


- Application Mode



Chip on Board

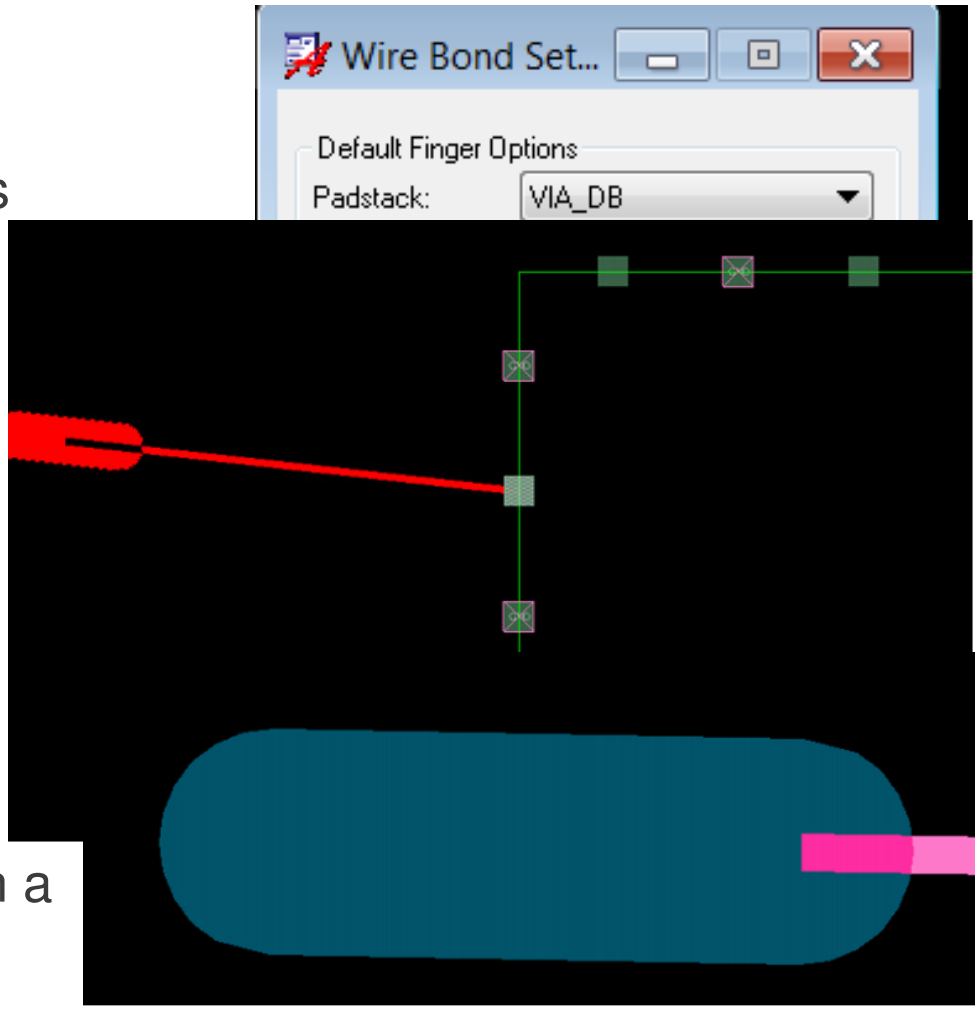
- User Preferences
- *User Preferences > Ic_packaging > Wirebond_ed*



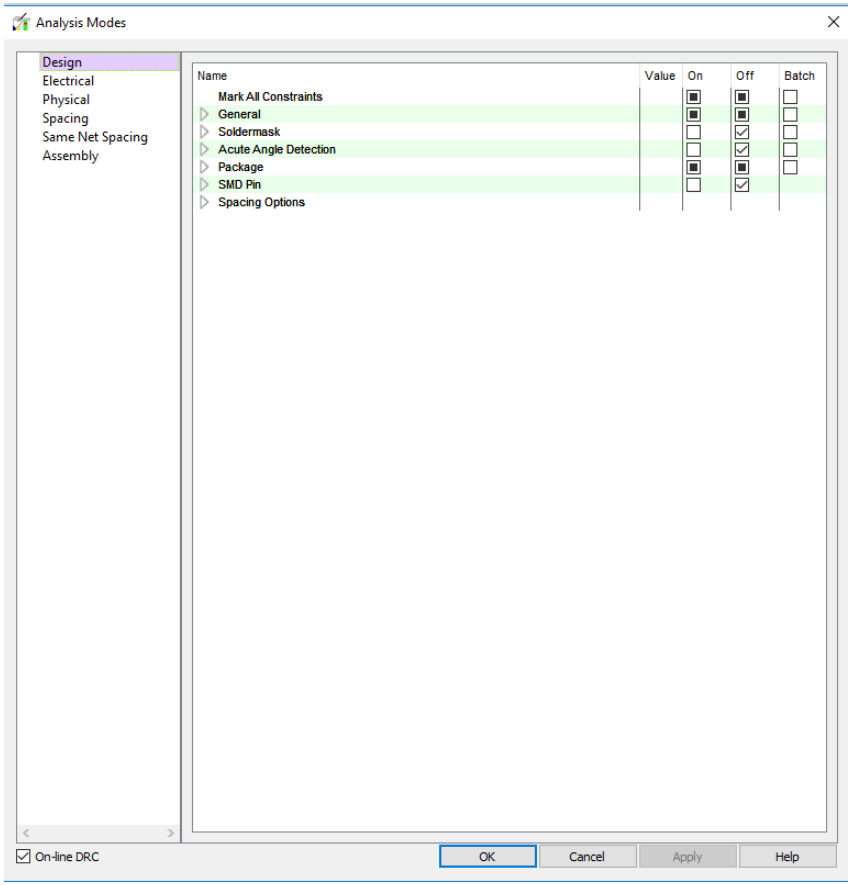
Example: Double click on DIE pad = wirebond_add

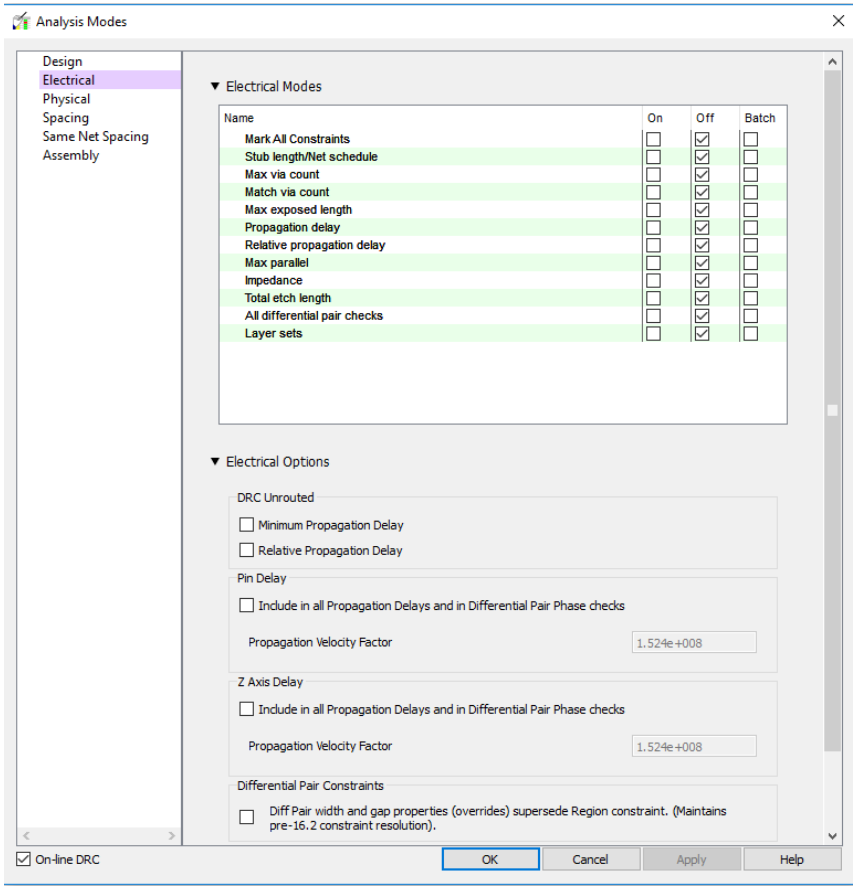
Chip on Board

- Defining the Bond Finger Alignment Options
  - Route > Wirebond > Settings
- Adding a Wirebond
  - Select one or more pins
  - Length and Angle of wire is displayed
- Moving Tack Point
  - Reposition wires within bond fingers
  - Enables multiple wires within a bond finger



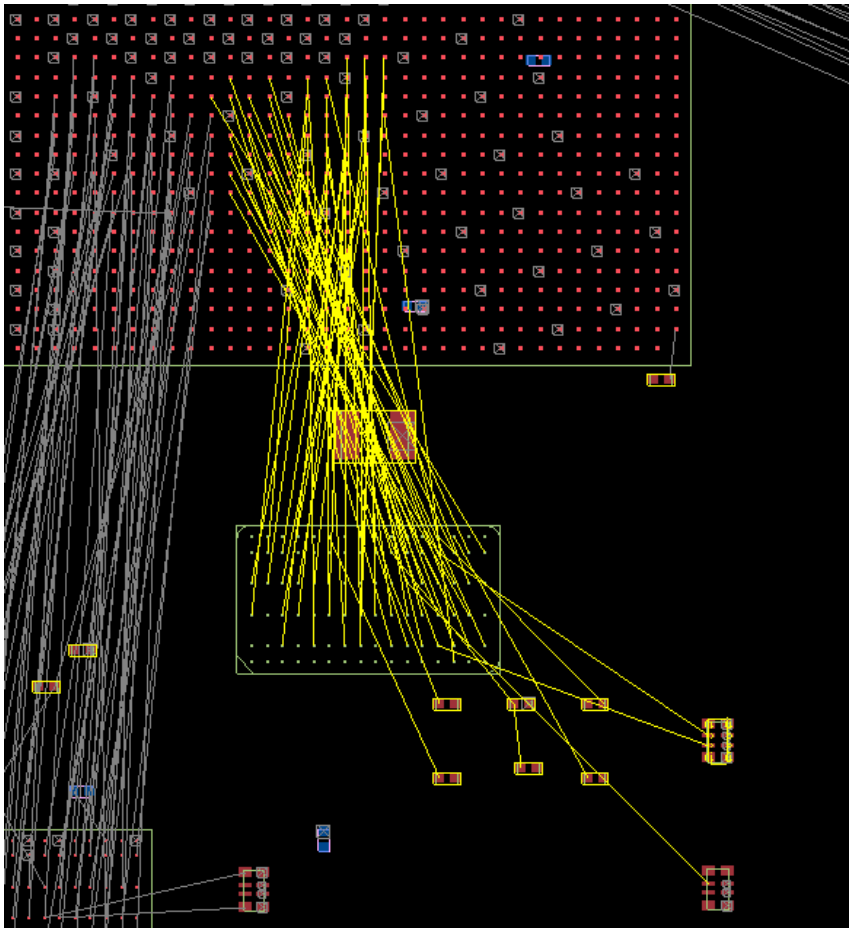
Analysis Mode Forms Updated





Dynamic Ratsnest

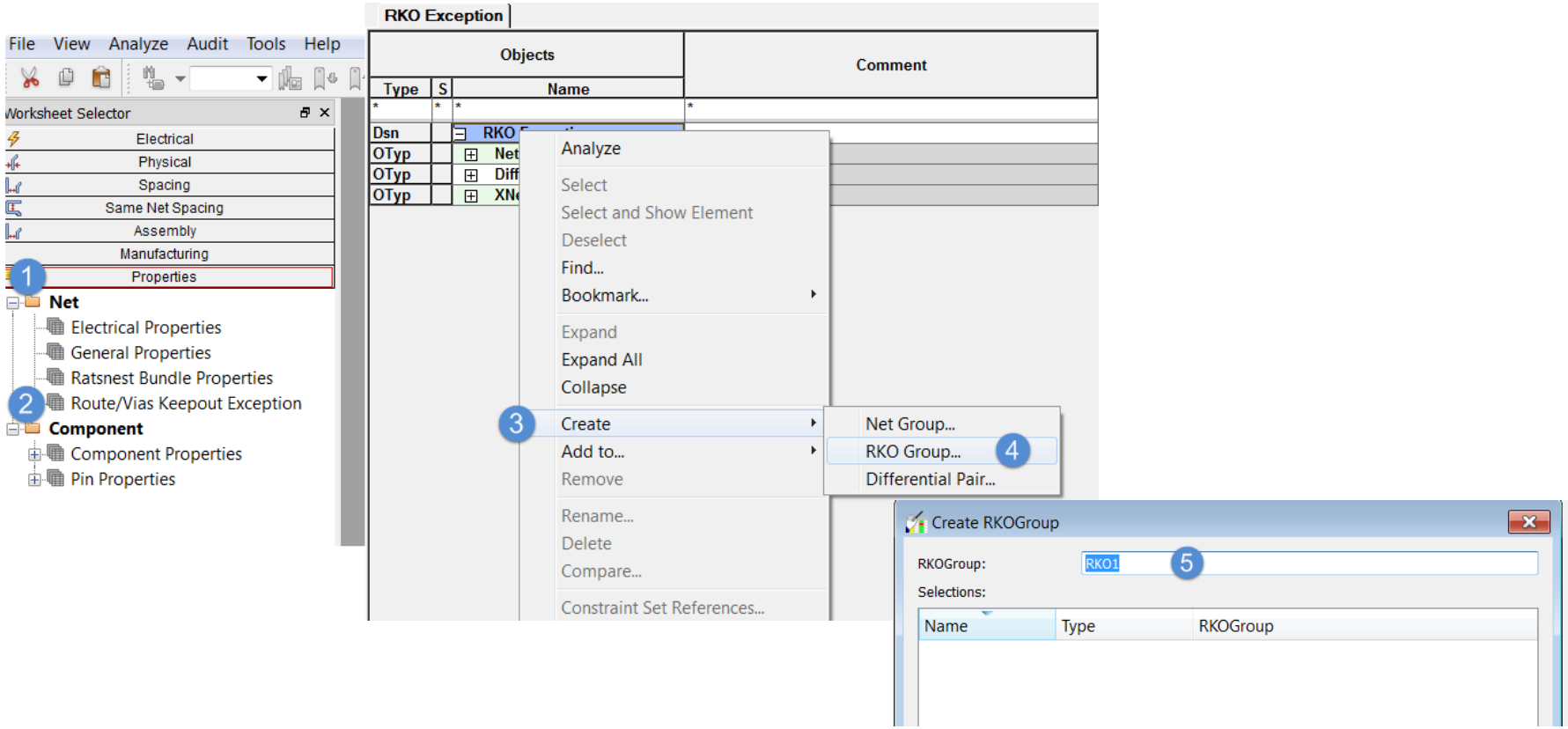
- Ratsnest lines update dynamically during component move
- Not supported
  - User-Defined Net Schedule
  - System-Define Net Schedule
  - Power Nets
  - Ground Nets
  - Nets with pin count greater than 20
  - Components with pin count greater than 100



NOTE: To disable, *set no_dynamic_ratsnest* in *User Preferences > Placement > General*

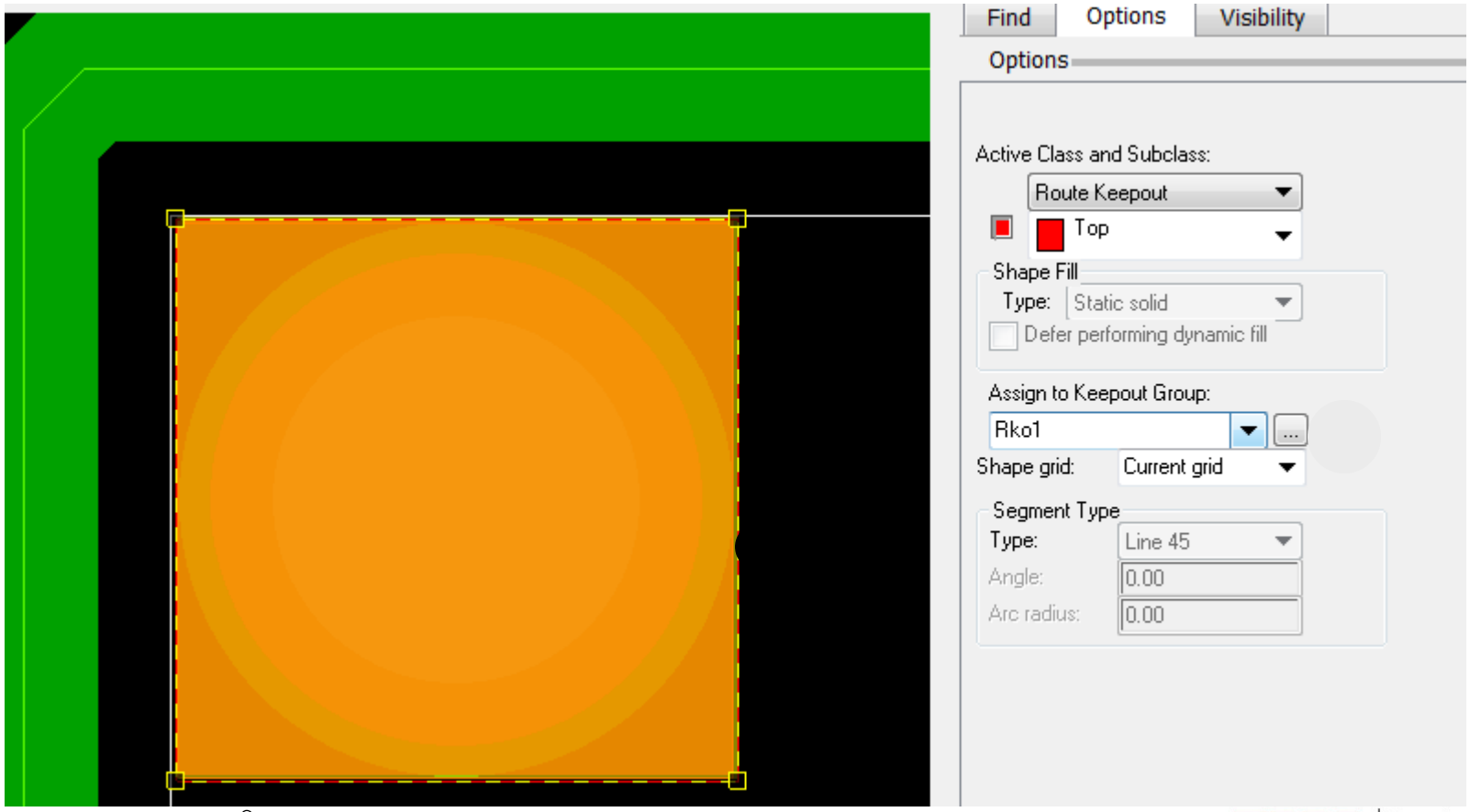
Route Keepout Net Exception

- Creating RKO Group in Properties Domain of CM
  - Members of RKO Group show no DRCs



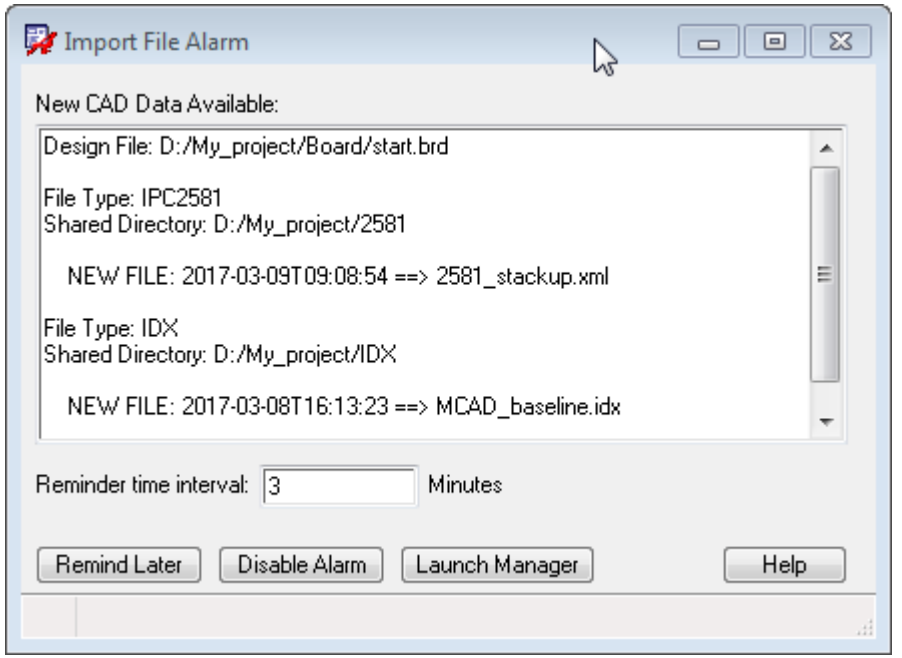
Route Keepout Net Exception

- Assigning RKO Group to RKO Shape in PCB Editor
  - Use Options tab in PCB Editor



Import File Manager

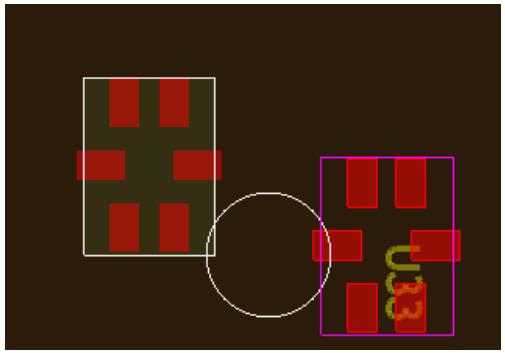
- Detects updated import files
- Displays a pop-up notification
  - Provides Options
- Supported File Extensions
  - Logic - pst*.dat
  - IPC2581 - xml and cvg
  - IDX - idx
  - IDF - dbf and emn
  - DXF - dxf



NOTE: Set env variables in *User Preferences > File_management > Miscellaneous*

Productivity Enhancements CCR Driven

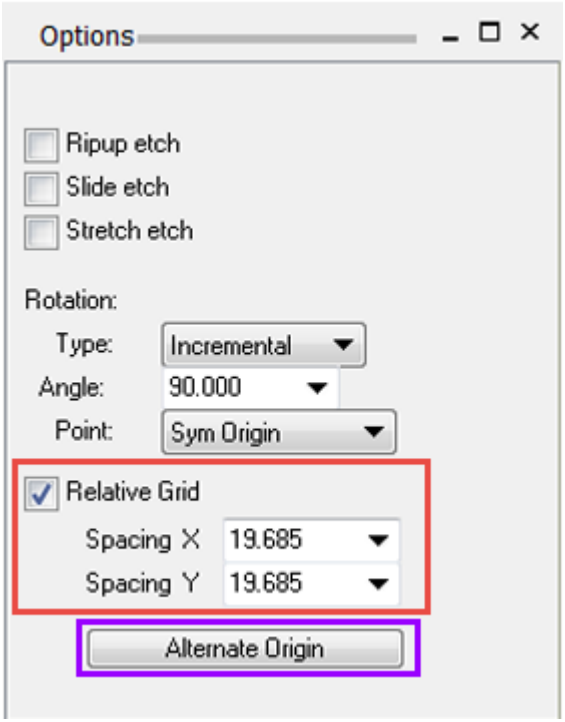
- Legacy “Edit-Move” command now integrated into the DFA application
  - High demand CCR
  - Previously limited to Place Manual and Place App Mode

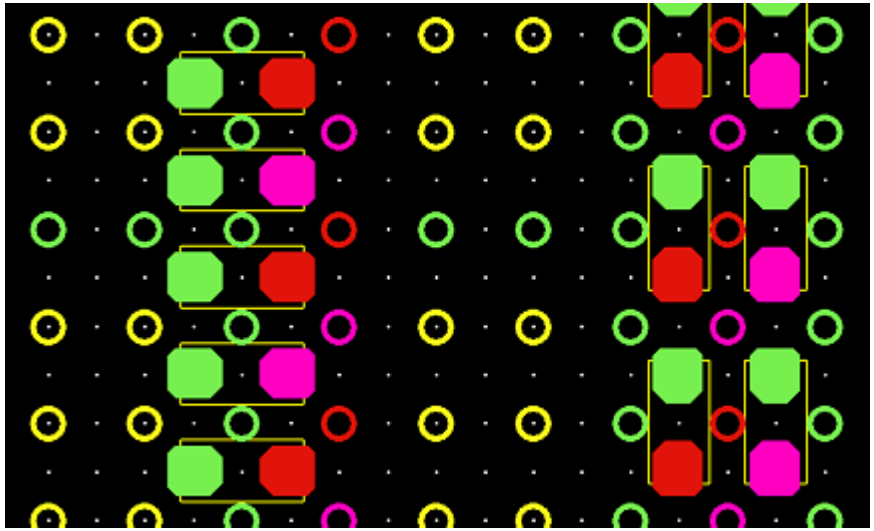


- Assign net to vias
  - High demand CCR
  - Offered in General and Etch Edit App modes
  - Hover over via(s) then RMB - Assign Net

Relative Grid

- Available during *Move* command only

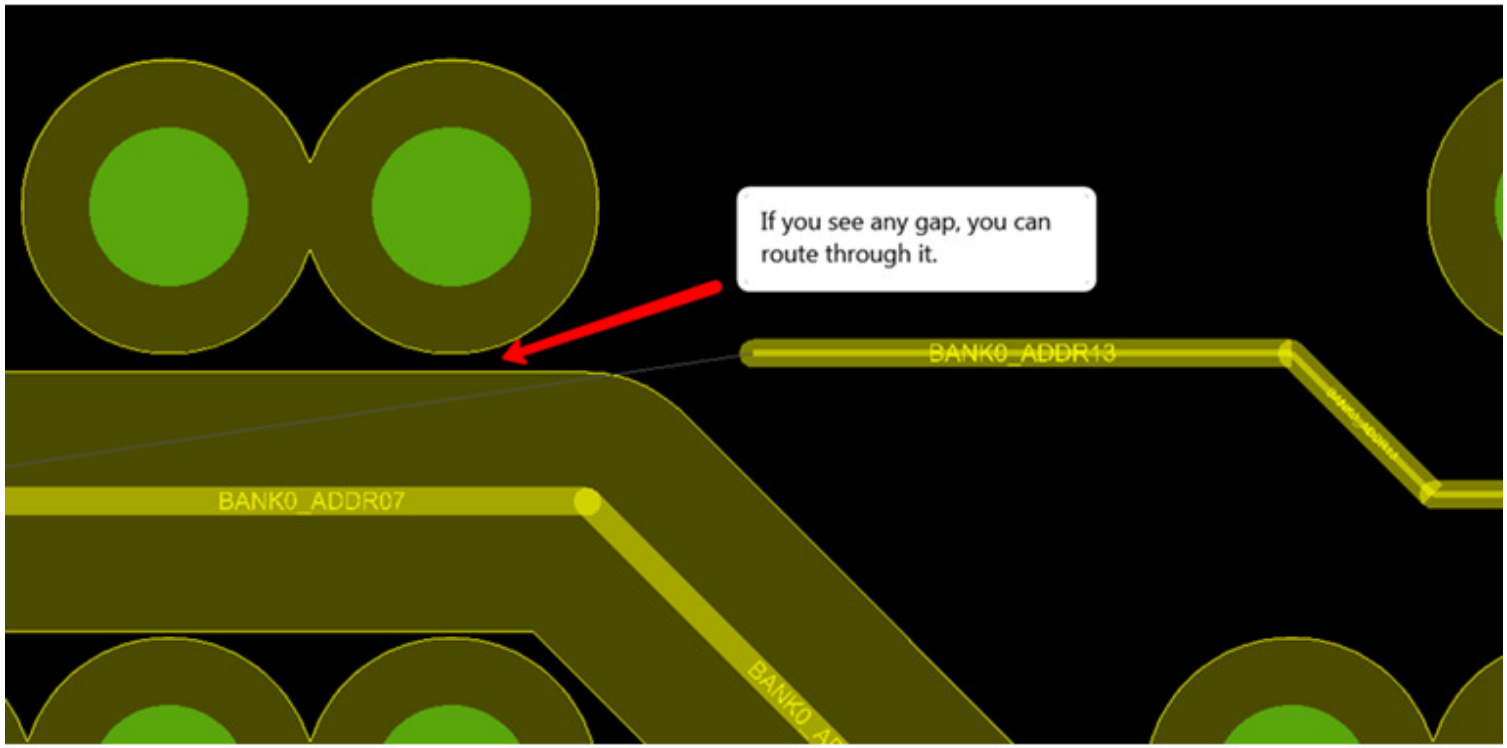




Example: Allows decoupling caps to be placed relative to a fanout via on a 1mm BGA

Route Clearance View *(Unsupported Prototype)*

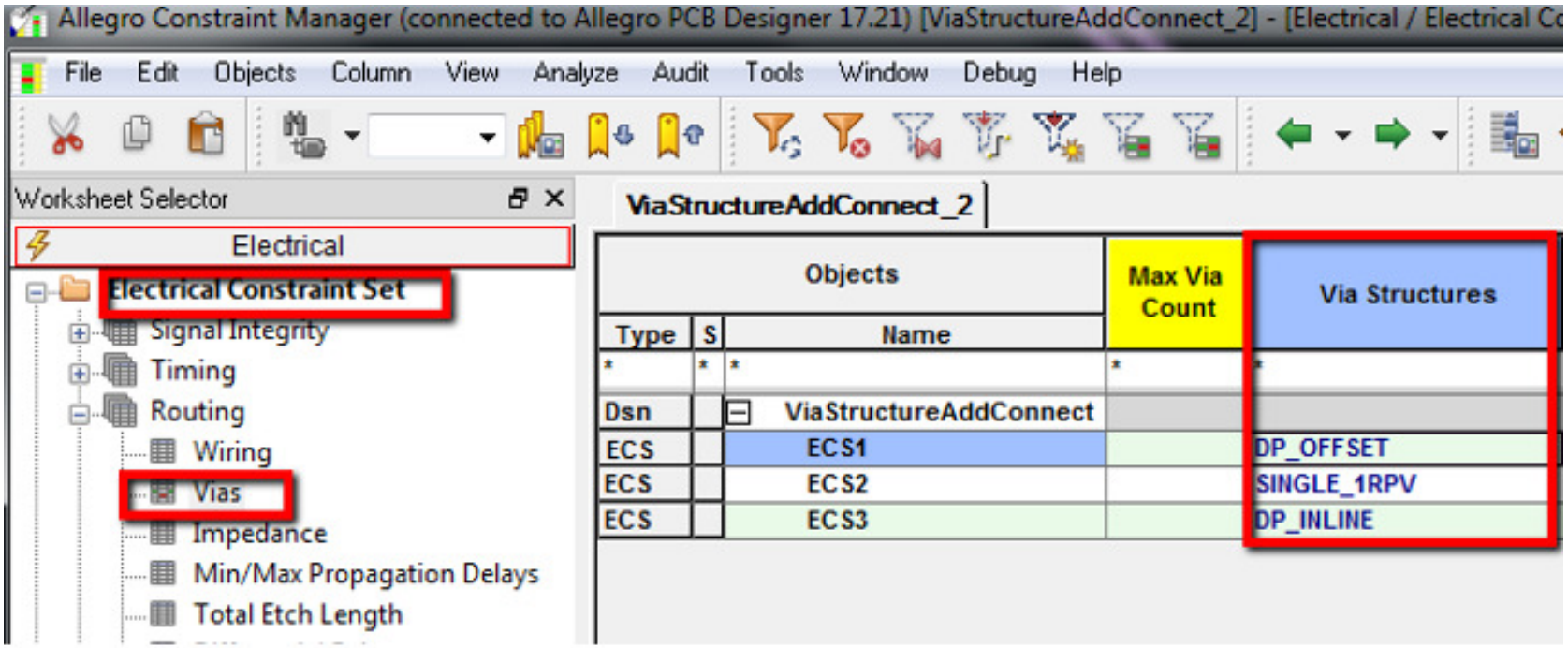
- Visual assistant for estimating space available in channels
- Determines routability based on spacing and line width



Note: Set in User Preferences > Unsupported > clearance_view > channel

Via Structures in Constraint Manager

- Via Structures are now added to ECSets in CM

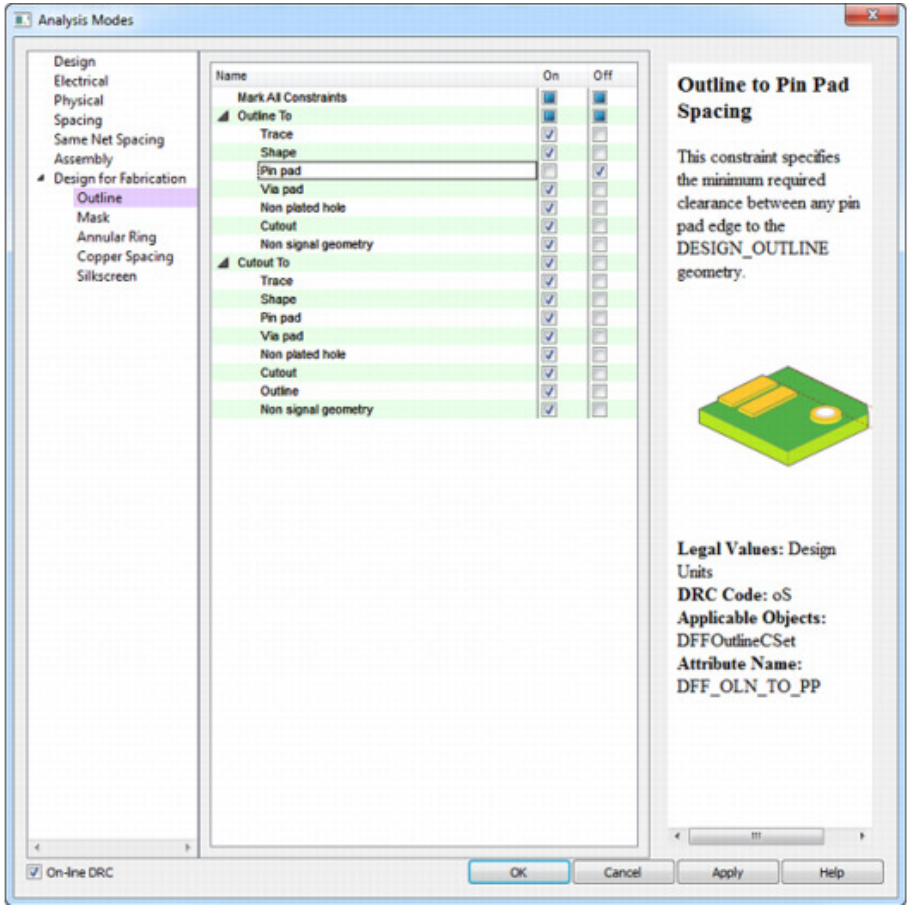


Inter-Layer DRC Update

- Inter-Layer DRC spreadsheet now supports Manufacturing class subclasses/layers

Allegro PCB Design True DFM

- In-Design DFx Environment
  - Bare Board Fabrication Checks
  - Defined as CSets in Constraint Manager
- Design for Fabrication CSets
  - Assigned to
    - Conductor Layers
    - Mask Layers
    - Silkscreen Layers
- DFx CSets may be exported
  - Technology Files
  - Constraint Files



Allegro PCB Design True DFM

- Outline Checks
  - Objects to Board Outline Spacing

Name	Constraint set usage	Outline To							Cutout To		
		Trace	Shape	Pin pad	Via pad	Non plated hole	Cutout	Non signal geometry	Trace	Shape	Pin pad
*	*	*	*	*	*	*	*	*	*	*	*
<Create new>											
Outline_Rigid_External	Etch	40.000	40.000	50.000	50.000	35.000		40.000	35.000	35.000	40.0
Outline_Rigid_Internal	Etch	50.000	50.000	50.000	50.000	35.000		45.000	40.000	40.000	40.0
Outline_Flex	Etch	35.000	35.000	40.000	40.000	35.000		15.000	25.000	25.000	25.0
Outline_Cutout	Stackup						35.000				
Sm_Oultine	Non-Etch		37.000	46.000	46.000	32.000				37.000	46.0

Allegro PCB Design True DFM

- Mask Checks
  - Minimum Mask Sliver Width
  - Minimum Mask Island by Square Area

Name	Constraint set usage	Mask	
		Slivers	Islands
*	*	*	*
<Create new>			
CI_Flex	Non-Etch	3.500	17.000
Sm_Rigid	Non-Etch	3.000	25.000

Allegro PCB Design True DFM

- Annular Ring Checks
  - Pad to Hole
  - Pad to Mask
  - Missing Mask
  - Hole to Antipad

Name	Constraint set usage	Pin				Via			
		Missing mask	Pad to mask	Hole to pad	Hole to antipad	Missing mask	Pad to mask	Hole to pad	Hole to antipad
	*	*	*	*	*	*	*	*	*
<Create new>									
Flex_Cl_Mask	Non-Etch	Yes	1.000			Yes	2.000		
Flex_Ext	Etch			9.000	11.000			6.000	8.000
Flex_Gm	Non-Etch	No	1.000			No			
Flex_Int	Etch			9.000	11.000			6.000	8.000
Flex__Pm	Non-Etch	Yes	0.500			No			
Rigid_Cu	Etch			8.000	10.000			6.000	7.500
Rigid_Sm	Non-Etch	Yes	1.000			Yes	1.000		

Allegro PCB Design True DFM

- Copper Spacing Checks
  - Signal Geometries
    - Trace, pads, vias, shapes, non-plated holes, etc.
  - Non-Signal Geometries

Name	Constraint set usage	Trace to						Shape to		
		Trace	Shape	Pin pad	Via pad	Non plated hole	Non signal geometry	Trace	Shape	Pin
*	*	*	*	*	*	*	*	*	*	*
<Create new>										
Flex_Ext	Etch	5.000	6.000	5.000	5.000	8.000	6.000	6.000	8.000	8.(
Rigid_Cu_Ext	Etch	4.500	6.000	5.000	5.000	8.000	5.000	6.000	7.500	7.5
Rigid_Cu_Int	Etch	4.000	5.000	5.000	4.000	8.000	5.000	5.000	7.500	7.5

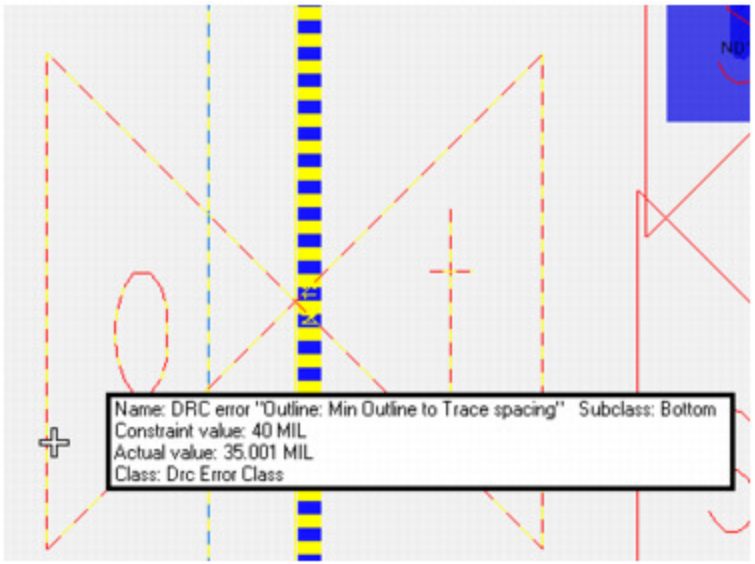
Allegro PCB Design True DFM

- Silkscreen Checks
  - Pin to Silkscreen
  - Via to Silkscreen
  - Non-Plated Hole to Silkscreen
  - Minimum Character Width
  - Minimum Line Width

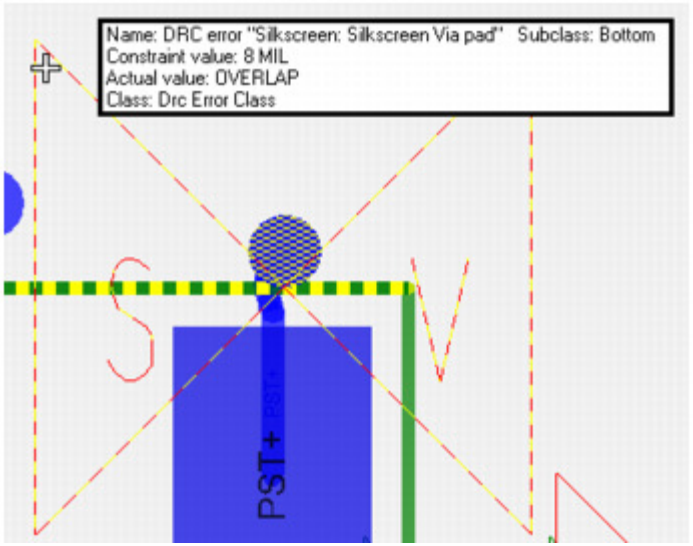
Name	Constraint set usage	Pin pad	Via pad	Non plated hole	Min width(line,arc,shape)	Min length(line,arc)
	*	*	*	*	*	*
<Create new>						
Flex_Ss	Non-Etch	8.000	6.000	10.000	4.500	7.000
Rigid_Ss	Non-Etch	10.000	8.000	12.000	5.000	10.000

Allegro PCB Design True DFM

- DRCs



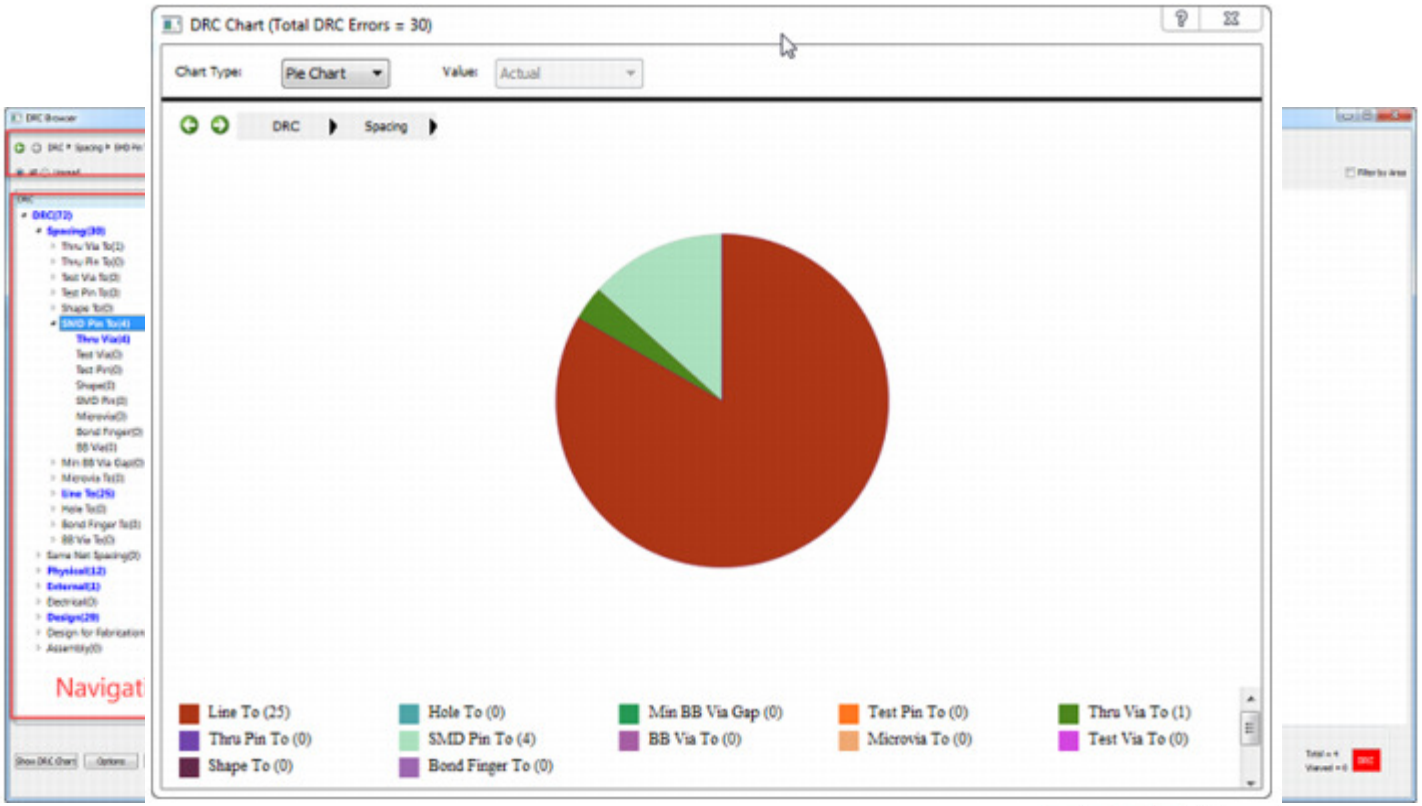
Trace to Outline Violation



Silkscreen to Via Violation

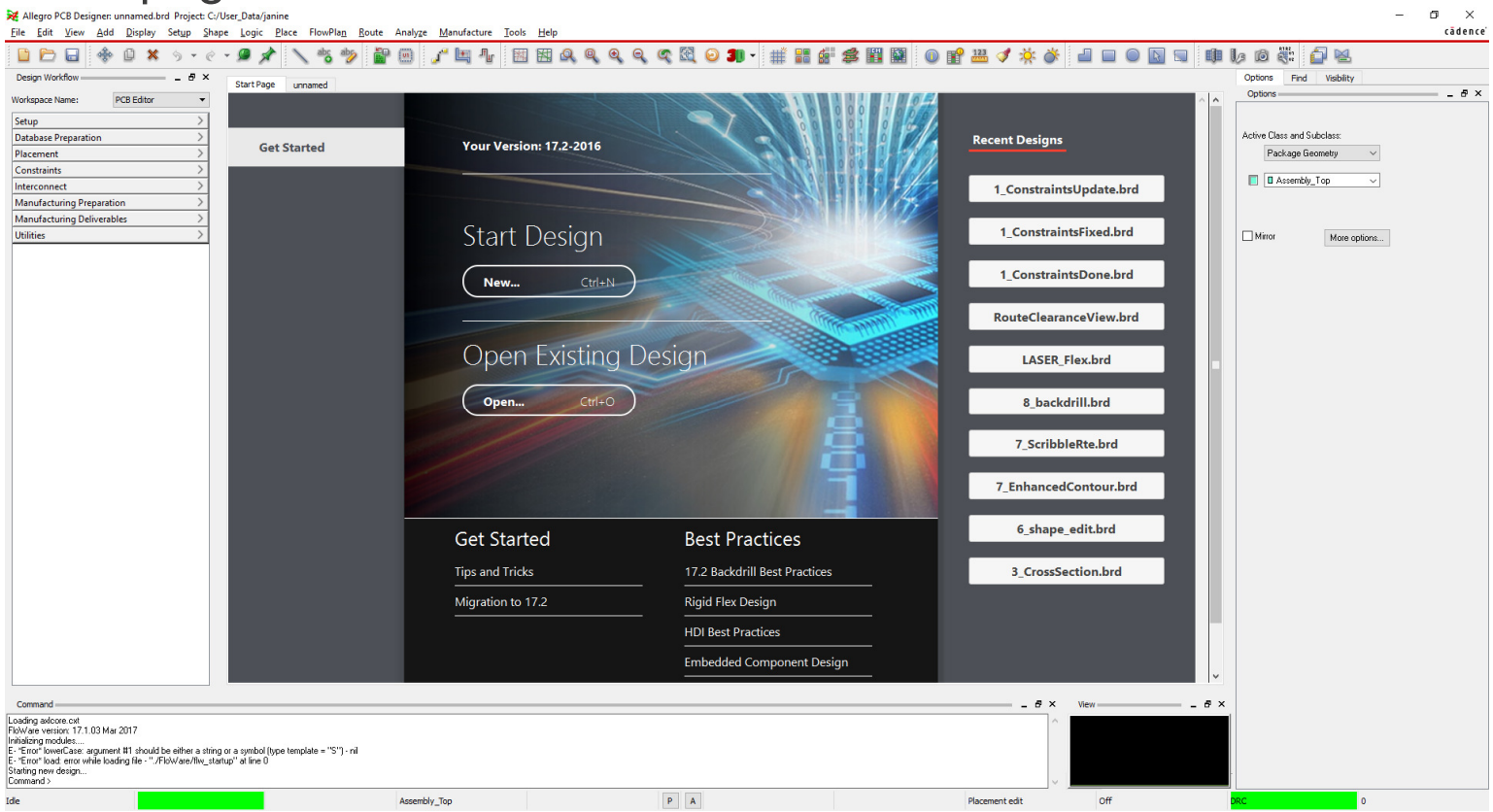
DRC Browser

- Enhances the ability to locate, review and correct DRCs
- ***Tools - DRC Browser***
- Functions
  - Navigation
  - Sorting
  - Filtering
- Views
  - List
  - Bar Chart
  - Pie Chart



New Start Page

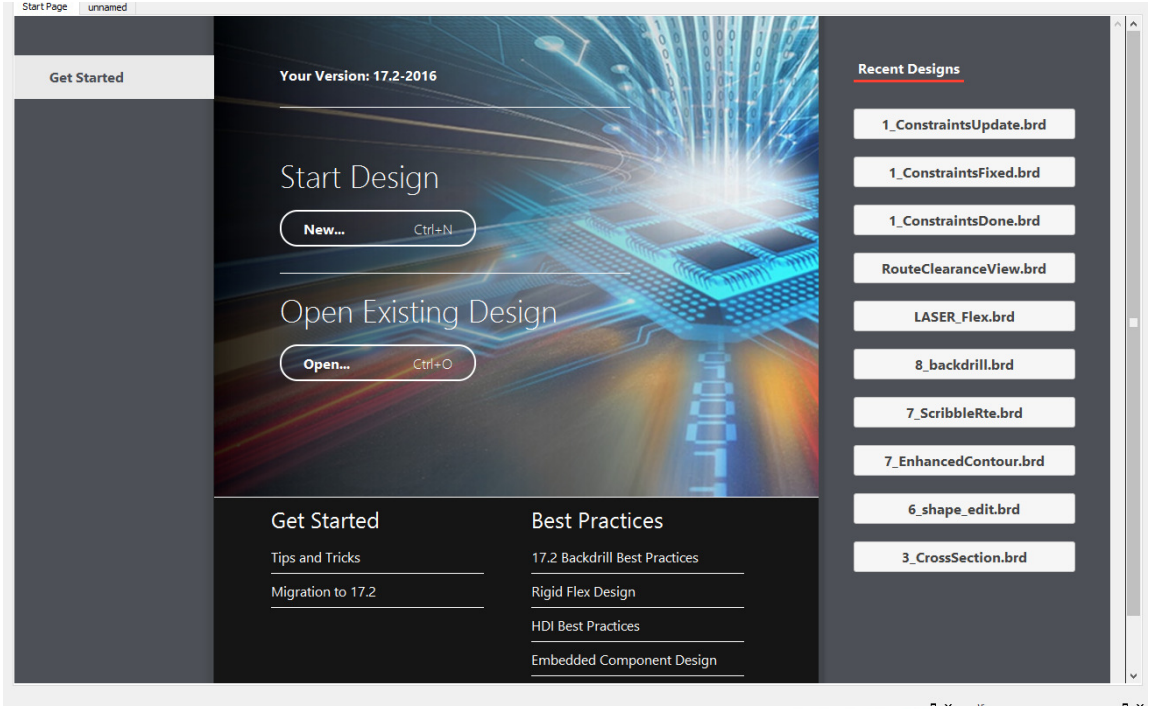
- When Allegro PCB Editor is launched without a design
  - Does not affect current use models
  - Start page is a tab in the canvas



New Start Page

- Recent Designs List
  - Provides easy access to valuable information

- Valuable information for new and existing users
  - Get Started
    - Tips and Tricks
    - Migration to 17.2
  - Best Practice papers
    - HDI
    - Rigid-Flex
    - Backdrill

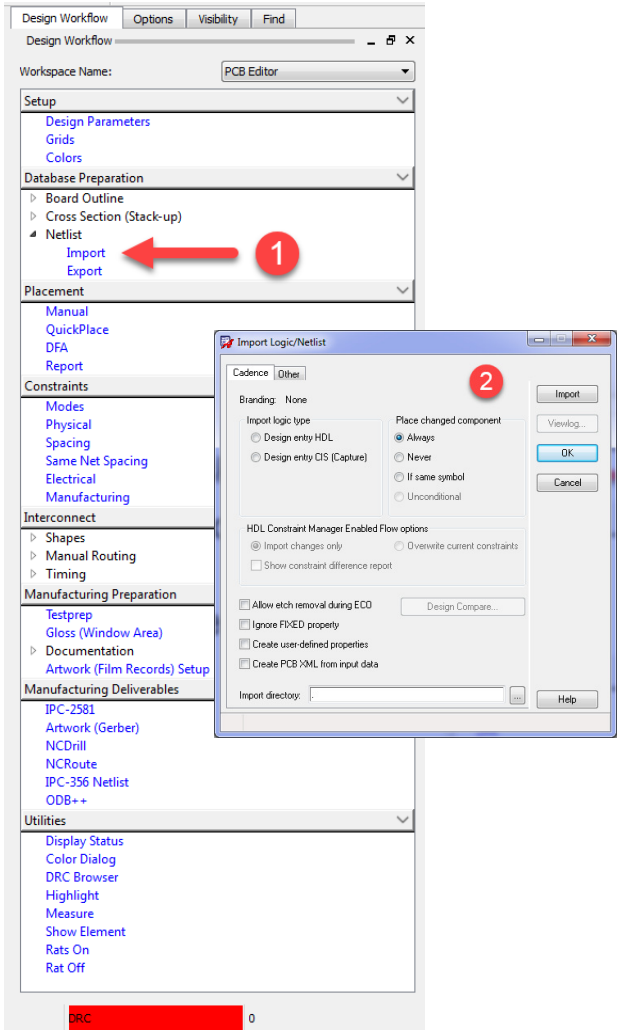


New Design Workflow Pane

- Great for new and experienced users
- Eliminates search icons or menus

- Guides users in performing basic tasks
  - Leverage experienced designers good practices for junior / new users
  - Selecting any choice will bring up proper dialog

- Create custom flows
  - Library creation
  - Internal checklist
  - Manufacturing deliverables

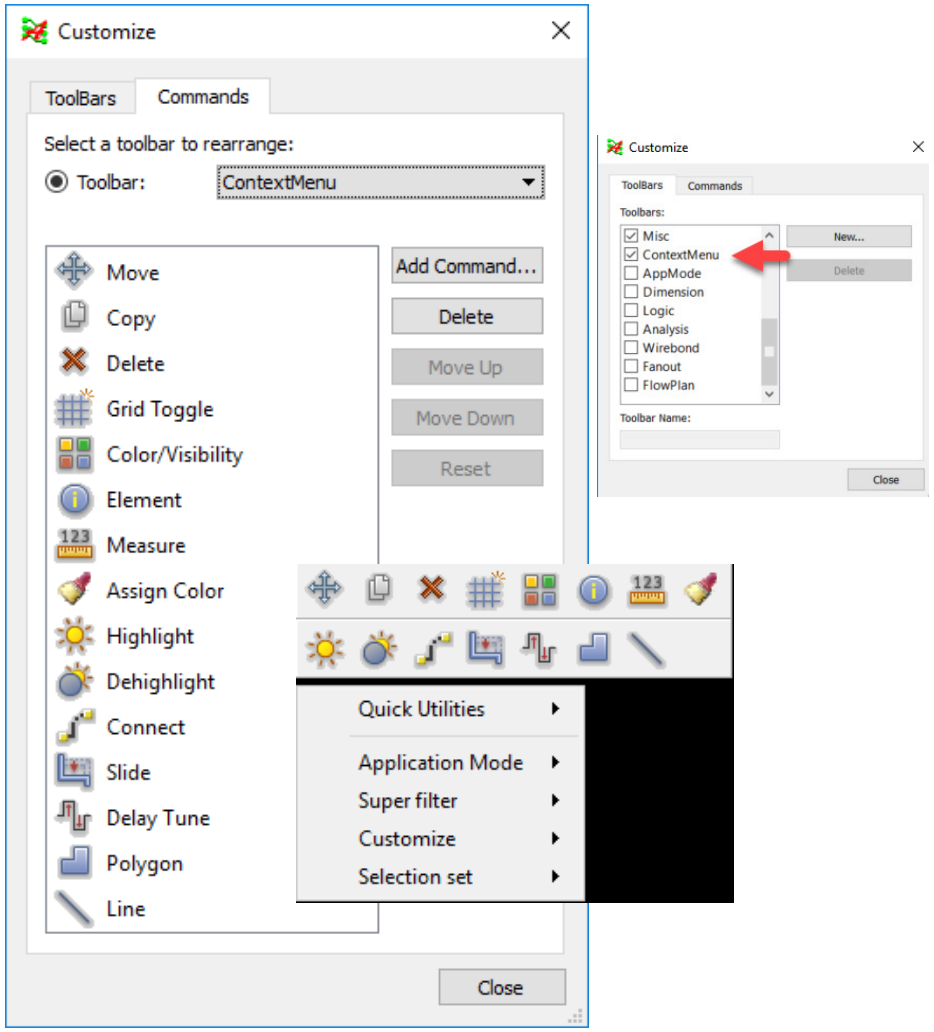


Canvas Enhancements

- Minimalistic Toolbars and Icons
  - Reduces clutter and confusion
  - Presents new users with basic icons
  - Full toolbars and icons available
  - Increased design work space
- Customize Design Canvas
  - Toolbars, Panes, Workspace
  - Save/recall views
  - Panes on other monitors
  - Managed -View – UI Settings menu

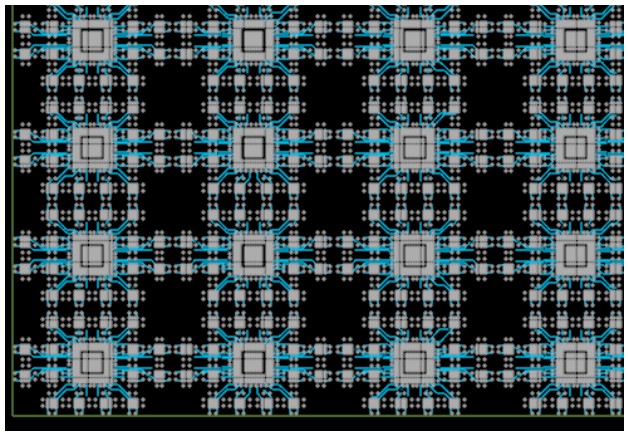
Canvas Enhancements

- Quick access to frequently used icons
  - RMB Context Menu
  - Reduces mouse travel
  - Consistent with MS tools
  - Fully customizable up to 16 icons
- Enable using ***View > Customize Toolbar***
  - *Select "**ContextMenu**" Toolbar*
- Customize using *"**Add Command**"*
  - *Re-ordering of icons supported*

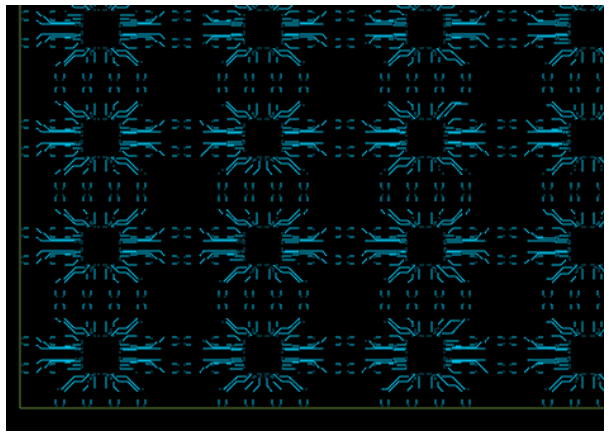


Canvas Enhancements
Improved Graphic Response Time& Resolution

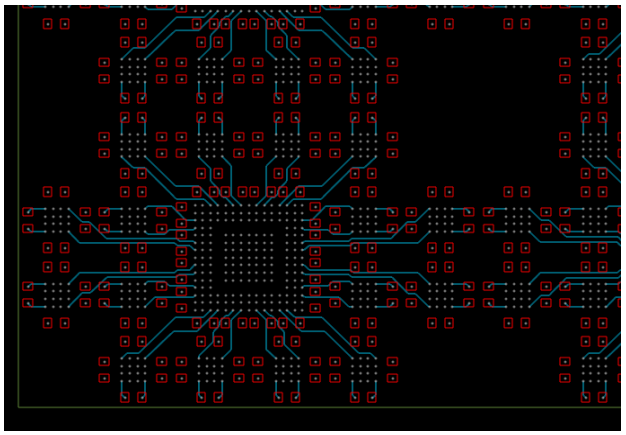
- Reduce visual complexity of large designs
- Quicker panning & zooming
- Color Dialog Object Filter Control
  - Customized level of pin/via granularity
  - Slider setting to filter small objects



Disabled - too much detail



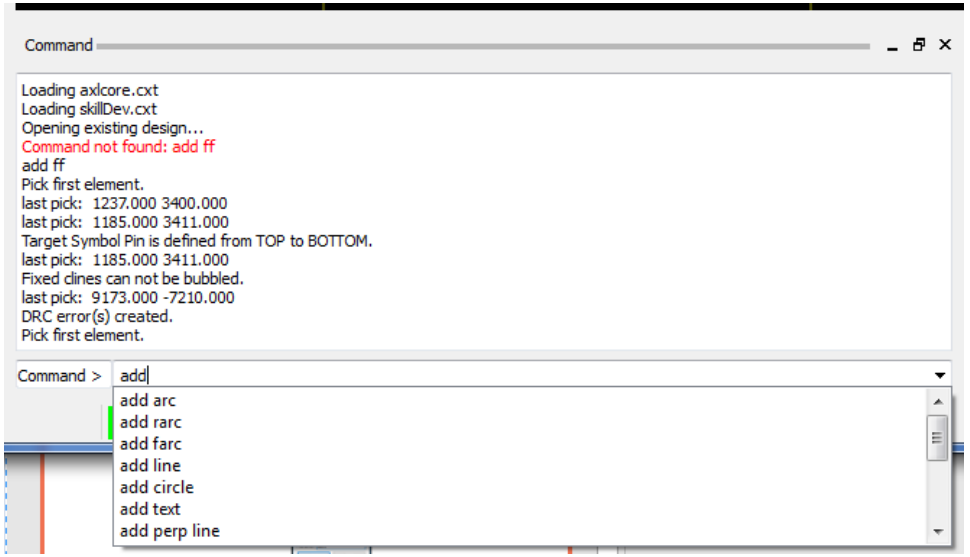
Enabled - Enough detail



Zoom in - Greater detail

Canvas Enhancements

- Modernized Command Window
  - Auto-Complete commands
  - Full history of typed commands
  - Separate input/output sections



- Colored Visual Indicators
  - (Black) = Messages
  - (Orange) = Warning
  - (Red) = Error

- Offered in QIR5 as Unsupported Prototype
  - Variable located in User Preference Editor – Unsupported folder

Migration to QIR5

- Existing users will not see change to their Toolbar arrangement
  - New users to Cadence or existing users moving to new machines will experience the new canvas default settings
- Invoking ***"Reset UI to Cadence Default"*** will default to
  - Minimalistic toolbar
  - Design Workflow pane
  - Command window
  - Option, Visibility, Find Panes
  - Worldview
- Design Workflow pane is optional and can be removed
  - Supported in the PCB Editor, APD and SiP products
- Toolbar and window pane settings stored in registry
- Users are encouraged to create custom UI settings using ***View > UI Settings – Save Settings***
  - Recall "saved" settings using the ***View – UI Settings*** command
  - Select setting from top section to popup form

Thanks for joining us!

Allegro & OrCAD PCB Editor