cadence®

Allegro® PCB Editor: What's New in Release 16.6

Product Version 16.6
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Allegro PCB Editor: What's New in Release 16.6

Product Version 16.6
October 2012

This document describes new features in the current and previous releases of Allegro PCB Editor. Significant enhancements have been made in the following areas:

- Route Interconnect Optimization
- Productivity Enhancements
- Design for Manufacturing
- Team Design (Partitioning) more Flexible in 16.6
- Embedded Component Design
- Database & Misc Enhancements
- Symbol Editor Enhancements
- Preparing for the 17.0 Release
- RF PCB Enhancements

To view the latest updates on hardware and software requirements, see the *Allegro Platform System Requirements*. Also refer to the *Migration Guide for Allegro Platform Products, Product Version 16.6*.

Route Interconnect Optimization

- Auto-Interactive Delay Tune (AiDT) – High Speed Product Option
- Slide Overhaul
- Offset Routing
- Smart Layer Behavior for Add Connect
- Disable Open Space Routing
- Line Width Retention during Add Connect
- Fix Cline Segments
- Copy/Move Cline Segments
- Unsupported Prototype Menu
- Auto Interactive Convert Corner (AiCC) Unsupported Prototype

Auto-Interactive Delay Tune (AiDT) – High Speed Product Option

Auto-interactive Delay Tuning reduces the time to meet timing constraints on advanced standards-based interfaces, such as DDR3, by 30-50%. The *AiDT* command allows you to rapidly adjust the timing of critical high-speed signals on an interface-by-interface basis, or apply it at byte-lane level, reducing the need to tune the traces on a PCB. You can interactively select clines or cline segments for tuning, *AiDT* then computes the required length for the selection set to meet timing constraints. This command utilizes controlled push/shove techniques while adding tuning patterns based on user-defined parameters.

You can invoke the *AiDT* command from the *Route* Menu. In the Etch Edit application mode, AiDT is available from the right-click pop-up menu for Clines and Cline Segments. When in the Flow Planning application mode, *AiDT* is available from the right-click pop-up menu for Rat-bundles.

Use Models

You can use *AiDT* in various design scenarios using the following techniques:

Single Cline Tuning

This technique is most effective when there is ample room for each cline to achieve timing, without the need to push/shove adjacent routing around. This technique is helpful if you prefer manually moving routing around to create space for tuning. This technique also has the impact on existing routing, since no push/shove is allowed.

Cline Segment Tuning

Selecting individual or groups of cline segments is a very effective means to control where elongation occurs with AiDT. Only selected segments can have elongation added and can push/shove during the operations. All the unselected segments are considered fixed during that operation and do not need any changes. AiDT may become limited at the junction between selected and unselected segments where pushing cannot occur.

Match Groups

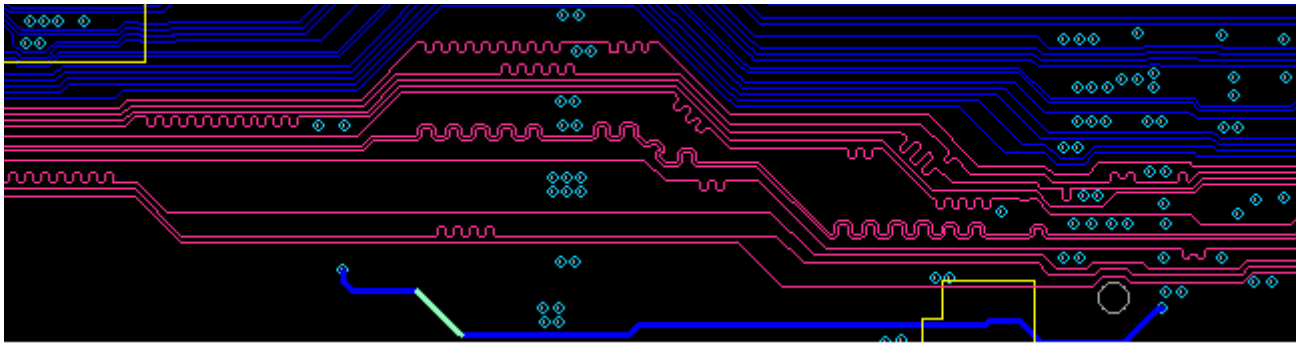
Tuning entire match group

This technique involves selecting all the clines from a match group to run at the same time. This technique is useful if all the routing is nearby, on the same layer, and the cline count is less than 20 signals.

Critical Signals

Critical signals are involved in a match group when running AiDT, these signals are manually tuning signals. The longest signal in the match group dictates the overall length requirement for the other signals. This value is computed by AiDT. The target (if there is one) controls the timing DRCs. If the target signal does not get to its desired length during the AiDT run, this may result in a misleading number of DRCs reported.

Figure 31- Tuning entire Match group



Slide Overhaul

The revamped `slide` command utilizes a move-intersect algorithm that delivers smoother, more predictable, and localized edits. This command simplifies the use model, integrating sliding of off-angle and arc routing, and provides new options to improve efficiency.

New Options in the Slide Command:

- Min Corner Size: A fill-in field for minimum 45 degree corner size allowed between two non-parallel cline segments. This field also supports [N] x width values.
- Min Arc Radius: A fill-in field for minimum arc size allowed between two cline segments. This field supports [N] x width values. This value prevents arcs from completely collapsing during slide operations.
- Vertex Action: A drop-down field that controls the action when you select the vertex between two segments during a slide operation or when running the Slide command. A special vertex cursor is shown as an indication when a pick gets the vertex rather than a segment.
- Line Corner – Causes the current angle at the vertex to be split and a new segment is created. The new segment is then active on the cursor and can be modified using the Slide command. This would allow you to change a 90 degree corner into 45 degree, or split any other existing angle. This is very useful to cleanup 90 corners, adjust off-angle corners, or reduce length of existing routes.
- Arc Corner – Causes an arc to be created at the selected vertex. The new arc is then active on the cursor and it can be modified using the Slide command. This is very useful to convert 90 or 45 corners to arcs.
- Move (default) – Causes the vertex to move as both adjacent segments are modified using the Slide command. This is essentially a 2 segment operation.

- None – Prevents any special action when a vertex is selected.
- Auto Join – This option controls the behavior when parallel cline segments meet during a slide operation. The ON behavior of this option causes parallel cline segments to join as they meet during the slide operation, allowing the user to continue the current operation on larger sections of the cline. The OFF behavior of this option does not join parallel cline segments when they meet (unless a click is made), but instead creates new segments to connect the parallel cline segments. By default, the option is ON.

  Holding the CTRL key down during the slide operation gives the opposite behavior of the current setting on the Options form. This is useful to get the alternate behavior of Auto Join during a single edit, without having to switch the settings in the Options tab.
- Extend Selection – This option preserves the connective pattern of multiple cline segments during a slide operation. The ON behavior of this option extends the original selection made during the slide operation to include the two cline segments adjacent to the selection (additional segment on each side). The OFF behavior does not affect the original selection. By default, this option is OFF.

  It is recommended to use the SHIFT key for the ON behavior during specific slide operations. Holding the SHIFT key down during the slide operation gives the opposite behavior of the current setting on the Options form. This is useful to get the alternate behavior of Extend Selection during a single edit, without having to switch the option setting.

  This option is very efficient for sliding tuning patterns or other multi-segment structures when it is desired to keep the basic shape of the cline segments, without having to do a window selection on the segments.
- Arc corners – Extend Selection can be used when sliding a 45/90 degree segment that has arc corners and you want to maintain the arcs while the selected segment slides. This option is similar to the arcs with segments option.

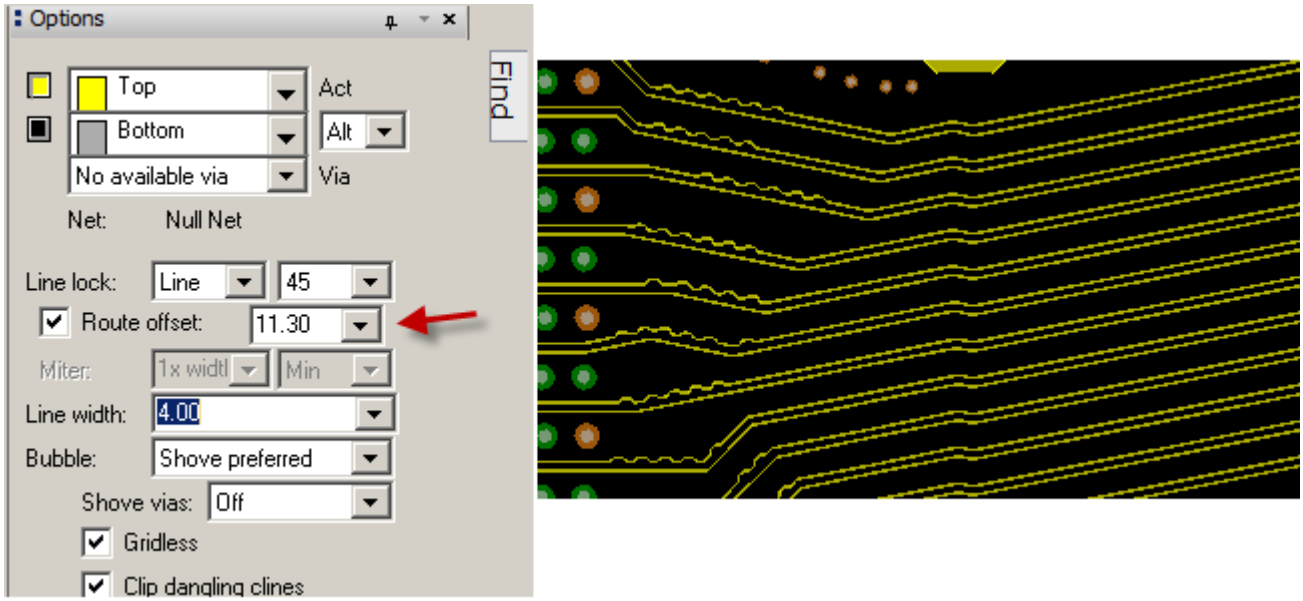
Offset Routing

The Add Connect *Offset* option is designed to primarily address the requirement to route with non-standard angles to help minimize impedance discontinuities while routing across fiberglass substrates.

Function Keys

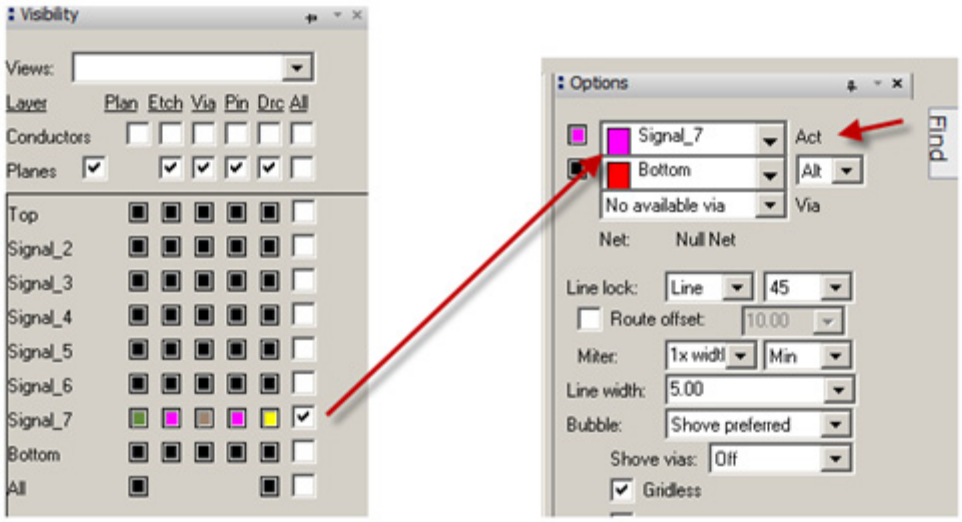
- TAB Key – system defined key used to switch between a soft bend (1st angle increment) and a hard turn (2nd angle increment). Each time you hit the TAB key, it will flip to the other angle.

- *funckey a "pop flip"* - consider creating a user defined function assignment to help you toggle between conventional and offset routing. The letter "a" is used as an example.



Smart Layer Behavior for Add Connect

When using the *Add Connect* command, the active layer field will now automatically synchronize to that of a single visible layer. Previously, any visibility adjustment to limit the display to a single etch layer would require an adjustment to the active layer as well.



Single layer synchronization

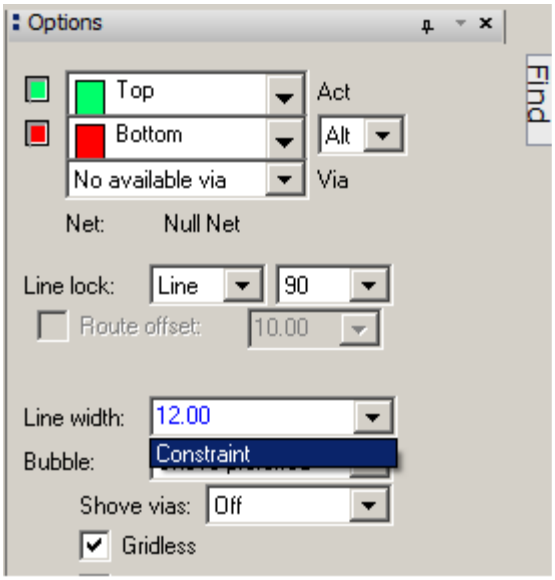
Disable Open Space Routing

By default, the *Add Connect* command generates routes when a pick is made on database elements like pins or vias but also when a pick is made in open or black space. Designers who push the mouse fast and hard frequently make false picks and are forced to *Oops* out of the command and then refine the pick to a logical element like a pin or rat line. Some designers may embrace the open space pick concept when interconnect strategies call for partial routing of buses or interfaces. Since there is no clear preference on the default behavior, a solution driven by a user preference variable is offered. When enabled, the *Add Connect* command rejects any picks made that are not associated with database elements like rat lines, pins, vias, segments, or shapes. The variable setting does not affect multi-line route which is designed to work by making a pick in open space.

You can set the variable `acon_disable_nullnet_route` in Route – Connect in the *User Preference Editor* dialog box.

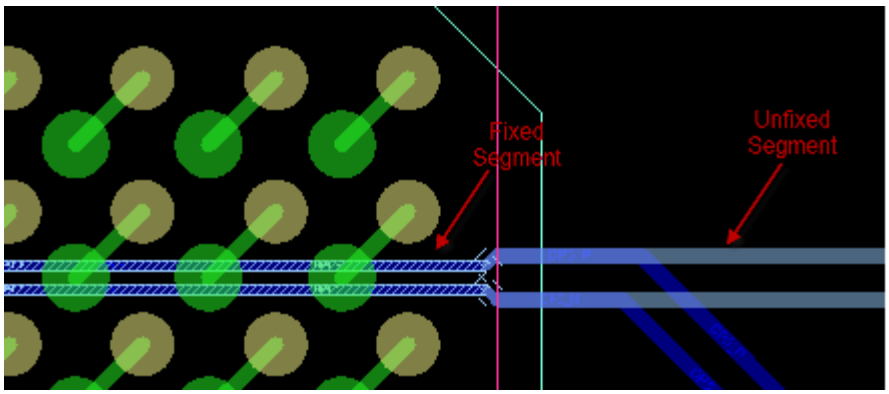
Line Width Retention during Add Connect

Currently, user line width overrides are permitted during the *Add Connect* command but are reset back to constraint-driven when the command is completed. The16.6 release maintains the user setting until they are manually reset. The line width override now appears in blue to represent an override state. You can easily reset to constraint mode by selecting Constraint from the drop-down menu.



Fix Cline Segments

The `fix` command now supports segment based database elements. The command is supported in the verb-noun editing model or in the General or Etch Edit application modes.



Note: Consider using Stipple overlays to distinguish fixed from non-fixed elements.

Copy/Move Cline Segments

The Copy and Move commands are enhanced to support cline segments and other segment database elements.

Unsupported Prototype Menu

The *Route - Unsupported Prototype menu* is added in 16.6 release. The variable support to access the unsupported menus is no longer required. You can check this location periodically for prototype applications.

Auto Interactive Convert Corner (AiCC) Unsupported Prototype

Routing trends associated with high speed interfaces point to an increase in Arc-based cornering requirements. The *Auto Interactive Convert Corner (AiCC)* command improves user efficiency for converting route corners in the Allegro design whether they be are single ended or differential pair based. As with *AiDT*, you have full control of advanced GRE functionality from the Allegro canvas. You can interactively select nets, clines, or segments for conversion to Arc, 45, or 90 degree corners.

Command

You can run the *Auto Interactive Convert Corner* command from the *Route – Unsupported Prototypes Menu*.

Options

The following options are available while running the *AiCC* command.

- Convert Type: Conversion options of Arc, 45, and 90 degrees
- Allow in cns areas: This allows you to control if corner conversion should be performed inside constraint regions. By default this option is set to Yes.
- Preferred Radius Size: Set to desired radius when Convert Type of Arc is enabled.
- Min Radius: Minimum acceptable radius when Convert Type of Arc is enabled.
- Preferred Corner Size: Set to desired corner size when Convert Type of 45 is enabled.
- Min Corner Size: Minimum acceptable corner size when Convert Type of 45 is enabled.
- Allow DRCs: DRC's are permitted for corner conversions.

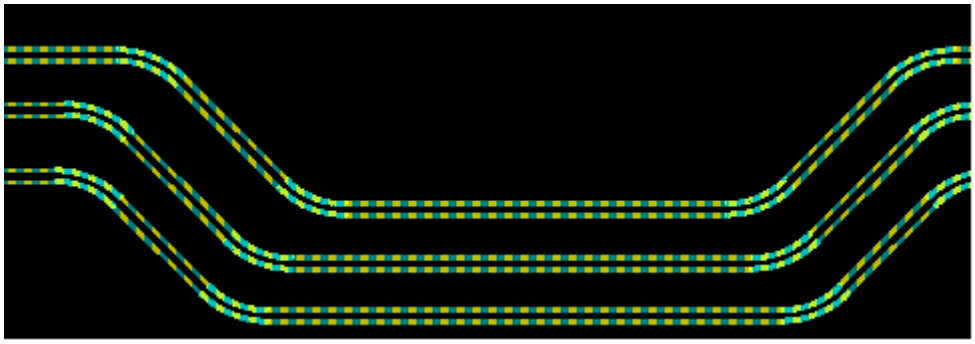
Find Filter

AiCC can be run on existing Nets, Clines or Segments. Hierarchical Groups may also be used to select clines (e.g. Net Classes, Diff Pairs)

Reporting

A viewlog file reports corners that failed to convert.

Figure 3-2 Diff Pair corner conversion to Arc



Productivity Enhancements

This section lists the enhancements made to enhance the productivity in the Allegro PCB Editor.

- Component Alignment updates
- Place Replicate support of Text
- Quickplace - Overlap Components
- Symbol Instance Refresh
- Parameterized Cornering for Rectangular Shapes
- Shape Expansion/Contraction
- Add Circle - Ease of Use Improvements
- Change Radius of Line Drawn Circle
- Thermal width for Xhatch shapes
- Shape Updating
- Shape Messaging
- Embedded Net Names
- Rat Display – End in View Only
- Show Measure Support for Dual Units
- Multiple Constraint Region Assignments
- Move Lines and Text outside Existing Class Structure
- "Snap Pick to" updates
- Status Bar updates
- Select by Lasso or Path
- Highlight Nets associated with Component
- Split Plane Association
- DRC by Window
- Replace Padstack Enhancements

Component Alignment updates

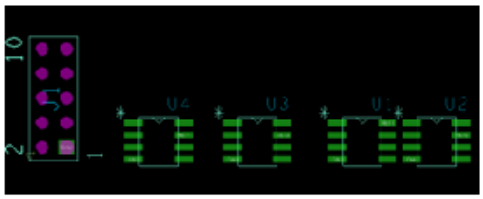
Component Alignment was introduced in SPB 16.3 and now enhanced in 16.6 to support the following new options.

Alignment Edge

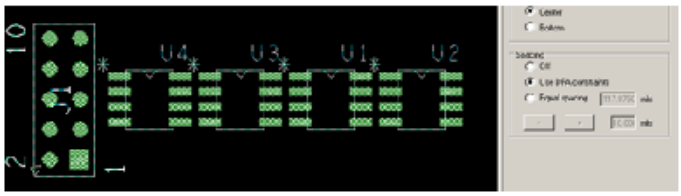
- When aligning vertically, select left or right as the edge to base the alignment on.
- When aligning horizontally, select top or bottom as the edge to base alignment on.

Spacing Options

- Use DFA Constraints - Compresses components in the selection set to the minimum DFA spacing distance.
- Equal Spacing - algorithm computes space between the first and last component of the selection set then divides by the number of components resulting in an equalized spacing gap between each component. Use the increment/decrement controls to adjust component spacing real time.



Before alignment



After alignment with DFA compression

Place Replicate support of Text

The Place Replicate application now supports the processing of component reference designators. The work performed in customizing assembly text or silkscreen to the seed circuit can now be leveraged across the replicated modules.

Quickplace - Overlap Components

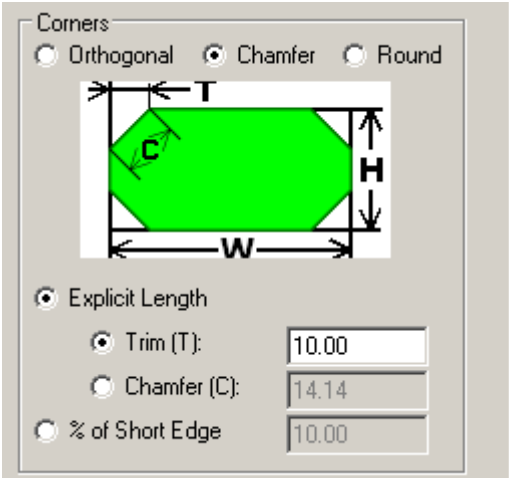
Quickplace is an application used to quickly scatter components around the perimeter of the design or to a room location. By default, components are placed not to overlap each other. As a result, the application may fail to place components if space is not available. A new control option, *Overlap components by* is introduced to improve completion percentages. You can control the amount of overlap. The default value is seeded at 50%.

Symbol Instance Refresh

Support for refreshing a symbol instance is now available in Place Edit Application Mode. Hover the mouse pointer over a symbol then use the RMB context sensitive menu to access the *Refresh Symbol Instance* command. At a particular stage in the design, data related to the symbol(s) may have been deleted; typically the silkscreen outline or text nodes. Perhaps on a board re-spin, conditions change making it favorable to restore the deleted outline/text of specific symbols but not all.

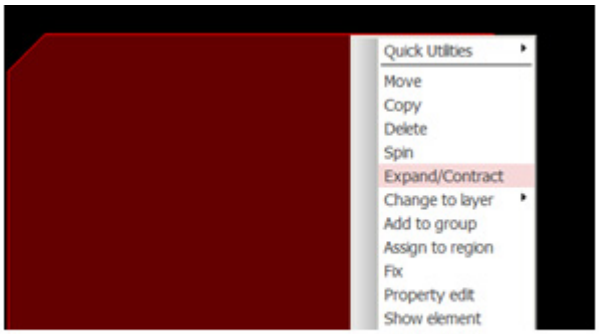
Parameterized Cornering for Rectangular Shapes

The *Shape - Add Rectangle* command is enhanced to support cornering options of *Chamfer* and *Round*. You can control the corner length/radius using either *Explicit Length* values or as a *Percentage of the Short Edge*. When adding a rectangular shape, you have the option to interactively draw the rectangle or use the new *Place Rectangle* using parameterized entries for width and height.

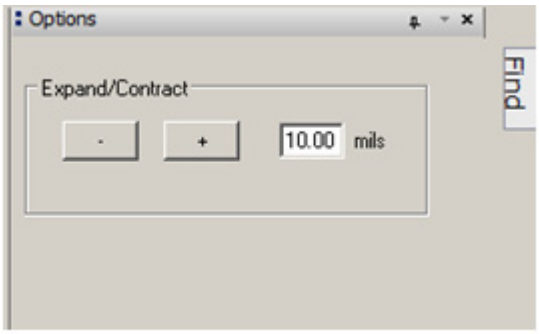


Shape Expansion/Contraction

The ability to contract or expand a shape is available using the General Edit Application Mode. Hover the mouse pointer over the shape then use RMB context sensitive menu to access the *Expand/Contract* command. Use +/- buttons to incrementally change the shape size.



Context menu for expand/contract



increment controls

Add Circle - Ease of Use Improvements

The following ease of use updates are made to commands associated with adding a circle. Relevant commands include *Add Circle*, *Shape Circular* and *Shape Manual Void – Circular*.

Circle creation options

- Draw Circle – mouse guided circle creation
- Place Circle – user guided placement of parameterized circle
- Center / Radius – place parameterized circle at x,y coordinate

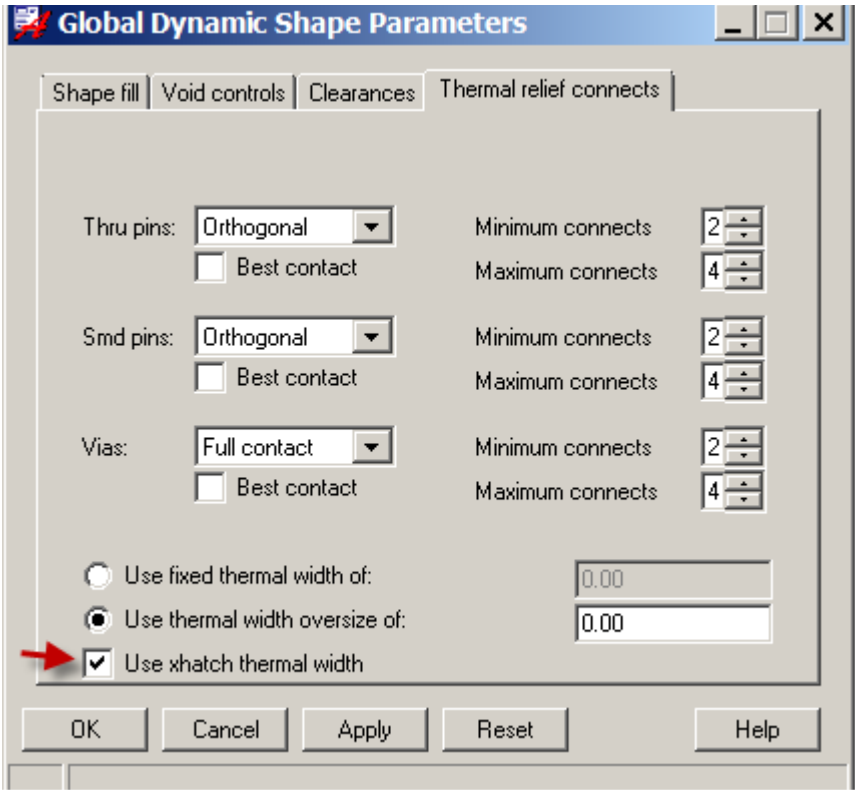
Change Radius of Line Drawn Circle

Use General Edit Application mode to easily change the radius of an instantiated line drawn circle. Hover the mouse pointer over a circle then use the RMB to access the *Change Radius* command.

Thermal width for Xhatch shapes

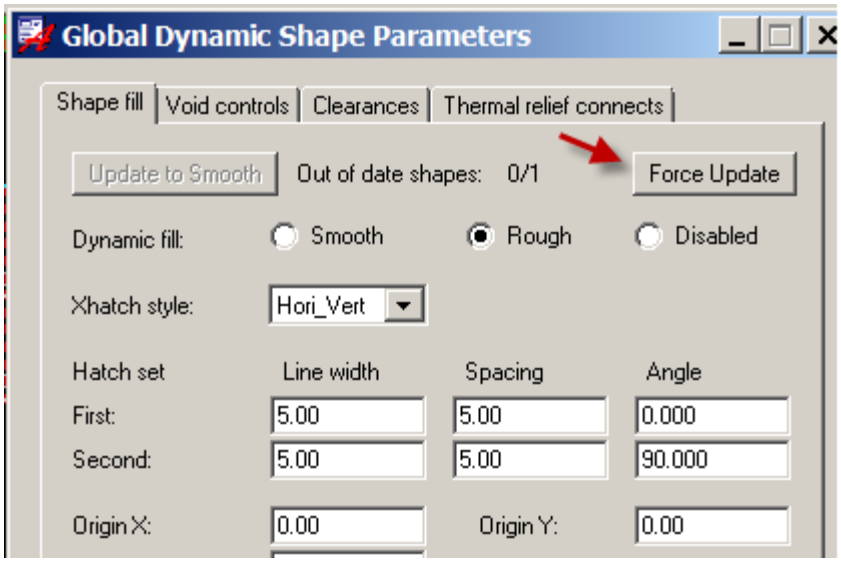
A new dynamic shape option aligns thermal spoke widths used for cross hatch shape applications to that of the line widths used for the actual shape hatching. Normally the thermal

line width is controlled by the MINIMUM_LINE_WIDTH property associated with the net. If the property value changes, the thermal width would be updated. A Flex PCB Designer can now set this option and maintain the integrity of the copper hatched region regardless of line width updates forced by the schematic or property overrides.



Shape Updating

New shape update control is available in the *Global Dynamic Shape Parameter* dialog box. It is designed to force an update on all dynamic shapes.



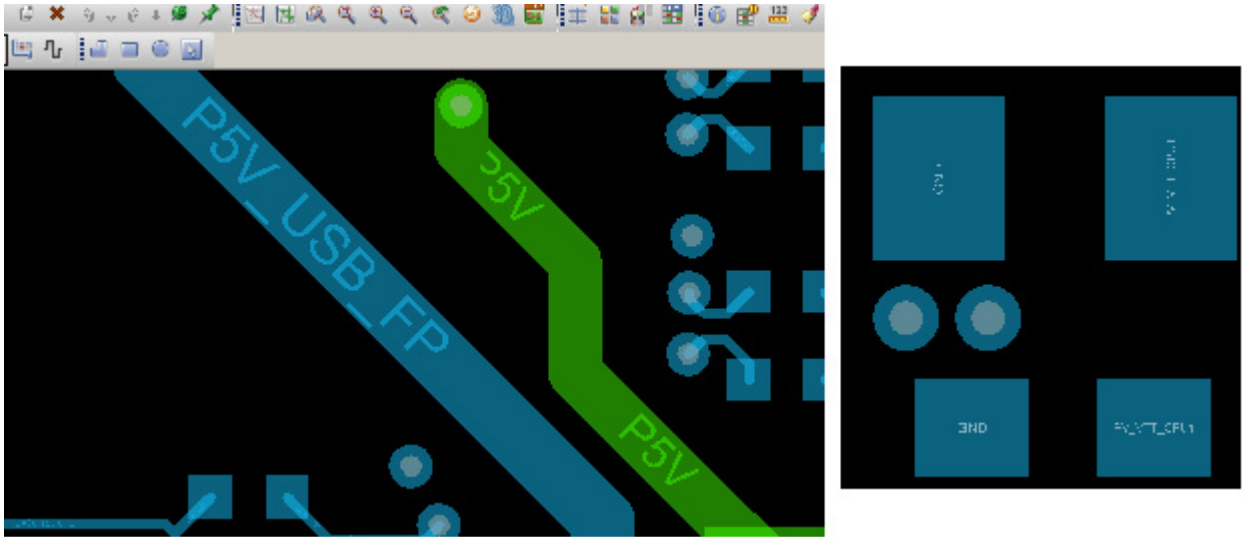
Shape Messaging

A warning message is provided about lost voids when changing a static shape to a dynamic shape.

Embedded Net Names

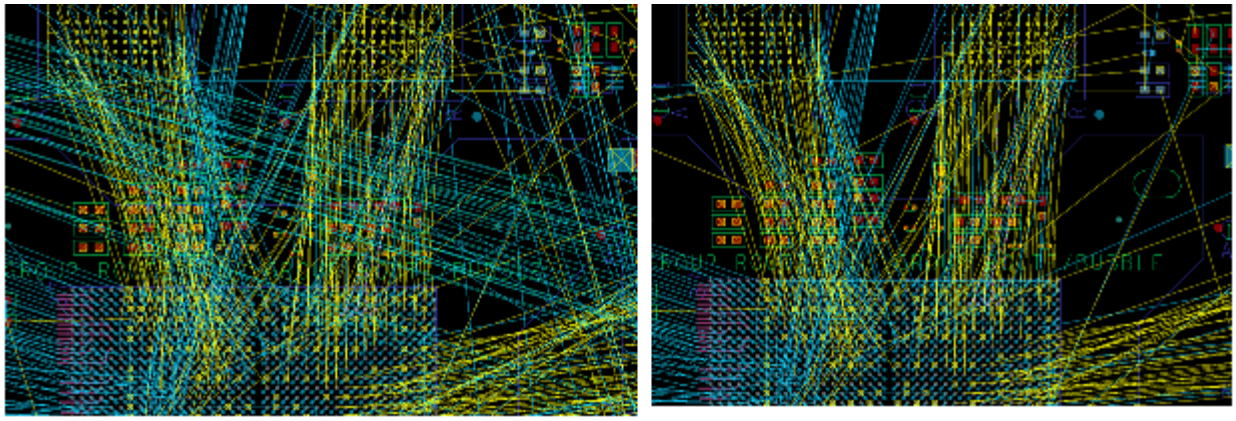
A new graphical display option embeds net names within the cline path, pins, shapes and flow lines. Useful in just about any PCB application, the display of net names will be extremely valuable for those involved in design reviews or board debug. This feature is enabled by default in all PCB products and does require Open GL to be enabled. The visibility controls

for traces, pins and shapes are available by accessing the *Setup – Design Parameters – Display* form.



Rat Display – End in View Only

A new ratsnest display option is designed to reduce the density of rat display in the workspace. Rats seen as pass through, ones not terminating to a pin in view are automatically filtered from the display.



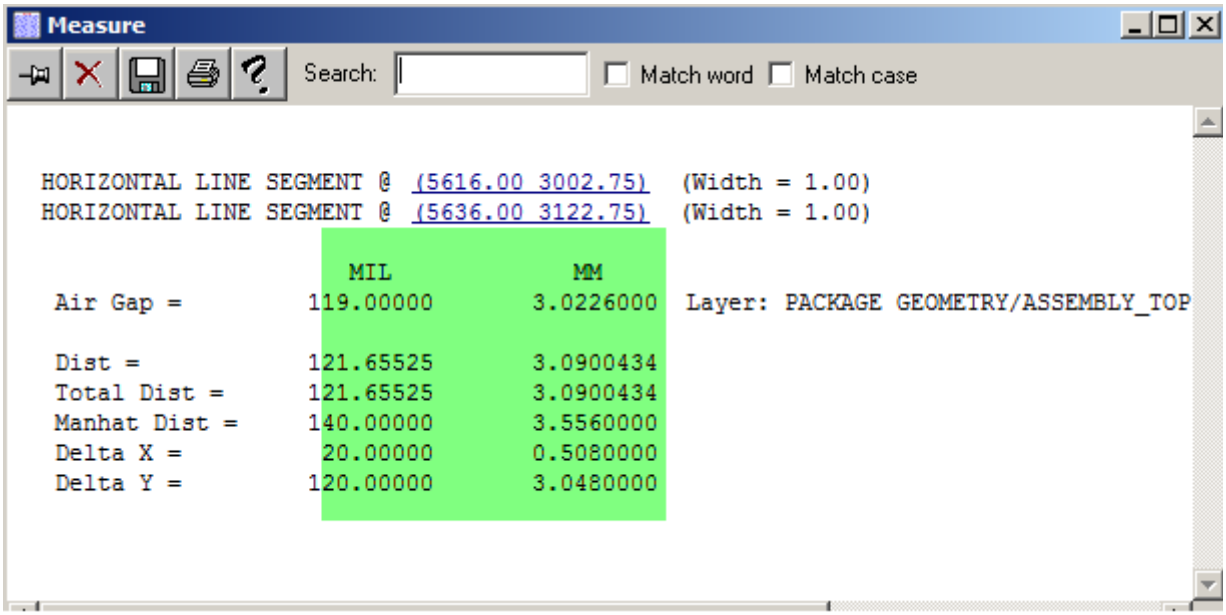
Normal display

End in View Filter

Show Measure Support for Dual Units

The *Show Measure* command now displays results in database and alternate units. To see the alternate unit enable the user preference variable `showmeasure_altunits`.

Show Measure also supports a measurement between padstacks even if a common layer does not exist. (16.5 ISR) This will be helpful when measuring mask related geometry to conductor.



Multiple Constraint Region Assignments

Multiple region shapes can now be assigned to a single region constraint object. Using General edit application mode, pre-select region shapes then use the context sensitive RMB menu to access the *Assign to region* command.

Move Lines and Text outside Existing Class Structure

Lines and text can now be moved outside their present Class-Subclass structure. In previous releases, workarounds using clip board were necessary to accomplish this task. Hover the mouse pointer over the line, text or rectangular element then use the RMB to access the *Change Class/Subclass* command. Select a new class then one of the subclasses within the Class structure from the popup dialog.

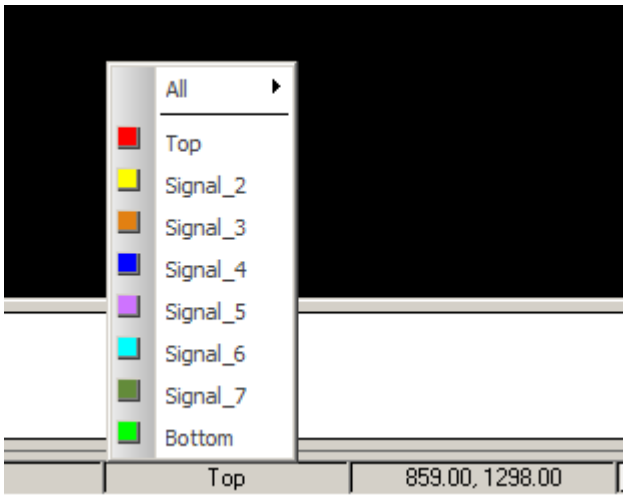
"Snap Pick to" updates

- The snap pick to function is now available on the Edit – Vertex RMB menu.
- Additional snap elements have been added to the RMB menu
  - Rectangle Edge Vertex
  - Rectangle Edge Midpoint
  - Rectangle Edge
  - Shape Center
  - Symbol Center

Status Bar updates

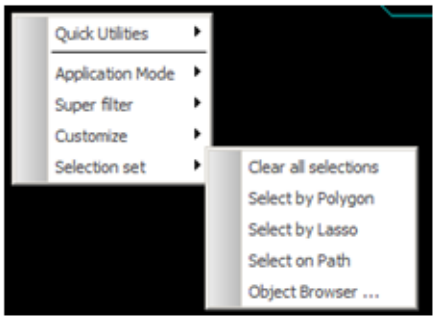
In 16.5, functional responses could be obtained by clicking fields in the status bar. The 16.6 includes:

- Color Swatches have been added adjacent to subclass names
- A selection of a subclass now automatically enables the visibility of subclass (if previously disabled)

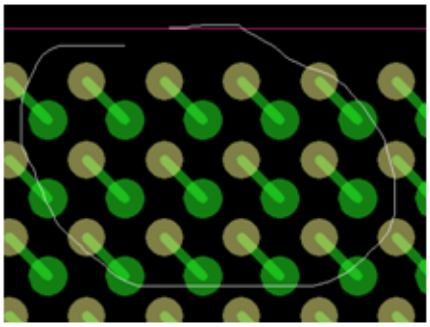


Select by Lasso or Path

Two new selection options are available with commands that normally support temp groups; move or highlight for example. If working in an application mode, you can access these selection options from RMB – Selection Set.



Menu


Lasso


Path

Highlight Nets associated with Component

A simplified method to highlight or dehighlight all nets associated with a component is offered in all applications modes. Hover over a symbol(s) then use the RMB to access the *Highlight associated nets* command. Nets assigned the DC Voltage property are ignored.

Split Plane Association

Net associations to split planes are now stored in the database. This reduces chance of error when re-generating split planes on positive or negative layer. The former use model required re-assignment of net during command which was error prone and cumbersome.

When a split plane is regenerated, the net choice dialog for each shape is set to the default net that will be assigned to the shape. If you click *OK* it confirms the net assignment to the shape. If you wish to select a different net, then select the '*' in the drop-down and then select the correct shape.

If *Cancel* is selected in the net selection dialog, a confirmation dialog with two choices will appear.

- Click *OK* to allow the system to automatically assign nets to the remaining shapes based on database association.
- Click *Cancel* to set all remaining shapes to dummy nets.

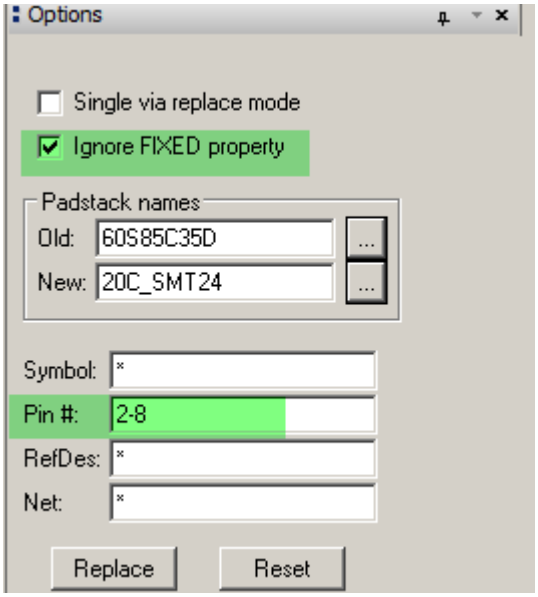
DRC by Window

The *DRC by Window* command is an alternative to running DRC update at the full design level. As the name suggests, the command is limited to checking the elements within the extents of a user defined selection window. On large, highly constrained designs where database performance is problematic, one can simply disable On-line DRC mode if favor of this On-demand method.

The *DRC by Window* command is located in *Tools – Window DRC* or available from the Toolbar.

Replace Padstack Enhancements

- The *Replace Padstack* command is now available as a context menu item when the selection set consists of mixed padstack instances. Prior to 16.6, the selection set would have to be limited to common padstacks. This is available in General Edit Application mode.
- The Options Panel now supports *Ignore FIXED property*.
- The *Pin Number* field has been enhanced to support a range of values



Design for Manufacturing

- IPC-2581 Data Transfer Standard
- Artwork / Film Records Enhancements
- NC Drill Enhancements
- NC Route Enhancements
- Thieving Enhancements
- Associative Dimensioning Updates
- Change Line Font

IPC-2581 Data Transfer Standard

Allegro PCB Editor now has the ability to export and import PCB design data in the IPC-2581 format. The IPC-2581 export allows users to extract PCB design data for manufacturing where artwork, NC drill, NC route, test, and BOM are combined into one single file. Based on the IPC 2581 standard, the user may select the specific types of data to be exported based on the function, such as fabrication, assembly, or test. IPC-2581 data produced by Allegro PCB Editor may also be viewed by using one of the free IPC 2581 viewers available on the IPC 2581 Consortium's web site (http://www.ipc2581.com/index.php/ipc-2581-files).

Allegro also supports the import of IPC 2581 data for the purposes of viewing the generated artwork and comparing that data to the existing film record layers. For more information on the IPC 2581 standard visit the IPC web site at http://webstds.ipc.org/2581/2581intro.htm.

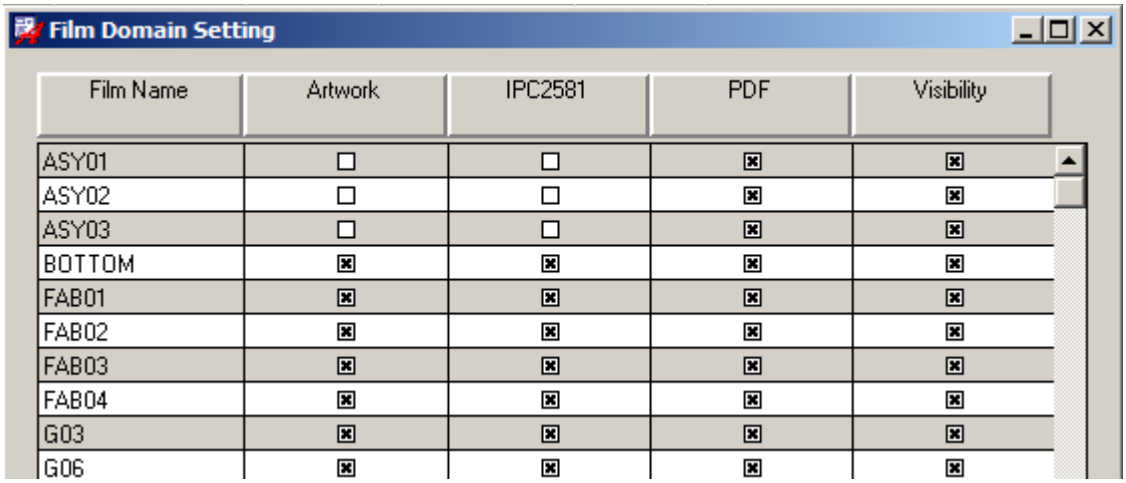
IPC-2581 provides a 21st century approach to transferring PCB design data to manufacturing through an open, neutral, global standard. To learn more about the IPC-2581 Consortium, its charter, to find out who the members are, visit www.ipc2581.com.

Benefits of using IPC-2581 for transferring PCB design data to manufacturing includes:

- Cost savings – through an efficient transfer mechanism (instead of dealing with myriads of files).
- Elimination of unnecessary iterations between design and supply companies.
- Improved chances of first pass success.

Artwork / Film Records Enhancements

- Artwork films can now be designated by domain where they appear. There are four domains available; *Artwork, PDF, IPC2581* and *Visibility*. Access the User Interface by clicking on *Domain Selection*



- New *Draw Holes Only* option available in film record form. PIN and/or VIA CLASS layers must be specified for the film to control which holes are plotted, and the option is not allowed with ETCH layers in the film. The hole that is plotted is a true size hole, and oval or rectangular slot holes are shown with their true shape as well.
- RS274X now supports output of shape with voids overlapping other shapes. No error is generated. "aborting film - Shape with first segment has a void with extents that touches another shape with first segment"
- Film names have been increased from 17 to a maximum of 47 characters.
- Artwork by default will suppress Null pads when unused pad suppression is enabled.
- Photoplot.log now has a warning if un-defined line width is set to 0.
- For new designs initial artwork parameters now defaults to same unit type as board
- Artwork by default will suppress Null pads when unused pad suppression is enabled

NC Drill Enhancements

Creating new drill data will now report the number of holes to the allegro status line. This was previously reported to just the log file.

NC Route Enhancements

- Separate plated versus non-plated files - An option has been added to the NC Route user interface to specify that separate output files are desired for plated versus non-plated routing. When this option is enabled, non-plated routing for both the board and slot holes will continue to be output to a *<name>.rou* file, while plated routing for both the board and slot holes will now be output to a new *<name>_plated.rou*' file. When disabled, all NC Routes will continue to be output to the single *<name>.rou* file.

- Auto-generate tool codes and sizes - The current NC Route functionality requires that the user supply an ncroutebits.txt file that specifies the EXCELLON format tool codes and sizes that will be needed for the routing of board paths and/or slot holes of a design. This requires that the user has detailed knowledge of the routing requirements of the design, and also that the tool sizes need to be in the specified in the EXCELLON format output units as opposed to the more familiar units of the design in question. In 16.6, if an ncroutebits.txt file is NOT found, the tool code and size information will be automatically determined and used. The information will also be output to an ncroutebits_auto.txt file for reference, similar to the nc_tools_auto.txt file generated by NC Drill in the same situation. The ncroutebits_auto.tx' file itself will never be read as currently named by NC Route. It could be renamed though to ncroutebits.txt for any subsequent executions of NC Route to bypass the auto-generation.

Thieving Enhancements

- Thieving outline - New *Rectangle* option added to list. If selected, the user is required to make only two digitalizations of a rubber-banded rectangle.

- Thieving style - A new *Line* setting has been added to the existing ones of *Circle* and *Rectangle*. The fill elements will be created as actual cline/line segment entities as opposed to via entities for *Circle* or *Rectangle*. The options settings for both Size X and Size Y must be specified where the lesser value will be the width of the segment, and the greater value the length of the segment. Therefore horizontal or vertical segments can be specified as fill elements, but not angled segments.

Note: The rounded endpoints of the segment are added to the specified length value.

- All etch layers - The specified thieving will be re-generated and added for each positive etch layer of the design.

- All soldermask layers - The specified thieving will be re-generated and added for each soldermask layer of the design.

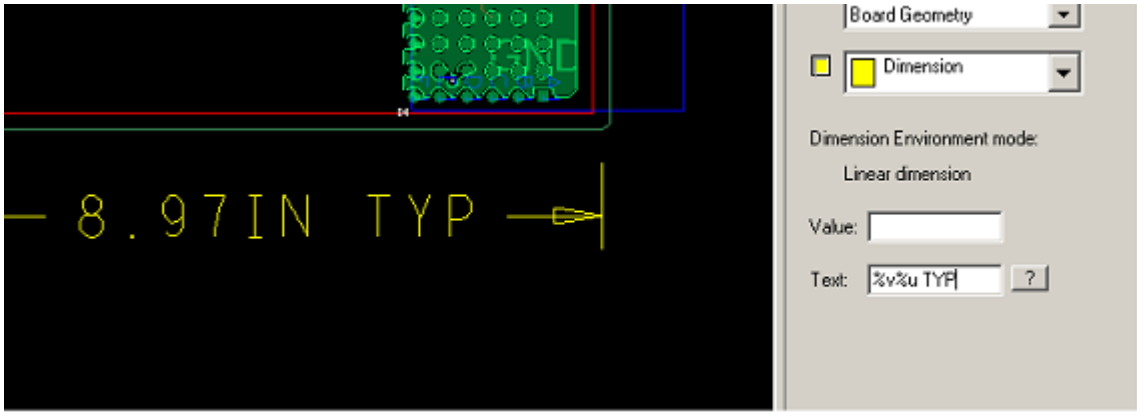
Associative Dimensioning Updates

- Customized Dimension Text – The options form for the various types of dimension creation and *Change text* now supports a *Text* field in addition to the standard *Value* field. Essentially any user entered *Text* string overrides the computed value that is normally applied. Any alphanumeric characters are allowed in the specified *Text* string. For example, one could create a linear dimension with value text of 'XYZ' by entering it in the *Text* field. The *Text* field supports the following formats for entry

%v	Insert the actual dimension value in the text. Either the normal computed value, or the *Value* typein override if one was specified.
%u	Insert the appropriate units indicator in the text for the dimension value (e.g. 'IN' for inches or 'MM' for millimeters).
%%	A guaranteed way to get an actual '%' character in the string, especially if the next character is otherwise a recognized substring insertion.

EXAMPLES

XYZ	XYZ
Value is %v	Value is 1.0
Value is %v %u	Value is 1.0 IN
%v%u	1.0IN
%v is the value	1.0 is the value



- Balloon Dimension update – Instance parameter support is now available for balloon leaders. This allows different types of balloons (circles, squares …) to be used in the same design.

Change Line Font

The ability to change line font is available in General Edit Application Mode. Hover over a line then use the RMB context sensitive menu to access the *Change Line Font* command.

Team Design (Partitioning) more Flexible in 16.6

New features associated with Physical Team Design are intended to reduce the number of.DPF (design partition file) import/export iterations the PCB Design team experiences in the typical physical team design flow. By permitting Partition Designers to place and route across partition boundaries as well as having constraint editing privileges, design schedules can be significantly reduced as a result of less interrupts in the flow.

- Flexible Boundaries
- Constraint Editing
- Differences Report
- ECO Wizard

Flexible Boundaries

Designed to reduce the number of iterations between the Master and Partition Designers, it's now possible for Partition Designers to move components or route signals outside their respective boundaries. The Master Designer controls whether boundaries are flexible enabling the new Workflow manager option called *Soft Boundary*. This behavior is an all or none condition for the team.

Prior to 16.6, components could always be moved outside the boundary of a partition to allow the user more space to work in the partition, but when the partition was exported back to the Master Designer, components outside the boundary were ignored. When soft boundaries are enabled those components moved outside will now be saved during the export.

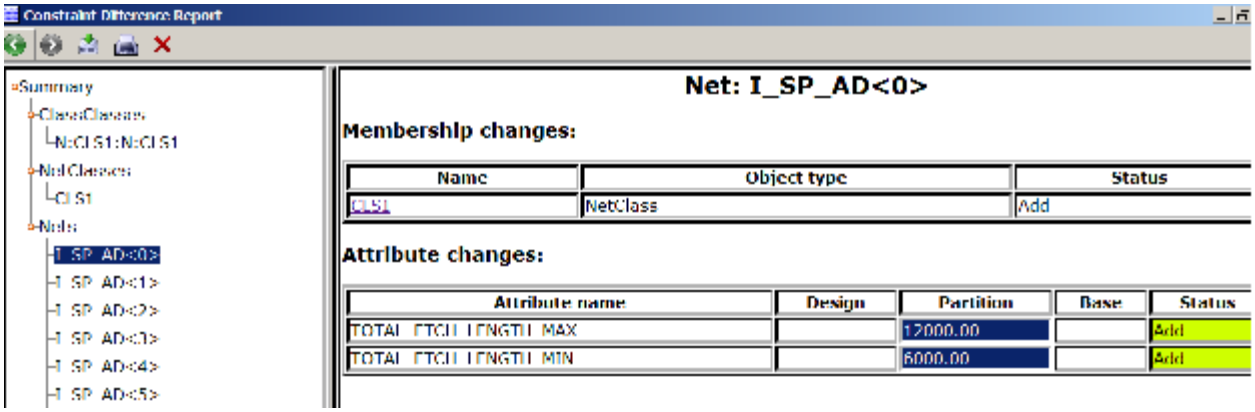
Constraint Editing

Partition Designers are now permitted to edit Physical, Spacing and Electrical Constraints. The Master Designer controls whether constraint editing privileges are granted to the team by enabling the new Workflow manager option called *Edit_cns.* This behavior is also an all or none situation.

Design level constraint editing is not permitted in partition databases.

Differences Report

Compare constraints differences between Master and Partition files using the *CNS_Report* function available in the Workflow Manager.



ECO Wizard

Available in the workflow manager, the ECO wizard is designed to help streamline the process involving new netlist submits. This entails importing all outstanding partition databases, netlist import then re-export of partition files.

Embedded Component Design

With increased market demands for smaller and lighter products, improved performance and higher speeds, it may become necessary to consider the embedding of passive or even active components within the inner substrates of the PCB. Phase I of Embedded Component Design was introduced in the 16.5 release. It offers mounting methodologies of direct and indirect attachments. Phase II enhancements in 16.6 include:

- Dual Side Contact Components
- Vertically Placed Components
- 2 Layer PCB Support
- Suppression of Unassigned Indirect Vias
- New Embedded Cavity DRCs

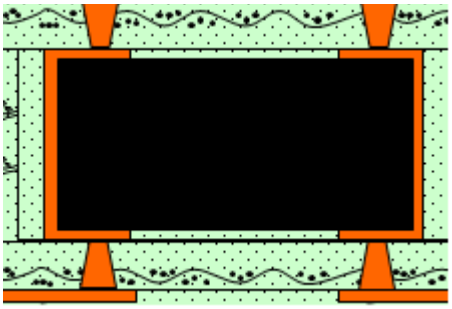
Dual Side Contact Components

The use of dual-sided contact components when placed on internal layers of the PCB allows connections to be made from either side of the device. One of the benefits of using this emerging technology is the reduction of core vias that may have been used to make connections from the component to either side of the PCB. Symbols targeted for dual side applications must have the property DUAL_SIDED_COMPONENT applied in the Allegro Symbol Editor. The associated padstacks of the symbol must have a begin and end layer pad defined.

When the symbol with the dual sided property is placed, the begin pad defined in the padstack definition is mapped to the inner layer the component is placed on. The alternate pad, defined as the end pad at the definition level, is mapped to the layer closest to the top of the component based on the component height.

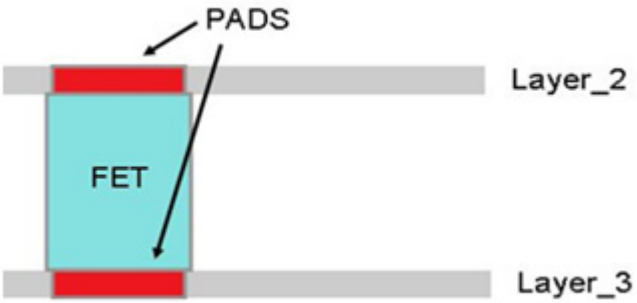
Existing Allegro embedded setup methodologies are fully supported; direct or indirect attach as well as body up/down. Since the stackup is unlikely to be constructed with material

thickness that aligns with the component height, it's likely the indirect attach method is used for this technology.



Vertically Placed Components

The DUAL_SIDED_COMPONENT property can be leveraged to support vertical component applications. Apply the property DUAL_SIDED_COMPONENT to the symbol definition. Assuming a two pin component, map pin 1 & 2 to unique padstacks each with a Begin or End layer pad defined. The base layer is established using the *Embedded Layer Setup* form. The alternate layer pin is determined based on the value of the package height and stackup construction.



2 Layer PCB Support

By default, the Top and Bottom stackup layers do not support the placement of embedded components. When an attempt is made to change *Embedded Status* to either *Body up* or *Body down*, the system will prompt the user accordingly. To help facilitate the requirement for placing components between the Top and Bottoms layers, Allegro now supports the placing of components directly on the dielectric layer. This requires the user to name the dielectric layer(s) prior to invoking the *Embedded Layer Setup* form.

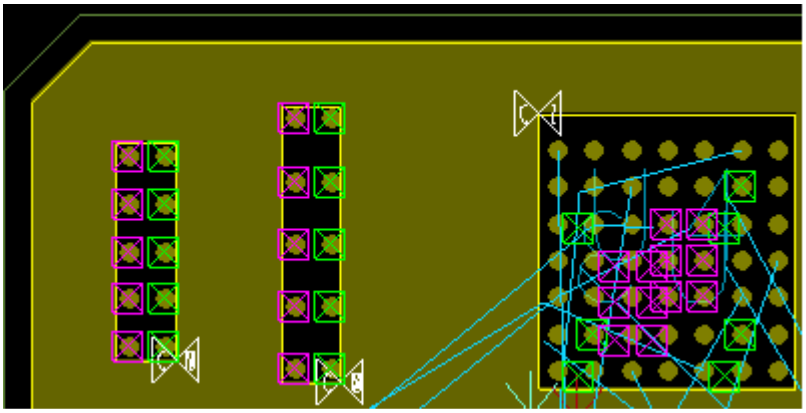
Suppression of Unassigned Indirect Vias

The suppression of unassigned indirect vias is now supported by assigning the property EMB_INDIRECT_VIA_SUPPRESS to the Component Definition, Component Instance or Symbol Pin. If a component is placed on an *Indirect Attached* embedded layer, this new property suppresses ALL via pads associated with the component if the PIN is not on a named net. The indirect attach via pads will only be restored if:

- The symbol pin changes to a named net
- The symbol is moved to a layer which is not indirect attach
- The property is removed

New Embedded Cavity DRCs

Max cavity size and max cavity component count were offered as reports in 16.5 and are now available as DRCs in 16.6. Fab houses supporting embedded component manufacturing offer design guidelines on cavity usage.



Database & Misc Enhancements

- Pastemask update
- Generic Tech File (Cross Section Neutral)
- Net Group Constraint Object
- New Design Defaults
- Find Filter update
- Plotting Improvements
- Buried/Blind via Generator update
- Design Re-Use Modules
- New Variables
- New Properties
- Modified Properties
- Reports
- IDF Out
- Fabmaster Output
- Symbol Export
- New Extracta command line options
- New DBdoctor command line options
- New Dbstat command line options
- Switchversion
- Dump Libraries
- Data Migration
- Downrev to 16.5
- Database Diary
- Performance Improvements
- Skill Enhancements

Pastemask update

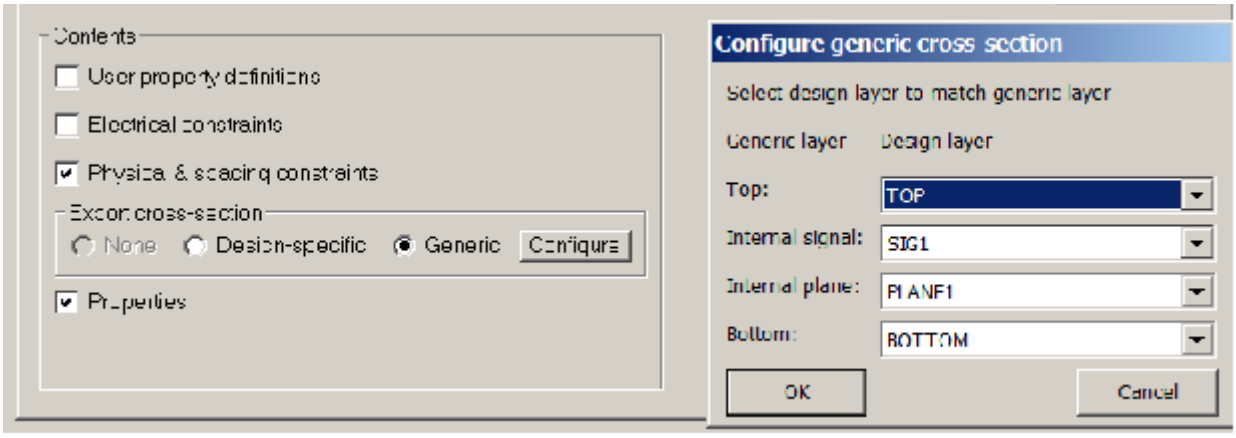
The Pastemask to Pastemask DRC now checks the Package Geometry/Pastemask_top shapes of the same symbol.

Generic Tech File (Cross Section Neutral)

A generic tech file is comprised of 4 by-layer values for all Physical and Spacing CSet constraints. These 4 values are not defined for any specific layer name but are associated with the layer types (Top, Internal Signal, Internal Plane, and Bottom). When the generic tech file is imported into a design, the values will populate all layers of the appropriate type in the target design. For example:

Layer Type (in Generic Tech File)	Layer (in target Design)
Top	TOP
Internal Signal	SIG1, SIG2, SIG3, SIG4
Internal Plane	PWR, GND
Bottom	BOT

When considering this style of tech file, it may be best to use the export function to create the base tech file. The graphic below is from the *File – Export – Tech File* command in Constraint Manager, The configure UI can be used to map specific layers to the Generic Types of Top, Internal signal, Internal plane or Bottom.



Net Group Constraint Object

A new net grouping mechanism has been added in 16.6 called NET_GROUP. Essentially, the NET GROUP replaces the BUS object. Cadence recommends that back-end tools (Allegro, APD and SIP) migrate to NET_GROUPS over BUSES and reserve bus groups to the front-end tools. While back-end users can still create the BUS constraint object using Edit Property, those created in the front-end Cadence tools will be marked as read-only in the back-end tools (you will not be able to delete them or add or delete members).

The Net Class is still supported and should be regarded as a relational constraint object.

New Design Defaults

New designs can be automatically seeded with a default template design or just default units/accuracy. A template design can contain anything; units/accuracy, parameters (including colors), constraints or physical data. To utilize a default template design methodology, place in a location specified by the `wizard_template_path` variable a design of the format:

- new_default.<ext>
- where <ext> is one of brd, dra, pad, mcm, or sip
- example = new_default.brd

You can instead choose to set only default units and accuracy in new designs by using environment variables. Refer to the *new_design* section of the *User Preference Editor*. The simplest approach is to use the *new_units* and *new_accuracy* to set the starting units for all design types. You can also set unit/accuracy by product types via additional env variables (Allegro, APD, cdnsip, pad_designer).

Find Filter update

The find by name section of the *Find Filter* has been updated to support hierarchical database objects. (Match group, Net group, Net class, Pin pair, Diff Pair, Region)

Plotting Improvements

PDF now supports the mirror setting in the artwork film record. (16.5 ISR)

Windows plot setup parameters now detects Allegro design units change and adjusts its settings.

Buried/Blind via Generator update

Both the auto and manual bbvia generation dialogs now can support generation of uvia padstacks in products that support uvias.

Design Re-Use Modules

- Import/export module will now preserve fillets when the manual fillet model is enabled in the design.
- 5X Support - Design Reuse modules can be stored in the appropriate 5x physical view that corresponds to its schematic design section. This feature is enabled by default and is the first location searched for design reuse (mdd) files. It can be disabled by setting the env variable modules_no_5x_support.

To use Allegro must read the `.cpm` file (via Allegro's *-proj* command line option) having Allegro start from *projmgr*. Allegro searches all libraries defined to locate the available set of `.mdd` files. Each physical view directory can specify at most one module (`.mdd`) file. In the `.mdd` file the current mdd is specified by the `master.tag` present in the view directory. The contents of this file must be the mdd file to use. We ignore the file extension since users sometime keep a brd with the same name in this directory. Example you have a module called ddr.mdd in the view. You need to have a `master.tag` in the same directory containing the name ddr`.mdd` or `ddr.brd` (or even `ddr.mcm`).

New Variables

- `place_text_filename` - allows overriding default output file name associated with the export placement function.
- `showmeasure_altunits` – Enable to have Show Measure report dual units.
- `ok_net_one_pin` - Single and No Pin net report now supports this net level property to suppress the report of nets where this is OK.
- `dump_library_directory` - dump libraries now allows the user to specify via this variable, where its output should be stored. Ideally this should be a location relative to current project directory.
- `wizard_template_path` – source location for template files (`.brd, .pad, .mcm, .sip, .dra`).
- `new_template_with_last_design` - Restores 16.5 capability by using the units and accuracy of the previous design to seed a new design.
- `allegro_new_accuracy` – specifies database accuracy on new boards.

- `allegro_new_units` – specifies database units on new boards.
- `modules_no_5x_support` – Disables re-use module 5X physical flow.

New Properties

- OK_NET_ONE_PIN - Single and No Pin net report now supports a net level property to suppress the report of nets where this is OK.
- DUAL_SIDED_COMPONENT – embedded component property for dual side contact. It can be added in the symbol editor at the design level and when the symbol is compiled into a psm it will be promoted to the definition.
- EMB_INDIRECT_VIA_SUPPRESS – use to removal symbol pins from embedded components (indirect attach method)
- DYN_XHATCH_THERM_WIDTH - property set on the dynamic shape to allow cross-hatched dynamic shapes generate thermal clines widths based upon the shape's cross hatch width. You should normally control this property via the Dynamic Shape dialogs.

Modified Properties

- VIA_AT_SMD_THRU - can now be added to pins in Symbol Editor
- LIBRARY_PATH - now visible (it existed in previous releases as a hidden property). It is a string value present on symbol definitions and modules (new for 16.6). It is used by the Symbol Library Path Report. For module databases (mdd) created with 16.6, this property is present at the design level and reports the board, mcm, or sip file location that was used to create the mdd file.
- All properties that were supported at the BUS level are also now supported in the NET_GROUP level. Many of these properties support constraints.
- IC_DESIGN_NET_NAME (SIP and APD) - now supported on a component and function definitions.
- IDX_EXCLUDE - can now be added to rectangles and shapes.

Reports

- Single and No Pin net report now supports net level property (OK_NET_ONE_PIN) to suppress the report of nets where this is OK.
- Net Loop – Detects loops or redundant circuitry associated with single or multiple layer etch configurations. DC nets and nets with over 100 pins are excluded from processing.

IDF Out

The *panel outline* has been added to the filter list of objects that can be excluded during IDF Export.

Fabmaster Output

The *File – Export* menu now supports *Fabmaster out*.

Symbol Export

SiP-based feature *Symbol Export to Spreadsheet* now available in PCB Editor.

New Extracta command line options

`-A`: list all database attachments,

`-a <name>`: extract specified database attachment.

`-l <logname>`: override extract.log file name and location

New DBdoctor command line options

`-shape_update` - update out of date dynamic shapes

`-force_shape_update` - force update of all dynamic shapes

Note: DBdoctor now creates a backup when used in uprev mode.

New Dbstat command line options

`-e` - report editing time and who saved the design last

Switchversion

On Windows, Switchversion's file association option now works with UAC enabled.

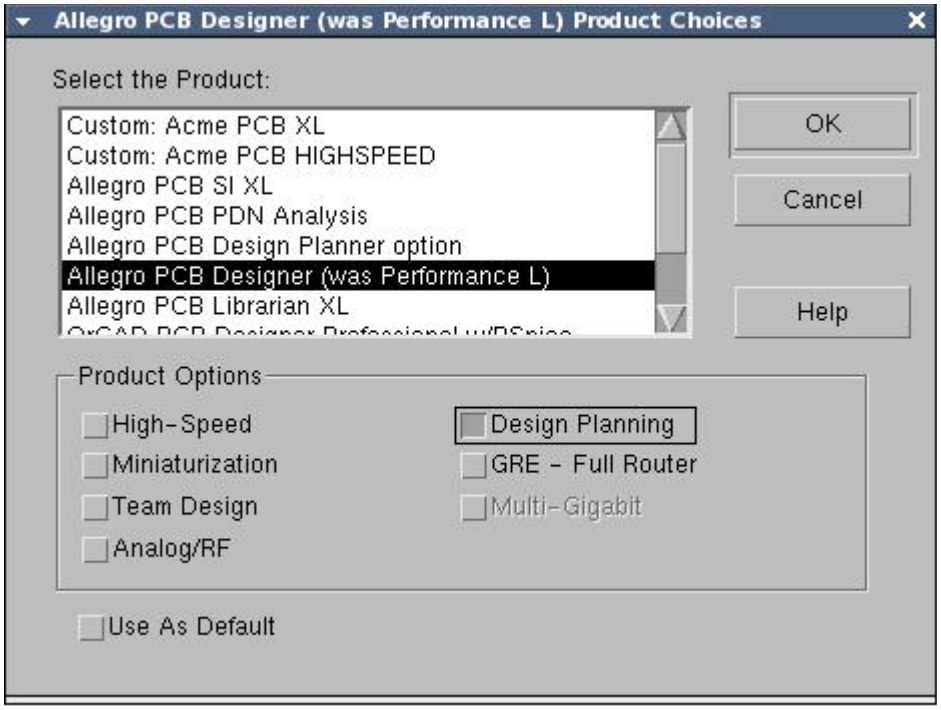
Dump Libraries

Dump libraries now allows the user to specify via an env variable, `dump_library_directory`, where its output should be stored. Ideally this should be a location relative to current project directory.

Product Selectors

- The Product Chooser User Interface now supports license caching to improve startup performance. This requires enabling the variable `allegro_license_caching`.
- The variable `license_nolegacy` when set will filter from the *Toolswap* command any product with legacy in its name. This is also available in 16.5.
- User Defined Product Packages - SPB Marketing implemented a new product packaging scheme in 16.5 that defined a base product and multiple options. Previous releases product packaging was based upon a tiered set of products where product options were secondary. CAD administrators have expressed a desire to package the base product with one or more options into single product. For example, this allows them to recreate the "Allegro PCB XL" product present in previous releases. It also lessens the possibility that there users might select the wrong mix of options for their design work. Basic requirements include following:
  - A customer site based product configuration file based upon CDS_SITE: license_packages_<product>.txt
    - where <product> is executable name (e.g.Allegro, APD or cdnsip)
    - Example: for PCB Allegro - license_packages_allegro.txt
  - Locate the file via CDS_SITE methodology; specifically via Allegro PATH variable LOCALPATH (default) which has the resolution:
    - <HOME>/pcbenv
    - <CDS_SITE>/pcb (also called ALLEGRO_SITE)
  - The configuration file allows the user to specify one or more User Product Packages that consist of:
    - A user product name
    - A base Cadence product
    - Zero or more Cadence options that are available for the base Cadence product.

- The UI shows customer configurations (exclude default Cadence configurations) in the Cadence Product Chooser.



- User Config file for above example

#filternocadence

Package Acme PCB XL

License Allegro_performance

Option Allegro_PCB_Highspeed_Option

Option Allegro_PCB_Mini_Option

Package Acme PCB Highspeed

License Allegro_performance

Option Allegro_PCB_Highspeed_Option

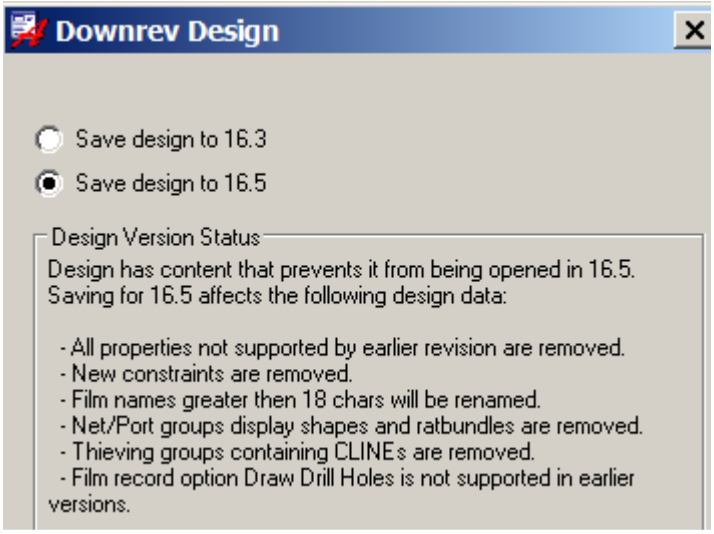
Data Migration

- Obsolete environment variables `display_shapefill` & `display_shapefill_analysis` are removed from the *User Preference Editor* form.

- Allegro is more aggressive in preventing VOLTAGE nets being added to BUS and MATCH_GROUP objects since it may cause performance problems.
- Disallow the backslash (\) as part of net names. An environment variable, `legacy_character_set` can be set to enable the old mode.
- A new net grouping mechanism has been added in 16.6 called NET_GROUPS. Cadence recommends back-end tools (Allegro, APD and SIP) migrate to NET_GROUPS over BUSES and reserve bus groups to the front-end tools. While back-end users can still create buses, those created in the front-end Cadence tools will be marked as read-only in the back-end tools (you will not be able to delete them or add or delete members).

Downrev to 16.5

Downrev to SPB16.5 is supported from the *File – Export* menu. As always, carefully consider the impact of downrev before commitment.



Database Diary

The *database diary* is now available in the PCB Editor. (currently in APD/SiP products)

It can be used to maintain user comments related to design activity and milestones.

You can access this command from *Tools – Database Diary.*

Performance Improvements

~ 2x improvement with Testprep and Autosilk commands.

Skill Enhancements

As always you should check `<cdsroot>/share/pcb/examples/skill/DOC` for what new functions are available in this release.

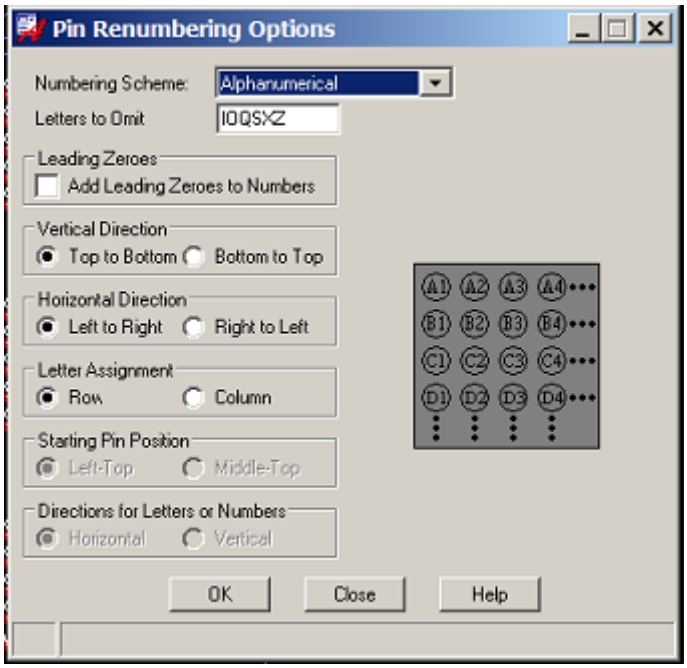
Multiline Skill input is now supported in the Skill development window. This is useful if you need to cut-n-paste a Skill code block into this Window. The *more>* prompt in the Skill window indicates that you are in multi-line mode. If you accidentally enter this mode and need to return to normal Skill input hit the `Esc` key followed by `Enter`. Typical means of entering this mode are due to mismatch parenthesis or double quotes.

Symbol Editor Enhancements

- Renumber Symbol Pins
- Symbol Editor - Import .CSV pin files

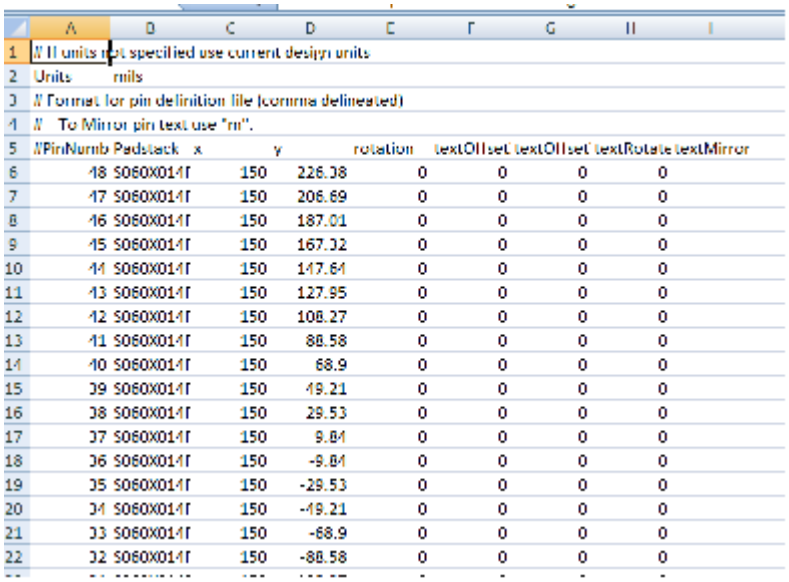
Renumber Symbol Pins

The Symbol Editor has been enhanced with a new utility designed to automatically renumber pins based on positional qualifiers. The path to the utility is *Layout – Renumber Pins*.



Symbol Editor - Import .csv pin files

The Symbol Editor now supports both exporting and importing of pin based .CSV files. The format of the file supports: pin number, padstack name, x position, y position, rotation, text offset x, text offset y, text rotate, mirror.



	A	B	C	D	E	F	G	H	I
1	# If units not specified use current design units								
2	Units	mils							
3	# Format for pin definition file (comma delineated)								
4	#	To Mirror pin text use "m".							
5	#PinNumb	Padstack	x	y	rotation	textOffset	textOffset	textRotate	textMirror
6	18	SO60X014T	150	226.38	0	0	0	0	
7	17	SO60X014T	150	206.69	0	0	0	0	
8	16	SO60X014T	150	187.01	0	0	0	0	
9	15	SO60X014T	150	167.32	0	0	0	0	
10	14	SO60X014T	150	147.64	0	0	0	0	
11	13	SO60X014T	150	127.95	0	0	0	0	
12	12	SO60X014T	150	108.27	0	0	0	0	
13	11	SO60X014T	150	88.58	0	0	0	0	
14	10	SO60X014T	150	68.9	0	0	0	0	
15	09	SO60X014T	150	49.21	0	0	0	0	
16	08	SO60X014T	150	29.53	0	0	0	0	
17	07	SO60X014T	150	9.84	0	0	0	0	
18	06	SO60X014T	150	-9.84	0	0	0	0	
19	05	SO60X014T	150	-29.53	0	0	0	0	
20	04	SO60X014T	150	-49.21	0	0	0	0	
21	03	SO60X014T	150	-68.9	0	0	0	0	
22	02	SO60X014T	150	-88.58	0	0	0	0	

Preparing for the 17.0 Release

This release (16.6) will be the last version that will allow designs (boards, mcm, symbols and padstacks) created in releases earlier then 11.0 to be upreved to the current release. For these old design versions, you must have an OS (Sparc Solaris or AIX) with a Cadence Allegro install to successfully perform a uprev of designs older than 11.0. With 17.0, Cadence will still be able to uprev these old customer designs but even this capability will be discontinued when 16.6 is EOL.

As part of 17.0 adoption, if you have pre-11.0 designs you may need to access, you should either:

- Uprev these designs to16.0 if you plan to have a need to continue to access them.
- Provision a legacy system (Sparc or AIX) with 16.6 and preserve it as a uprev system.

Tips:

- The batch program, dbstat, can be used to report the version of any Allegro database. It supports wildcards so it can be used to report the version of all databases in one directory.
- The batch programs, *uprev* and *uprev_overwrite*, can be used to bring databases up to the current Allegro software version. They both support a recursion option (see documentation) that allows them descend a directory hierarchy, updating any Allegro designs found.
- None of the these batch programs requires a Cadence license.

As a summary of the initial Allegro release supported on a "per platform" is listed below. These platforms will be unable to open or uprev a database older than their first release number.

Platform	First Release
Sparc	1.0
Windows	1.0
Linux	4.0
AIX	4.0

RF PCB Enhancements

In this release several enhancements have been made in RF PCB to increase your productivity.

- Layout Enhancements
- Autoplace Enhancements
- Via Exchange Between Allegro PCB Editor and ADS
- Miscellaneous Enhancements

Layout Enhancements

A major enhancement is made for snapping. In 16.5, when you snap an RF component to a non-RF component pad, you can only snap to the connecting point (usually is the center of the pad). Sometimes users want to connect RF components with non-RF components at the edge of a pad. This results in many RF commands need to be enhanced to support the snapping to pad edge functionality. This module includes:

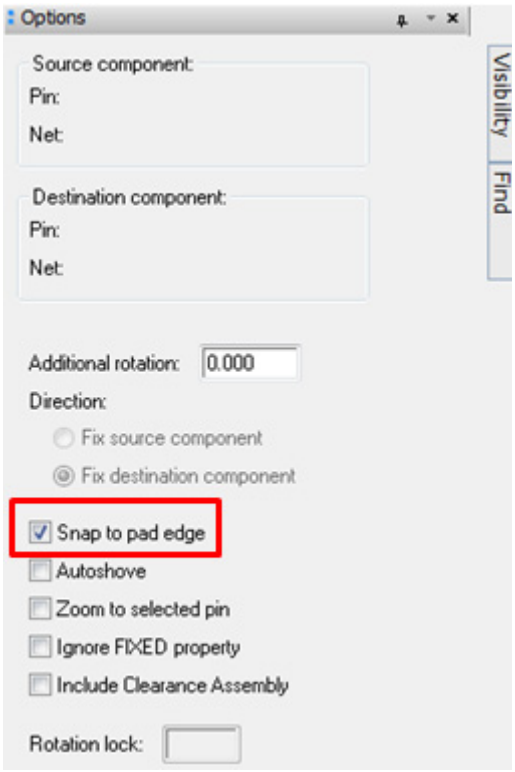
- Snap Enhancements
- Add Connect Enhancements
- Modify Connectivity Enhancements
- Add Component Enhancements
- Scaled Copy Enhancements
- Single Segment Connection
- Route with Any Angle Bend

Snap Enhancements

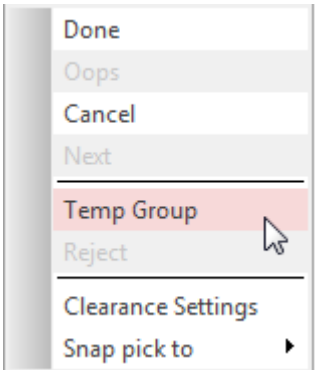
You can use this functionality to snap an RF component to a non-RF component, or a non-RF component to an RF component or even a non-RF component to another non-RF component based on the connectivity.

There is a *Snap to pad edge* check box on the form which is used for snapping to a specific edge of a pad.

Note: When you snap a non-RF pad edge to another non-RF pad edge, this may result in violations for manufacturing/assembly, so you've to manually check all those violations.



You can also select some components as a temp group to snap together. During the snap command, RMB select Temp Group and then click a pin to snap, the whole temp group will be moved together.

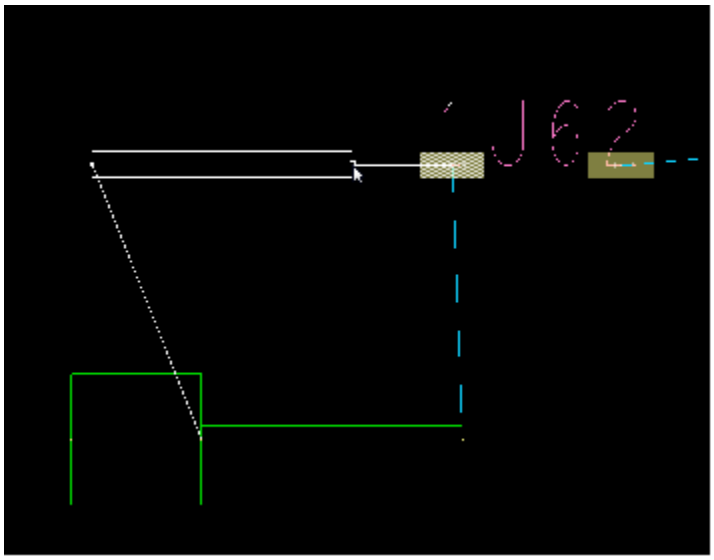


In 16.6, you are able to snap a component from outside of the outline to inside of the outline or snap a component from the inside of the outline to the outside of the outline.

The use model for the snapping pad edge is a little different from the original snapping functionality, once the *Snap to pad edge* option is checked, the direction for *Fix source component* or *Fix destination component* will be disabled. The source component will be attached to your mouse and you need to move your mouse close to the destination component pad edge.

RF to non-RF

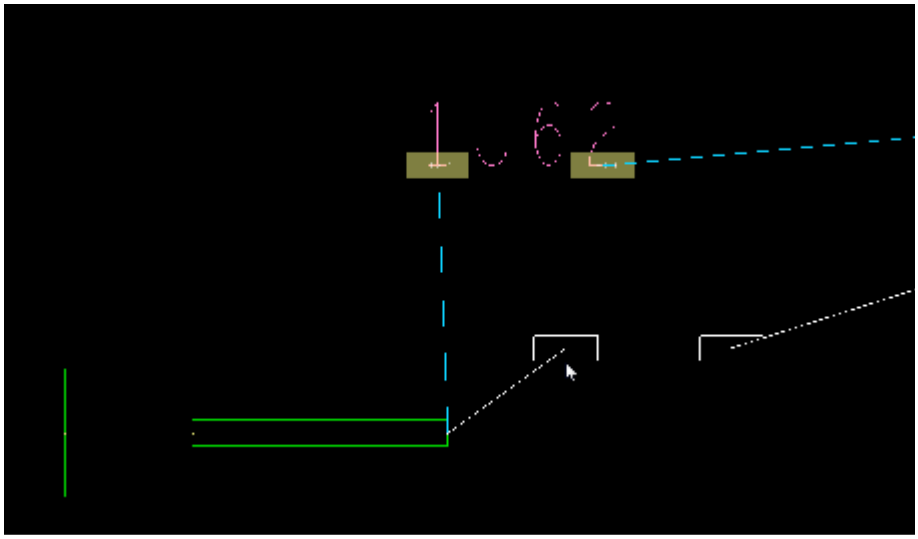
Click the RF component pin firstly and the RF component will be attached to your mouse, move your mouse close to the non-RF component pad, the RF component will be snapped to the edge of non-RF component pin. You can change the edge by moving your mouse close to a different edge of the pad, the dynamic path will show for you and you can click to place the RF component and the RF component will be connected with the non-RF component at the edge of the non-RF component pad. During the moving process, you can see the ratsnests for the connectivity.



Non-RF to RF/non-RF

Select an edge of the non-RF component pad and the non-RF component will be attached to your mouse, move your mouse close to the RF component pin (refer to the ratsnest) and the

non-RF component will be moved and snapped to the RF component, click to place the non-RF component.



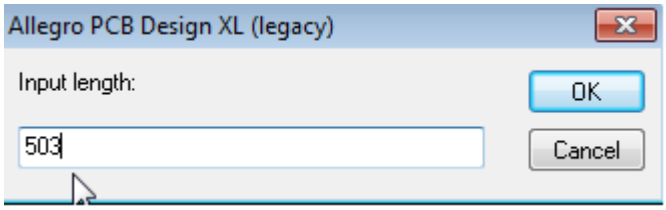
Add Connect Enhancements

The *Add Connect* command is enhanced to support snapping to pad edge functionality. When you check the *Snap to pad edge* option (available when the *Snap to connect point* option is checked), you can start routing from any edge of a pad by moving your mouse close the edge of the pad and clicking it to start.

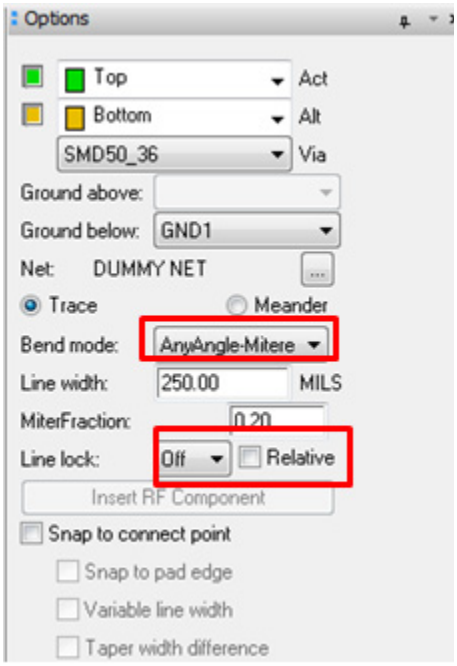
The *Variable line width* option will be available if the *Snap to connect point* option is checked. If you check the *Variable line width* option, the width of the RF trace will be variable based on the entry and the size of the pad and you can't change the trace width during the

routing. If you unchecked this option, the width of the trace will use the value that you entered on the Options tab and you can change the width during the routing process.

There is one more menu item *Accurate length* on the RMB menu during the routing. If you select it, the following form will pop up and you can enter a specific value for the length that you want to route.



You can route RF trace with any angle mitered bend by setting as following:

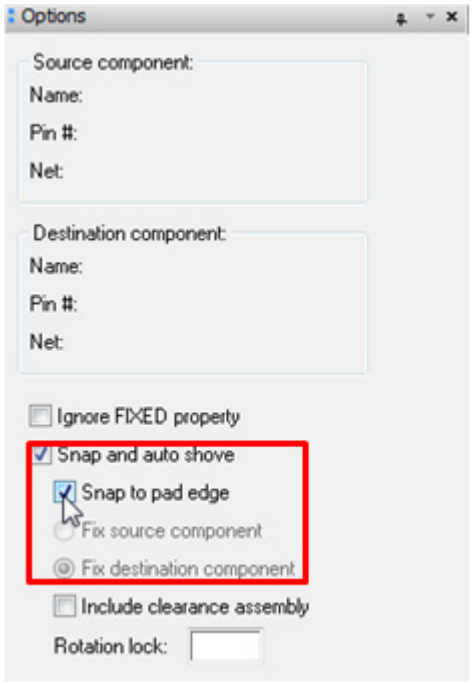


This can only provide the capability to start routing with any angle miter bend but may not complete the any angle routing between two specific points. If you want to do that, you may need to use the new command *Any Angle Bend Connect*.

Modify Connectivity Enhancements

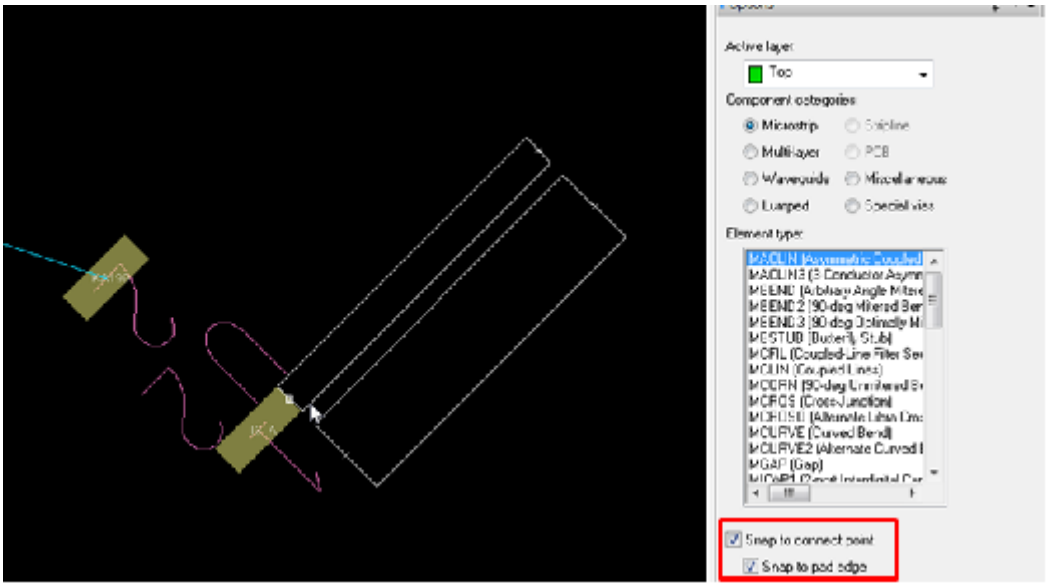
This command is enhanced by adding *Snap to pad edge* option. If this option is checked, the following *Fix source component* and *Fix destination component* options will be disabled.

The first selected component (by selecting the pin or pad edge) will be attached to your mouse and you can move your mouse to close the destination pin/pad edge.



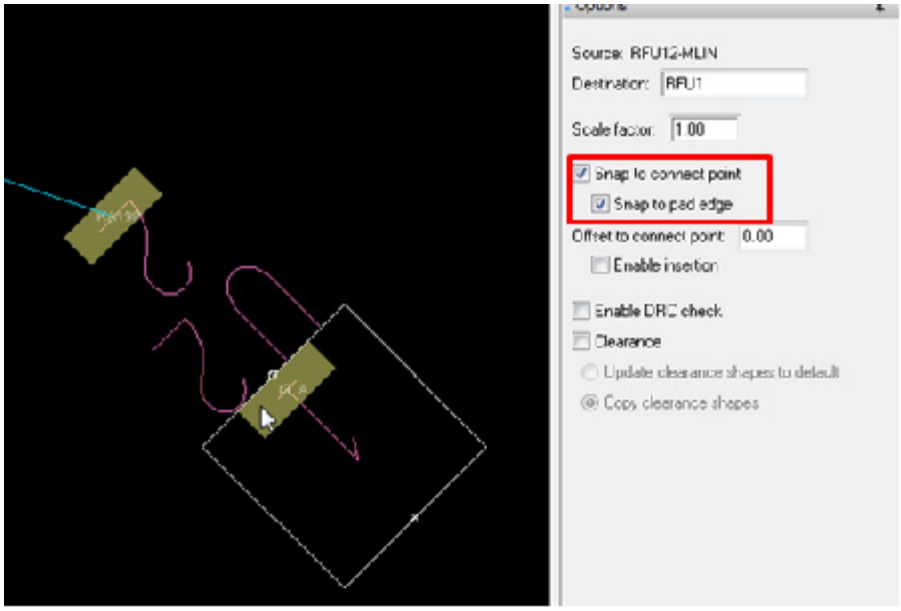
Add Component Enhancements

The *Add Componen*t is enhanced with the new option of *Snap to pad edge*. If this option is checked, the component to be placed can be located at a specific edge of a pad during the placement.



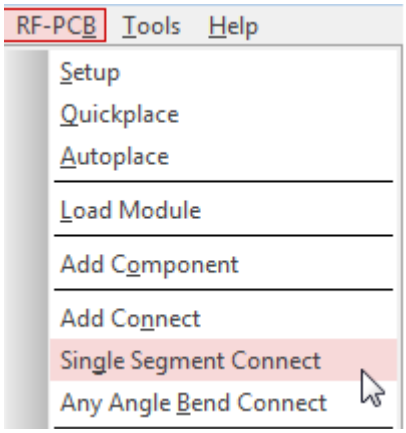
Scaled Copy Enhancements

This command is enhanced by increasing the option *Snap to pad edge*. Once this option is checked, the scaled copied RF component can be connected to any edge of a pad.



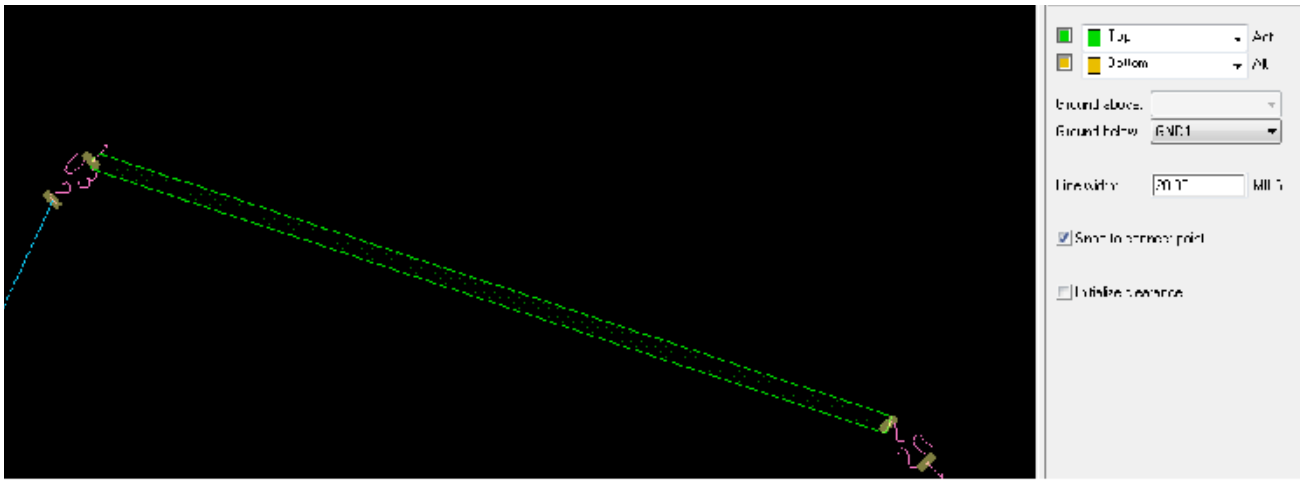
Single Segment Connection

In some cases, when you want to connect two points (pads) with a single segment (for example, microstrip line), you can use this new command from *RF-PCB - Single Segment Connect*.



To connect two pads, you can check *Snap to connect point* and then click the two pads. You may be asked to confirm to remove the ratsnest by changing the netname for a pin.

Using this command, you need to understand the routing may not be fully connected since the rotation of the pads.

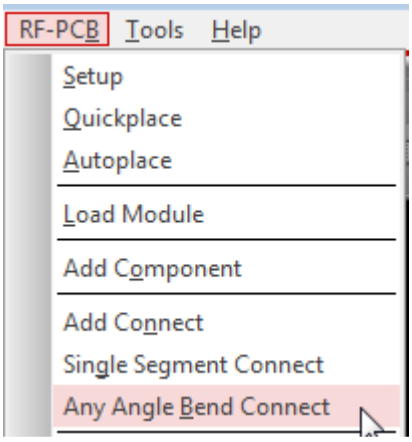


You can use this command for the connection between two non-RF components or two RF components or one RF component and one non-RF component.

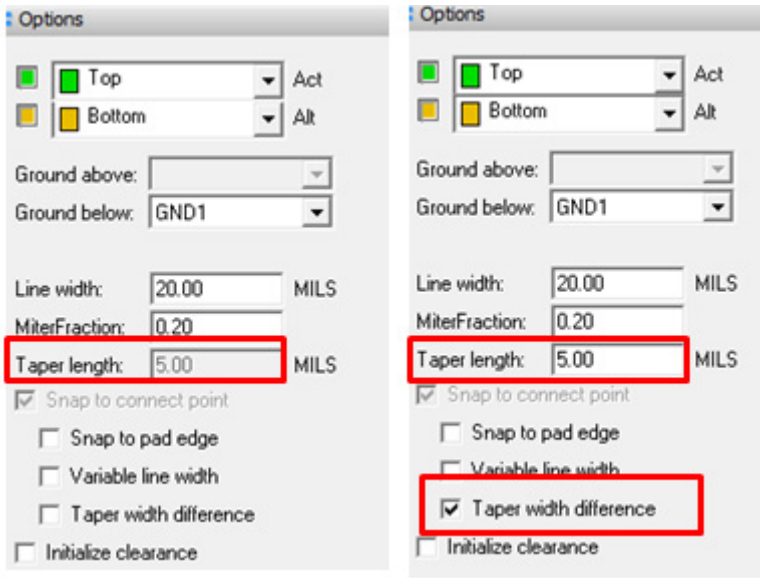
Route with Any Angle Bend

A new command is introduced to connect two pins/pads with any angle mitered bend. For example, three RF components (two line segments and one any angle mitered bend) to connect two specific pins/pads. The line segment may be Microstrip Line (MLIN) or Stripline (SLIN) and the any angle bend may be MBEND or SBEND2.

Choose *RF-PCB - Any Angle Bend Connect* to launch this command.



The parameters are shown on the *Options* tab as below:



You can enter the values for line width and miter fraction of the bend. For this command, the *Snap to connect point* option will be checked automatically and you can't change it. Under this option, there are three options you can control.

- Snap to pad edge: this option is used for the entry/exit of the routing at two pads.
- Variable line width: this option is used for the control of the width of the trace.
- Taper width difference: this option is used for the control of the last segment.

If *Snap to pad edge* option is checked, you can specify the edges for the connection between two pads. If it's unchecked, the connect point of the pins (usually is center of the pad) will be used for the connection.

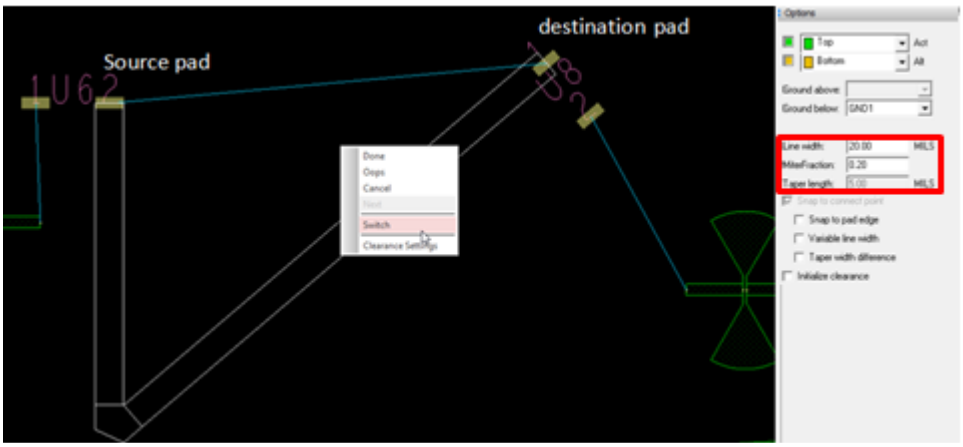
If the *Variable line width* option is checked, the connection will auto extract the width of the pads (if the entry width and exit width are different, then the exit/source width will be used). The width will be adjusted automatically based on the exit direction of the trace at source pin. The Line width on the form will not be used. If this option is unchecked, then the line width entered on the form will be used.

If the *Taper width difference* option is checked, the Taper length field will be enabled and you can enter a value for the taper length. If the destination pad (entry width) has a different value from the source pad (exit width), then the last segment will be a MTAPER with the specific length on the form.So in this case, there may be four elements (two MLINs, one any angle mitered MBEND and a MTAPER). This works only for Top/Bottom layer, for inner layers, this option will be disabled and you can't check it. If the taper length is too long, then you may not get the proper path for the connection.

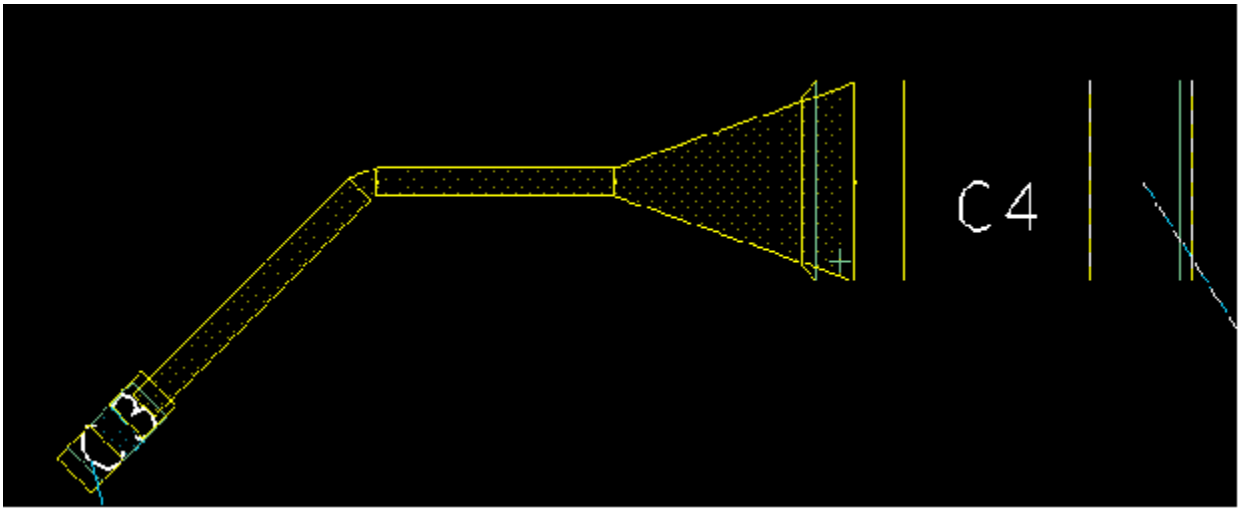
The use model for this command is as below:

- If the *Taper width difference* option is not checked, the routing includes three elements only.

Select the source pin/pad edge and then select the destination pin/pad edge, the shorted path will show for you by default and you can directly click to confirm or you can RMB select Switch to see other possible paths, select the expected path to click to complete the connection.



- If the *Taper width difference* option is checked, the routing may have four elements.



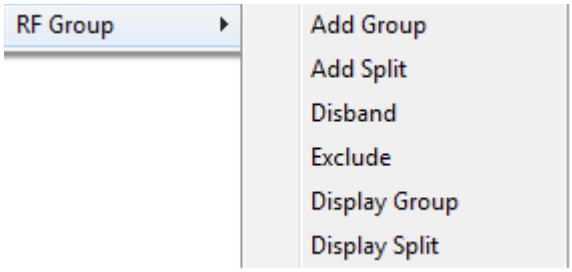
If you want to add clearances for the routed RF components, you can check the "Initialize clearance" option.

Autoplace Enhancements

- RF Grouping in Front End
- Enhancements in Back End

Autoplace is a very important step for RF layout creation after the schematic transferred to layout. The system will automatically create groups based on connectivity during the autoplace process. This will result in many groups in autoplace and it's difficult to find the proper groups to do autoplace. Users would like to define groups in schematic side based on functions such as LNA, pre-amplifier and so on and then select the proper groups to start autoplace.

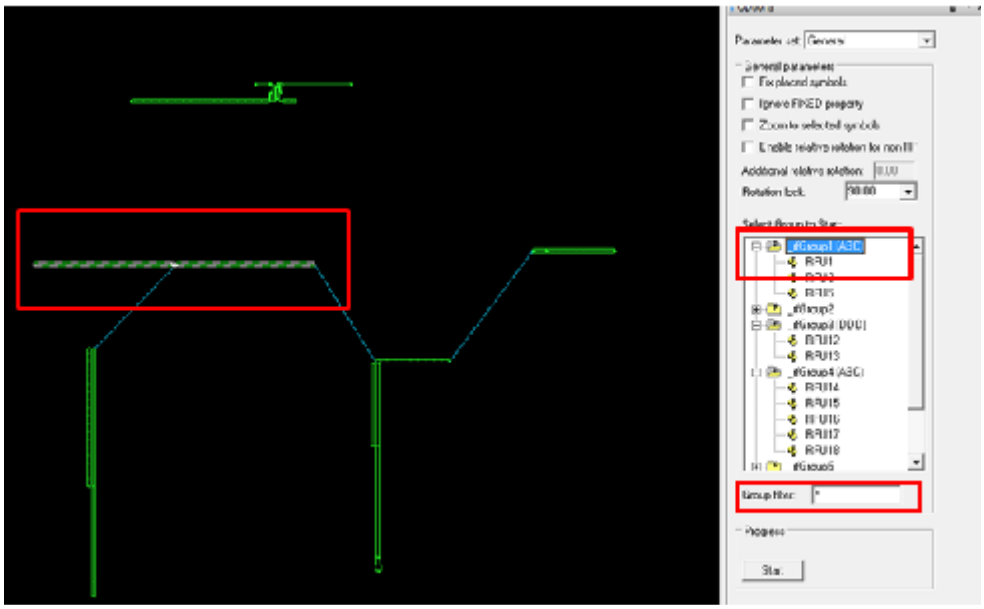
In 16.6, some new commands are added in Allegro Design Entry HDL to support grouping such as add group, disband group, display group to control the groups for autoplace. The detailed commands are as following:



All those commands are only available in the pre-selection mode.

- Add Group: Attach a property (RFGROUP) to the selected components.
- Add Split: Attach a property (RFSPLIT) to the wires selected. If a wire is attached with this property, then the logic group will be broken at here (one big logic group will be split into two logic groups).
- Disband: Remove the RFGROUP property from each RF component for the specific group.
- Exclude: Remove the property for selected objects (RFGROUP for RF components or RFSPLIT for wires).
- Display Group: Highlight/report the RF components within a specific group.
- Display Split: Highlight all wires with the RFSPLIT property.

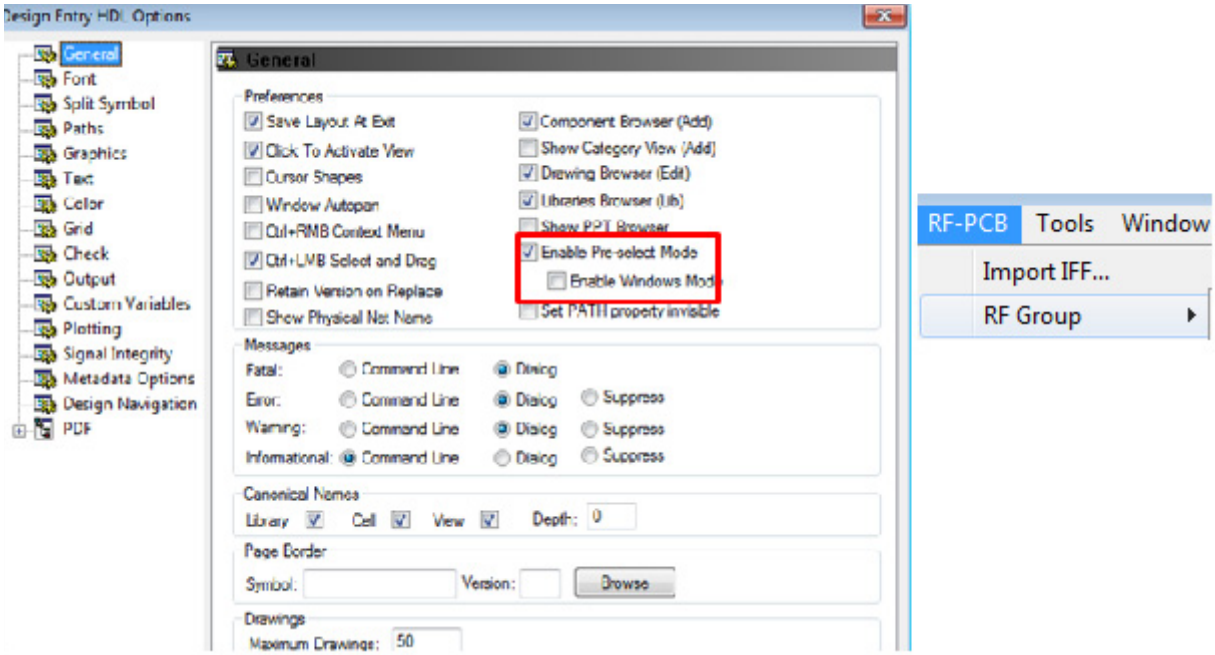
If you transfer the schematic to layout and launch Autoplace, you will see the groups are classified differently, the group names added in schematic are reflected in the autoplace.



You can use the *Group filter* to easily find/locate some specific groups to do autoplace.

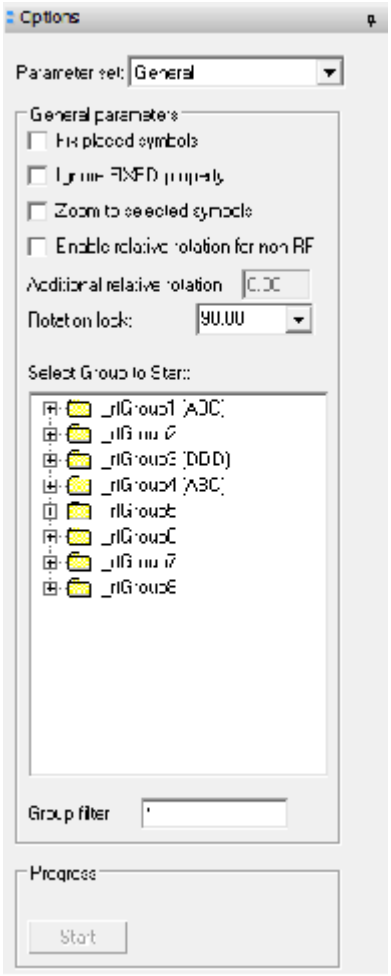
RF Grouping in Front End

To use the grouping functionality in schematic, choose *Tools - Options* and check the *Enable Pre-select Mode*. The RF PCB menus are shown in the figure below.



Enhancements in Back End

In PCB Editor choose *RF-PCB - Autoplace.*

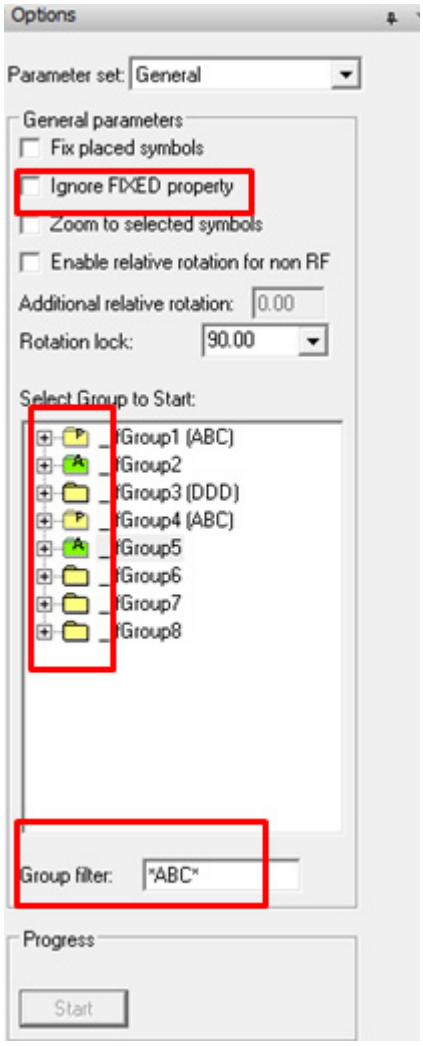


All components will be classified into different logic groups. Each logic group will have a name with the prefix _rfGroup. If you have already defined a group in schematic (for example ABC), then this name will be the name for a real physical group in layout. This name will be attached following the logic name within brackets such as _rfGroup1(ABC).

Some other enhancements for the autoplace are as below:

- Add a new check box *Ignore FIXED property*.
- A new mark A for the groups just completed autoplace.
- A filter to find/locate a group.
- Ratsnests display during the autoplace.

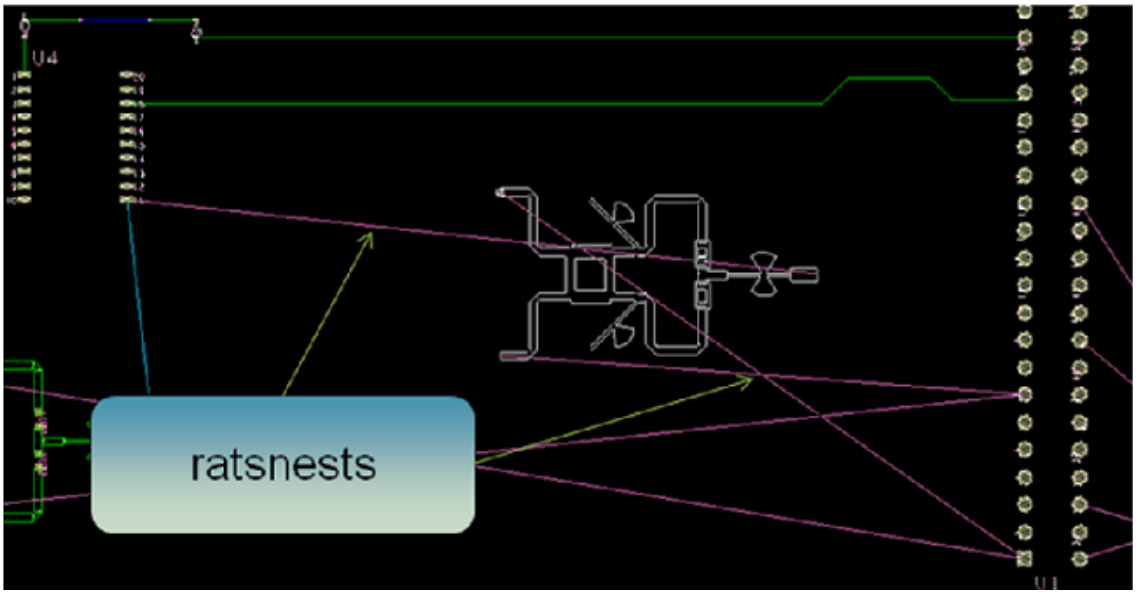
- Moving clearances as well
- Performance enhancements



If you check the *Ignore FIXED property* option, then a fixed component can be moved as well during the autoplace.

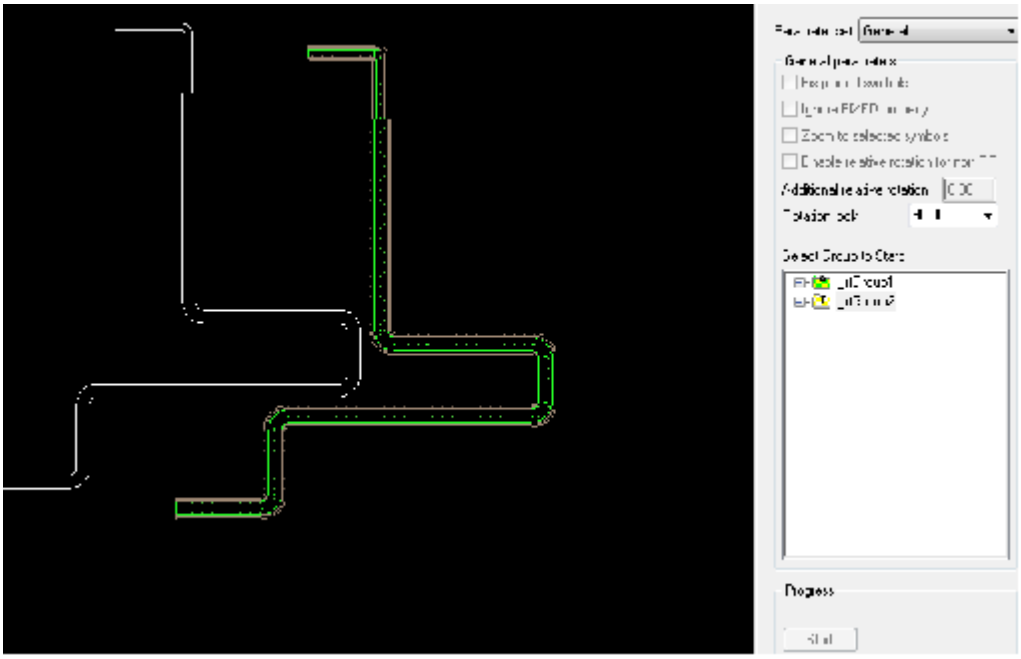
There are two kinds of marks for the groups. A group with P mark means this group is already placed into canvas before the autoplace command launched. A group with A mark (green color) means this group completed the autoplace in the current session. A group without any marks means this group is still unplaced and you may need to do autoplace for it.

The autoplace is enhanced to show the ratsnests while the dynamic path is attached to your mouse during the autoplace process. This is easy for you to place the group to the proper location.



Another enhancement is to support the clearance moving as well for the autoplace. For example, after completing the autoplace for a logical group and then adding the clearances for the components within the group. If you redo the autoplace and move to a different location

to place the group, the clearances will be moved as well. Before that, the clearances will not go with the RF components.



Via Exchange Between Allegro PCB Editor and ADS

- Export Allegro Generic Via Padstacks to ADS
- Export Allegro Design with Generic Vias to ADS by IFF
- Import IFF with Via Components into Allegro

Layer-to-layer via structures are almost always used in PCB designs. These common structures are not standardized in ADS, they are represented in several ways. These include instances of via models such as the microstrip VIA2, and as layout-only footprints that define the catch pads and drill holes with simple polygons.

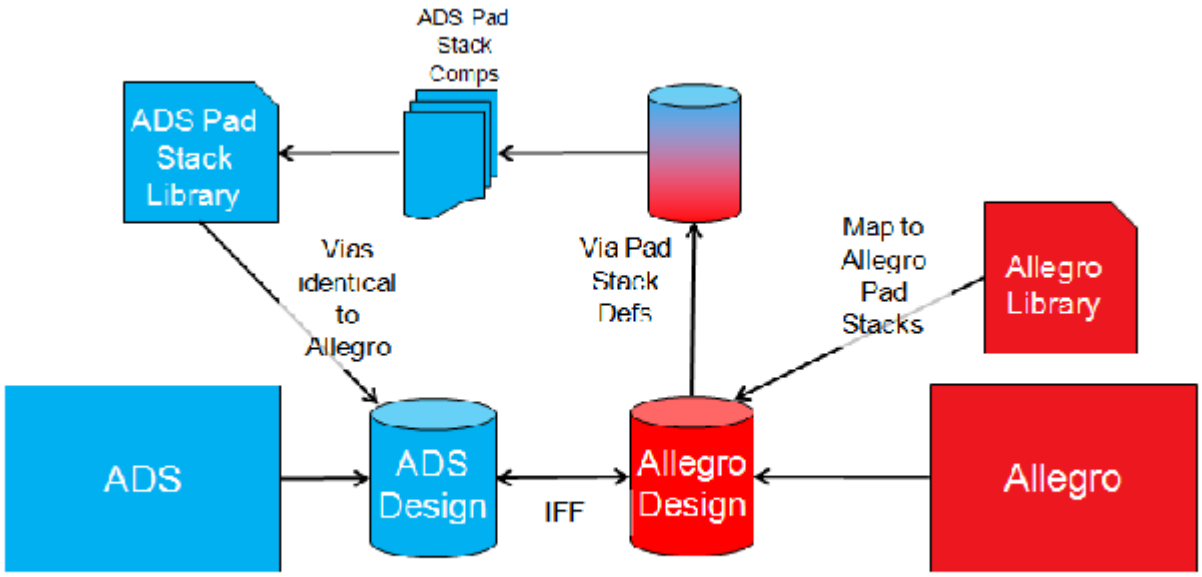
The disconnecting between the capabilities of PCB tool via structures and the equivalent object in ADS makes design transfer difficult. A PCB-tool via structure must be flattened to simple polygons for transfer to ADS, losing most of the information contained in the original PCB via. Likewise, those simple polygons can be transferred back to the PCB tool, but are not identified as a via structure and not treated as a layer-to-layer connection.ADS does not have the PCB compatible via library, that means no padstack definition for generic PCB via. To solve the problem, Cadence and Agilent worked out a solution: you can export Allegro generic via padstacks firstly from PCB Editor and then ADS will build PCB-style via library with pcbViaLib Utility offered in ADS2011.10. Agilent has provided the pcbViaLib design kit,

which provides via import utilities and a new ADS component, the pcbVia. This design kit defines a data file format that holds the definition of a PCB-tool style via structure, which is read by the pcbVia component and used with a layout macro to render exactly the same layout footprint in ADS as in the PCB tool.

When you export an Allegro layout design with generic vias to ADS by IFF, you can select export vias as components so all generic vias will be mapped to ADS via components.

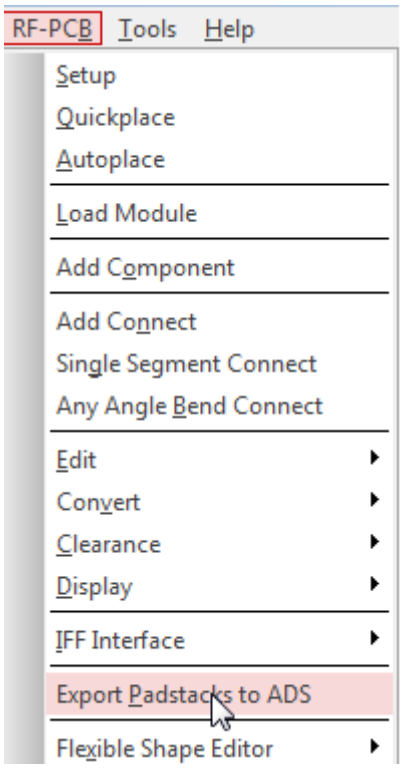
You can also use the via components in ADS layout and then export the ADS design with the kind of via components by IFF. When importing the design into PCB Editor by IFF, the I/F will automatically map back the ADS via components to Allegro generic via padstacks.

The flow for via management between Allegro an ADS is as following:



Export Allegro Generic Via Padstacks to ADS

To run the command choose *RF-PCB - Export Padstacks to ADS* for ADS via component creation.

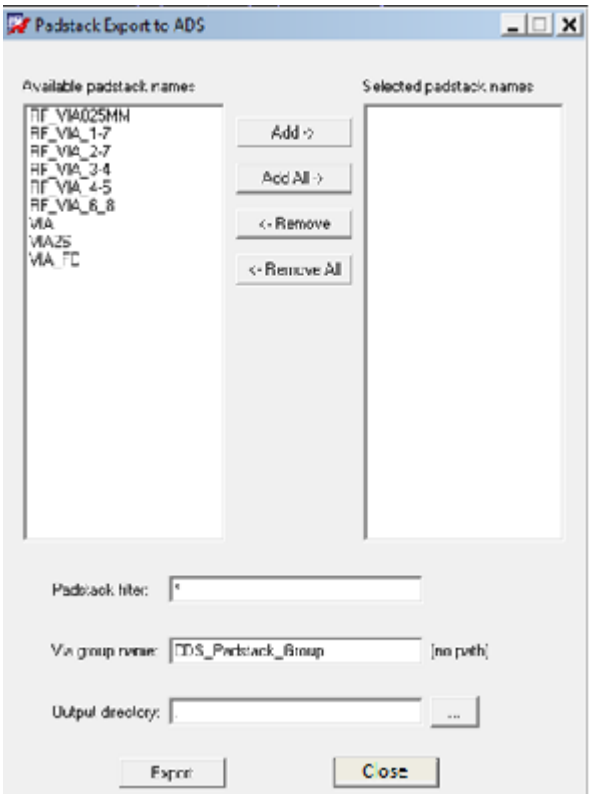


All vias used in the design will be listed and then you can select some/all vias to export. Please notice only vias in the layout will be listed on the form, so if you want to export a via padstack, you have to place the via into a design.

The Via group name is for ADS usage. Once you create the via components in ADS side, you can place a via component in ADS layout from the specific via group.

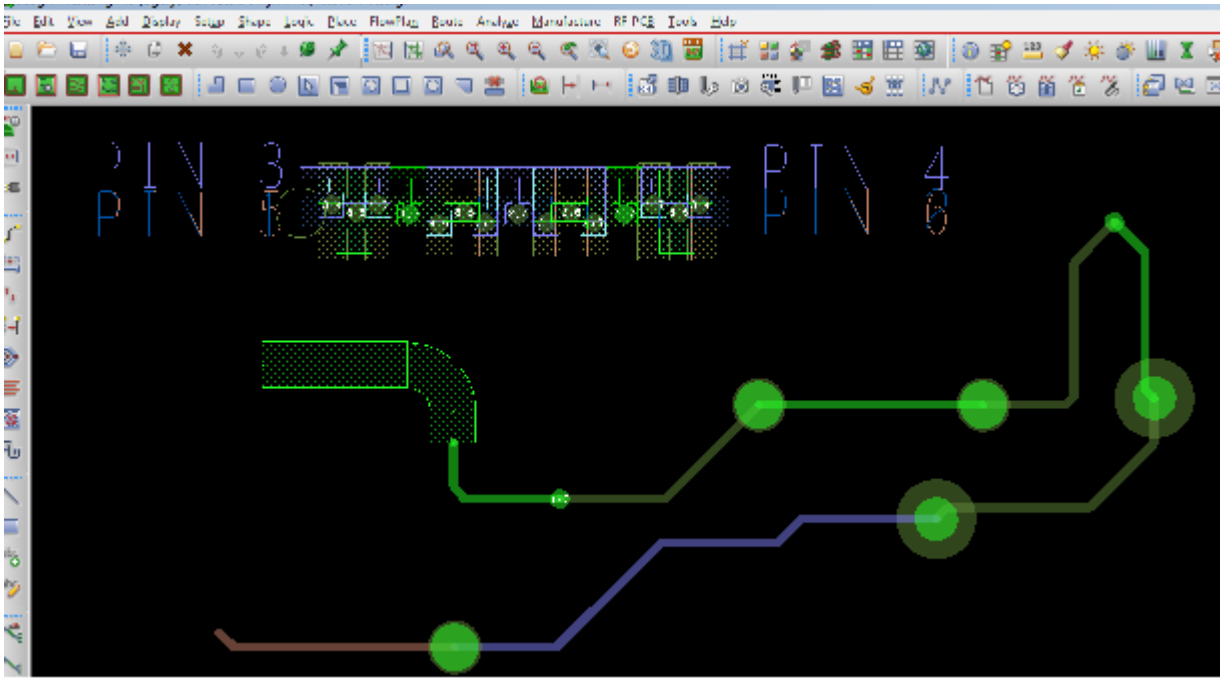
Note: It is recommended to use a unique group name for each design so that ADS will not confuse.

The exporting for via padstacks is not based on IFF format but AEL.

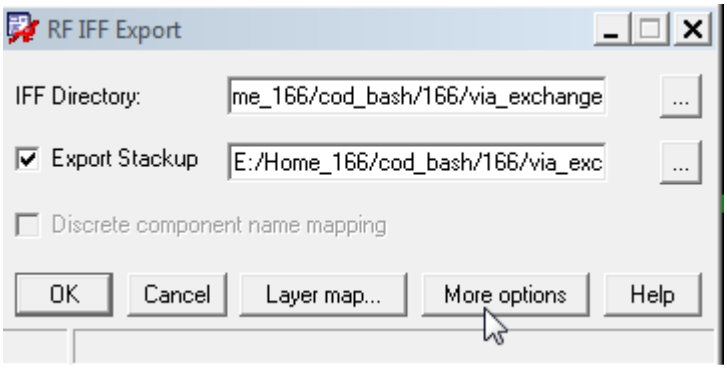


Export Allegro Design with Generic Vias to ADS by IFF

In a design with generic vias in PCB Editor choose *RF-PCB - IFF Interface - Export*.

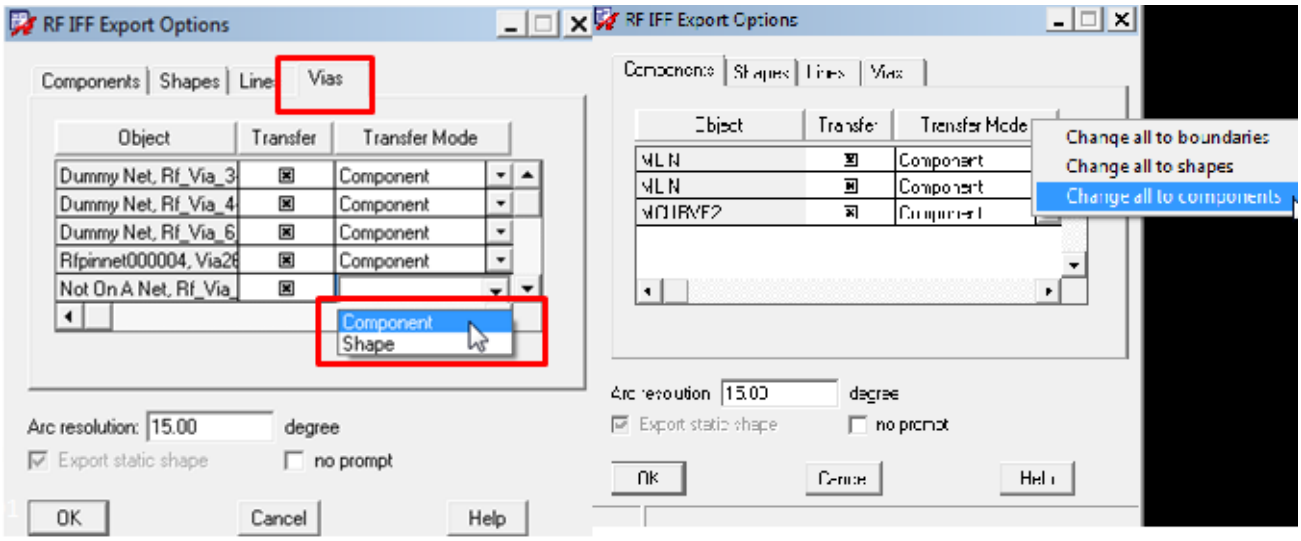


The IFF export dialog box appears.



You can click *More options*, to see the *Vias* tab. Two options available for via transfer mode. By default, all vias will be considered as components to export. You can change it to Shape

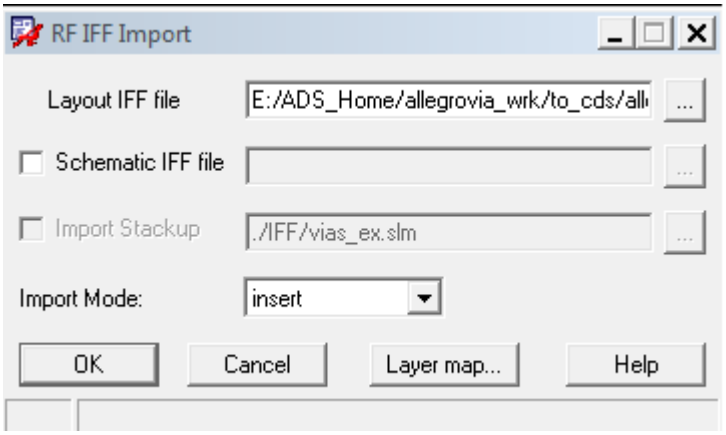
for the exporting as before. You can also RMB click on the header bar to select Change all to components as below:



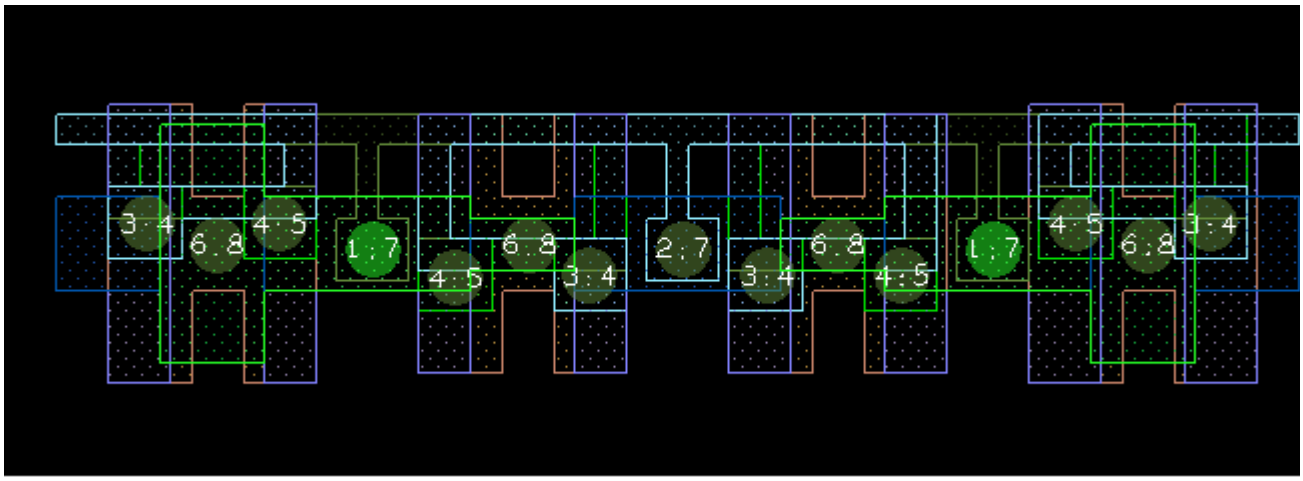
If you export all vias as components, then all selected generic vias will be written out as via components in IFF file so that ADS can recognize them.

Import IFF with Via Components into Allegro

In PCB Editor, choose *RF-PCB - IFF Interface - Import*, browse to the proper `layout.iff` file.



All via components in the IFF file will be mapped back to Allegro generic vias.



Miscellaneous Enhancements

Some other small enhancements made to RF PCB 16.6 includes:

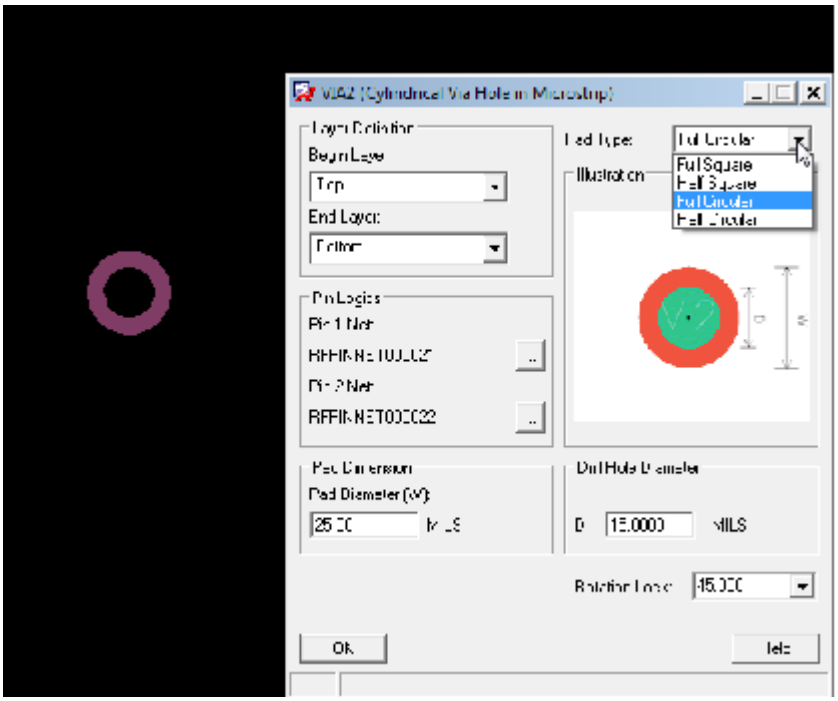
- New Libraries
- Setup Enhancements
- DRC Removal for Netlist Re-import
- Discrete Library Translator Enhancements

New Libraries

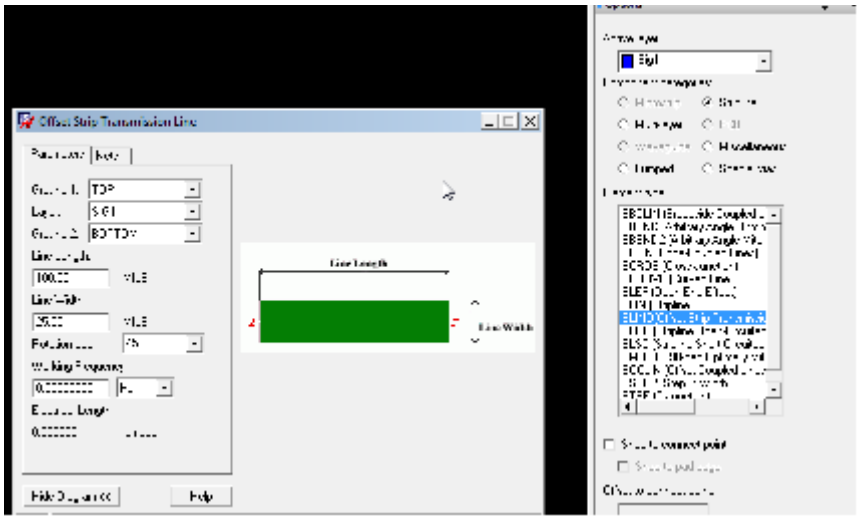
Two new RF components which existed in ADS are now added to library:

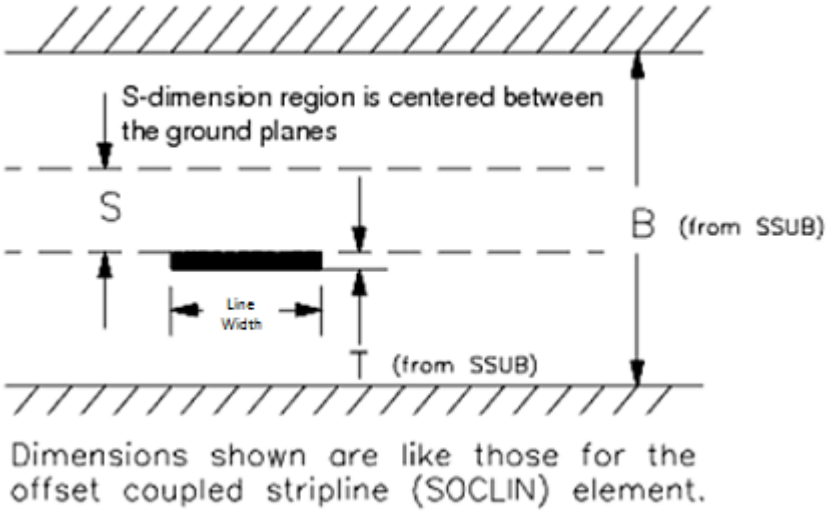
- VIA2
- SLINO

VIA2 is a special via component in ADS similar to Allegro via padstack (but it's not a padstack structure).



SLINO is a stripline component that has special substrate structure:





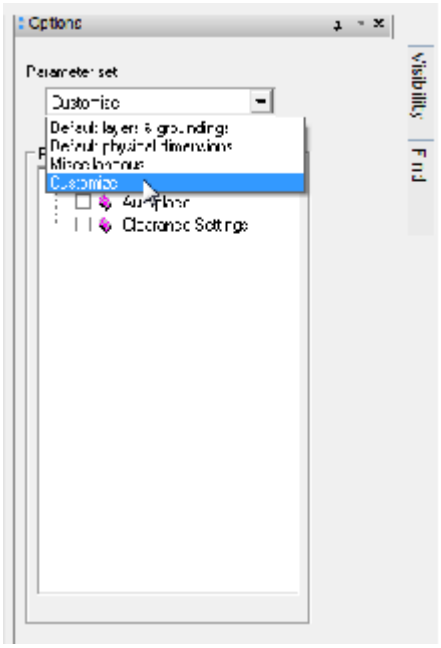
Dimensions shown are like those for the offset coupled stripline (SOCLIN) element.

Setup Enhancements

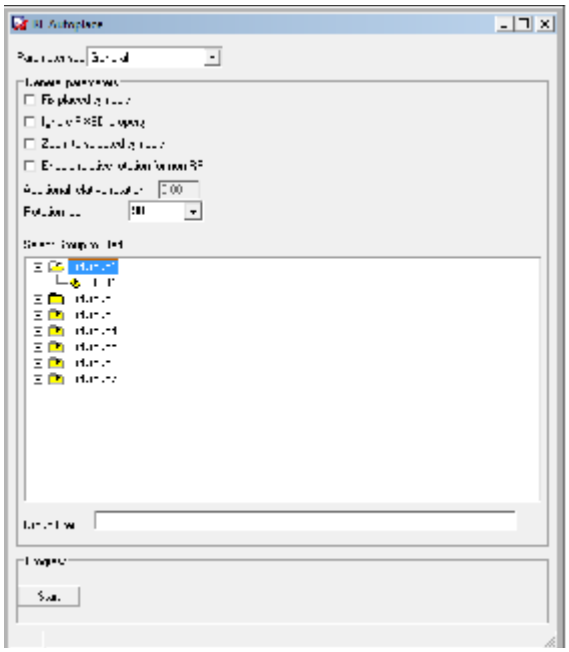
A new option *Customize* is added to the drop-down list for *Parameter* set in *Options* tab of *RF-PCB - Setup*. This is used to determine the GUI to be floating or fixed in the Options tab. There are three items currently:

- All
- Autoplace
- Clearance settings

If you check All, then all RF PCB GUI will be floating instead of fixed in Options tab.



If you check *Autoplace* option in above form and then you launch Autoplace command, you will see the GUI for Autoplace will be floating as following:

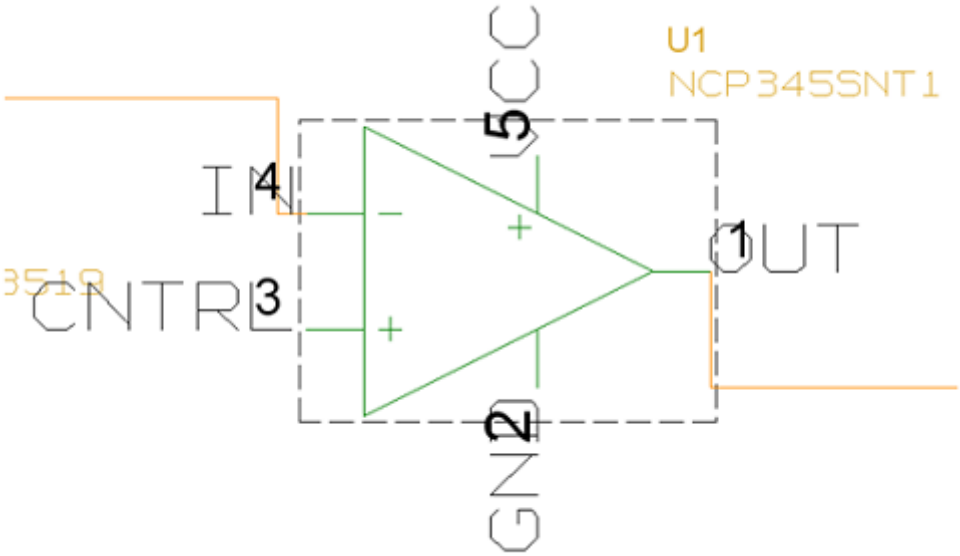


DRC Removal for Netlist Re-import

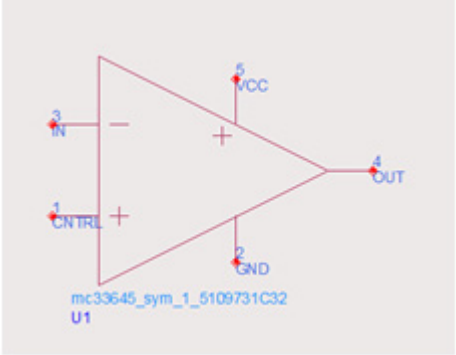
In the past, after you transfer a schematic to layout and complete the RF placement by Autoplace, if you re-import the original netlist without any changes into PCB Editor, you will see a lot of DRC (shape2shape or shape2pin) and you have to do autoplace again to remove those DRCs. This is because the shape nets for RF components are missed during the netlist importing so all RF shapes have a dummy net. This is enhanced to remove the DRCs for the re-importing netlist without any changes.

Discrete Library Translator Enhancements

When translating Allegro discrete library to ADS, some pin numbers may not be correct in ADS schematic. For example, when we export the following component to ADS:



The result in ADS may be as below:



Allegro PCB Editor: What's New in Release 16.5

Product Version 16.6
October 2012

This document describes new features in the current and previous releases of Allegro PCB Editor. Significant enhancements have been made in the following areas:

- Embedded Component Design
- Graphical User Interface
- Etch Edit Enhancements
- Intelligent PDF Output
- Associative Dimensioning
- Design for Manufacturing
- DRC Updates
- ECAD-MCAD Flow
- Database and Misc Enhancements
- RF PCB Enhancements

To view the latest updates on hardware and software requirements, see the *Allegro Platform System Requirements*. Also refer to the *Migration Guide for Allegro Platform Products, Product Version 16.5*.

Embedded Component Design

With increased market demands for smaller and lighter products, improved performance and higher speeds, it may become necessary to consider the embedding of passive or even active components within the inner substrates of the PCB. If you are designing product that essentially can be held in your hand, perhaps ones used in mobile applications or a consumer electronic device like a digital camera, embedded component technology may be in your product roadmap plans. The methods on how components are mounted and logically connected to the formation of cavities may differ from vendor to vendor. The Allegro Marketing and R&D teams have done its best to provide a robust solution that can accommodate the vast options you may encounter in the industry. As always, our best advice for advanced PCB Design whether that be HDI, Flex or Embedded is to work closely with your Fabricator who may also own the Allegro tools. They can advise on the proper parameter and constraint settings that best accommodate their process flow.

To support embedded components, following enhancements have been done in Allegro PCB Editor.

- Licensing
- Front to Back Flow Support
- Setup
- Key Terminology
- Design Rule Checks
- Best Practice Paper

Licensing

Embedded Component Design is available in both the PCB Editor and Package/SiP tools. Under the new licensing scheme for 16.5, the "Miniaturization" product option is selected.

Front to Back Flow Support

The overall functionality associated with Embedded Component Design is largely contained in the back end physical products. However, the primary method that enables a component to be an embedded candidate is driven from a component definition or instance level property called EMBEDDED_PLACEMENT. This property can be applied at the schematic level with values of `Required` or `Optional`, thus enforcing the front-to-back flow restrictions you may want to impose on your design process. Alternatively, it can be applied with the physical back-end editors.

Setup

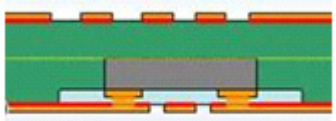
To setup your board file for supporting embedded components, choose *Setup – Embedded Layer Setup*

The embedded layer setup form controls the layer(s) to be used for embedded placement, Component direction of Body Up or Body Down, attachment methods of Direct or Indirect and associated global parameters.

Key Terminology

Direct Attach

The manufacturing technology where the components are soldered directly to an internal layer. One way to visualize this is to think of assembling a traditional PCB with the components on the external surface(s) and then laminating more layers on top of the components.

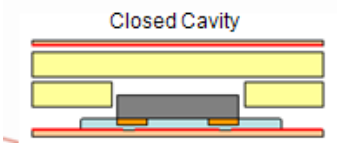


Indirect Attach

The manufacturing technology where the components are suspended in the dielectric material between the layers. Components are glued, not soldered. The electrical connections are made by drilling control dept microvias through the foil and epoxy to the component pins.

Closed Cavity

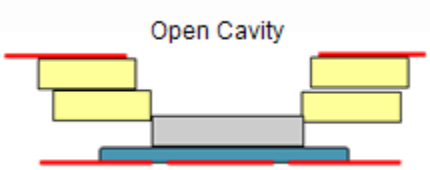
The space around the embedded component in the dielectric between two etch layers. The XY dimensions of the cavity are driven by the size of the component and other manufacturing rules. In most applications, the cavity will be between two adjacent layers; however, multilayer cavities will be supported.



Open Cavity

A blind hole in the substrate in which components are placed. This hole is open to one of the external substrate surfaces and may be several layers deep. The cavity will often have

progressively smaller lengths and widths from the external surface to the depth of the cavity.



Note: The terms above are Cadence generated. The Fabricator may use different terminology to describe their methodology.

Design Rule Checks

Two new constraints have been added, one to check for package to cavity clearance and second to verify the package height within the cavity.

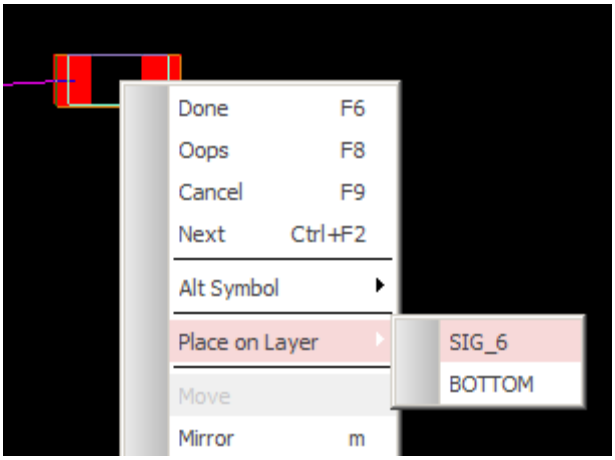
To enable these constraints, choose *Setup – Constraints –Modes – Design Modes (Package)*, and select the two options listed below Embedded DRCs.

Note: DFA - Component clearance is based on top side values from the DFA table.

Component Placement

- Use *Move/Place Manual* and right-click to access the *Place on Layer* command. Only legal layers to embed components appear in the form.

- Use Quickplace to quickly place embedded components on their targeted embedded layer. The *Quickplace* form is enhanced to recognize the Embedded_Placement property and Internal embedded layers.



Best Practice Paper

For further details on using embedded components, refer to product documentation and the *Embedded Component Design best practices* paper.

Graphical User Interface

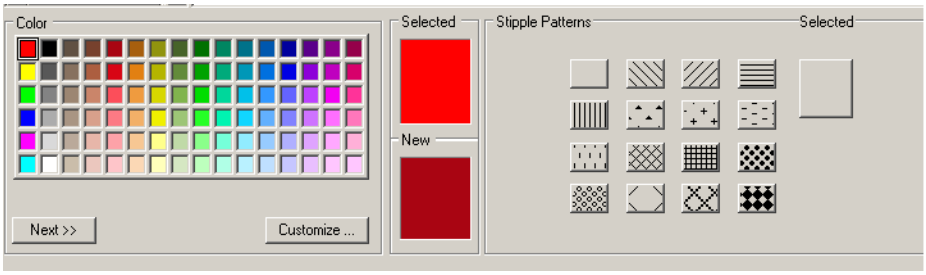
This section lists the enhancements made to the Allegro PCB Editor user interface.

- Highlighting With Stipple Patterns
- Dynamic and Static Shape Display
- Highlighting Fixed Objects
- Status Bar Updates
- 3-D Viewer Update
- Data Tip Setup
- Data Tip Display

Highlighting With Stipple Patterns

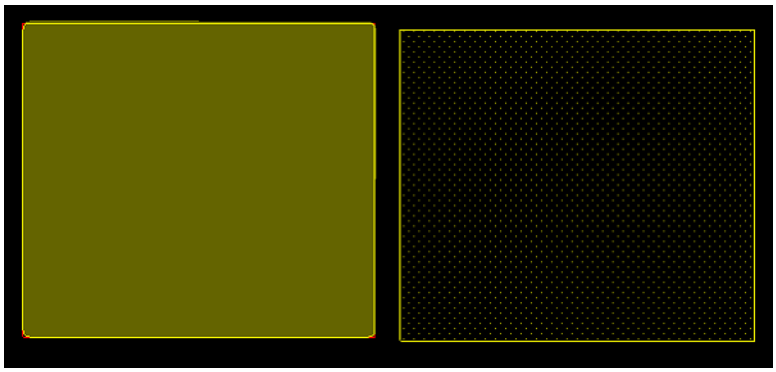
Stipple Patterns support is provided through `assign color` and `highlight` commands as well as through the *Color* dialog. The `assign color` command allows you to assign custom stipple patterns to objects in addition to assigning color and default highlight patterns it currently supports.D

- The `assign color` command, as its name implies, allows you to assign a custom color to a database element with the option of overlaying stipple patterns.
- The `highlight` command allows the assignment of stipple pattern to elements such as nets; no color assignment is done. This is the main difference between the `highlight assign color` commands. The *Find filter* options for both commands are the same.
- The *Color* dialog has been enhanced to allow stipple pattern assignment to layers. Assigning a pattern to a color cell is applied to all corresponding objects on that layer.



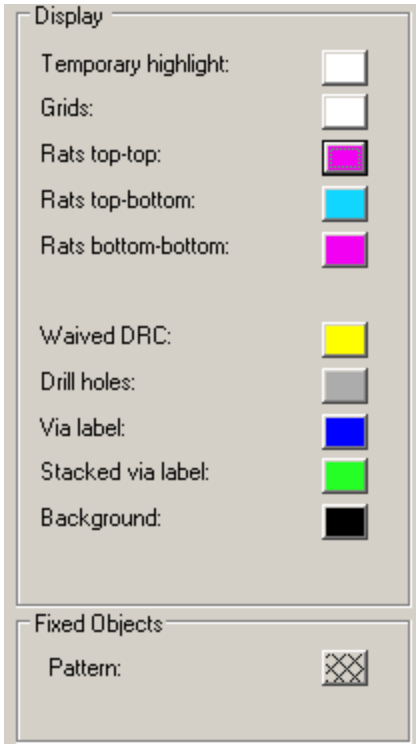
Dynamic and Static Shape Display

The former graphics behavior for dynamic and static shapes has been restored.



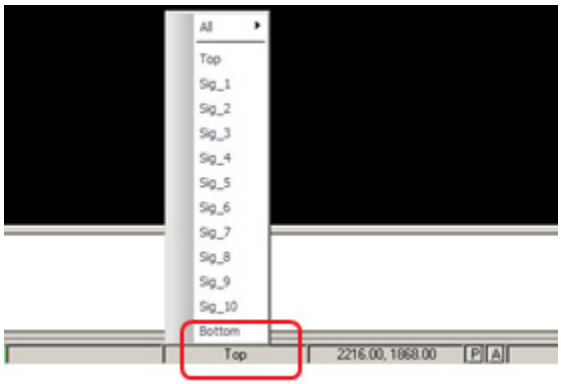
Highlighting Fixed Objects

Discerning fixed objects in the database can often be a trial and error exercise for a designer. One might attempt to slide a cline segment only to find out it has been fixed. A new graphical enhancement helps identify fixed elements with stipple pattern overlays. Assign any one of the available 15 stipple patterns to the new *Fixed Object* entry located in the *Display* tab of the *Color* dialog box.



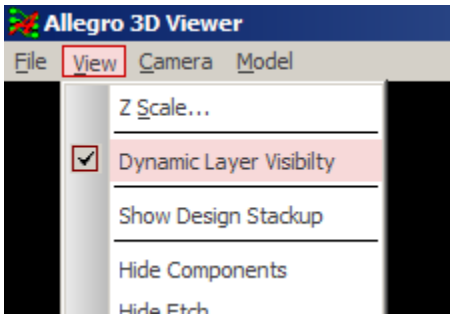
Status Bar Updates

Functional responses can be obtained by clicking fields in the status bar. For example, the field indicating the current subclass can be selected and changed to a new class/subclass. This is a good alternative to opening the *Options* tab over in the side panel.



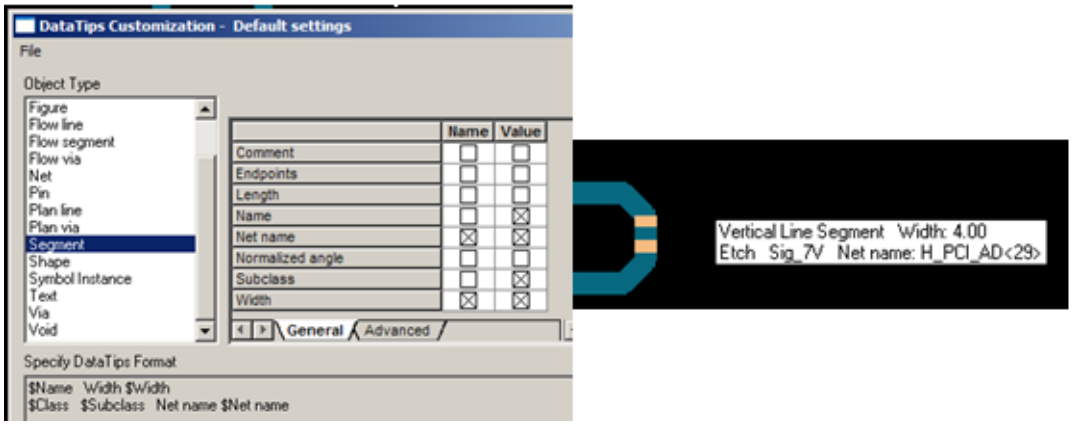
3-D Viewer Update

The 3D viewer now updates layer visibility changes dynamically. This mode is enabled by default.



Data Tip Setup

The *Object Type* field has expanded from 6 entries to 17 entries providing greater customization of on-screen display information. For example, hover over cline segments to obtain etch width as shown is the figure below.



Data Tip Display

Data Tips can now be enabled or disabled from the *Setup* Menu or tool bar icon  .

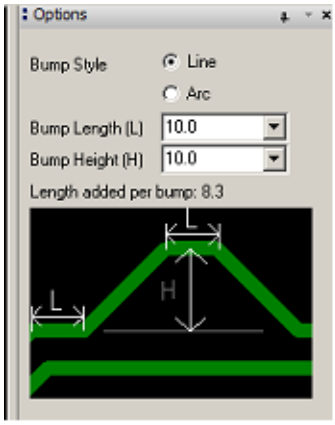
Etch Edit Enhancements

- Differential Phase Tuning
- Trace Tapering
- Group Route Via Patterns
- Diff Pair Routing - Transitions at Region Boundary
- Pad Exit Behavior
- HDI Via Labels
- HDI Via-Via Line Fattening
- Delete Via Structures
- Copy/Move Stacked Vias

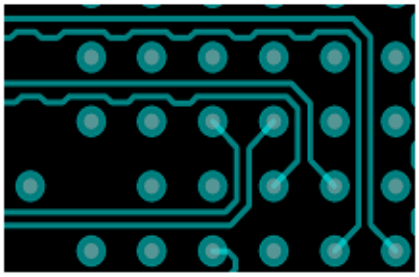
Differential Phase Tuning

Phase Tuning is an alternative to using the mouse guided delay tune command and offers the precision of finite length adjustment to differential signals that are length/phase constrained. It is especially effective on static or dynamic phase-constrained differential pairs where iterative etch compensation may be required at various points along the path of either member of the pair. Simply make a mouse click at any point on the cline path to add in a single-parameterized phase bump.

The command is located in the *Route* menu of the PCB Editor. When invoked, parameters can be set in the *Options* tab. Select a style of *Line* or *Arc* then define its respective length/size parameters. The form computes the added compensation for each bump before applying it.



Phase Tune Options



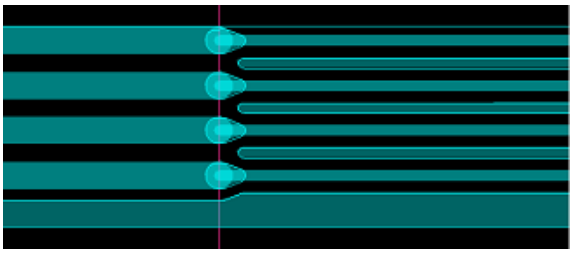
Differential Phase Bumps

Trace Tapering

Trace tapering is the gradual reduction of line width on a PCB. The purpose of tapering is to prevent abrupt changes in line width. Common in RF and Rigid Flex applications, tapering is used to reduce stress at the location of the line width transition.

Trace tapering feature is a function of the shape-based fillet algorithm. The fillet parameter form has been expanded to include a section specifically for trace tapering. Other minor changes include a section for *Global* options at the beginning of the form. As with pin/via based fillets, enabling the *Dynamic* option automatically adds the taper object during

interactive routing. If the *Dynamic* option is disabled, tapering can be done using the `add taper trace` command located in the *Route – Gloss* menu.



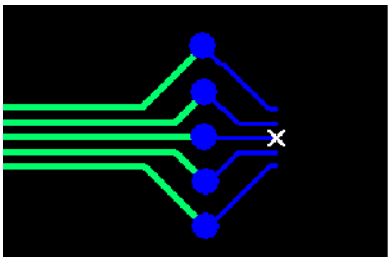
Cline transition at rigid-flex boundary

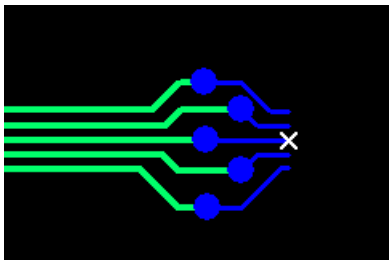
Group Route Via Patterns

Via Pattern support is available when in the `add connect` command. Group routing is initiated in one of the following ways:

- Invoke `add connect` command and then select a group of vias or cline segments to commence the group route.
- Invoke `add connect` command then right-click to select *Multiline Route* to route a user-defined number of dummy nets.

There are six available via patterns. These same patterns are available in the PCB Router (Specctra) interactive routing environment. With the `add connect` command enabled, right-click and select *Via Pattern* from the menu, and from the drop-down list select the required via pattern.





Diff Pair Routing - Transitions at Region Boundary

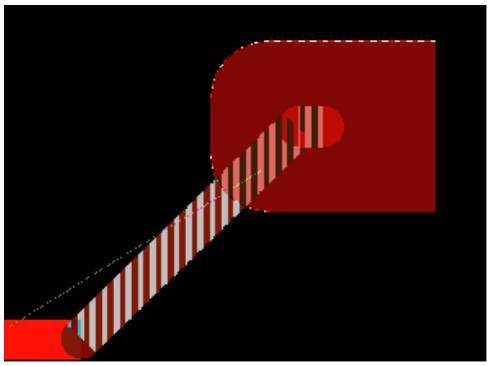
Quality improvements have been made to both `add connect` and `slide` commands in the area of Constraint Region transitions. They include:

- Symmetrical gathering of Differential Pairs at the boundary when crossed orthogonally or at 45 degrees.

- Maintain Differential Pair line width and gap during slide or when being shoved.
- Remove the *hinge* effect at boundary - free sliding of Differential Pair.

Pad Exit Behavior

When the Enhanced Pad Entry feature was introduced in SPB 16.3 release, it did not support pads drawn as shapes. For the 16.5 release, the feature has been enhanced to support shape based pads.

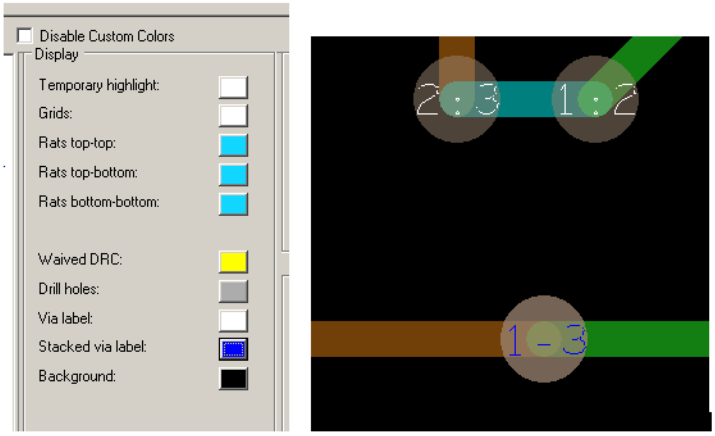


The Enhanced Pad Entry option is available on the right-click menu for both `add connect` and `slide` commands.

HDI Via Labels

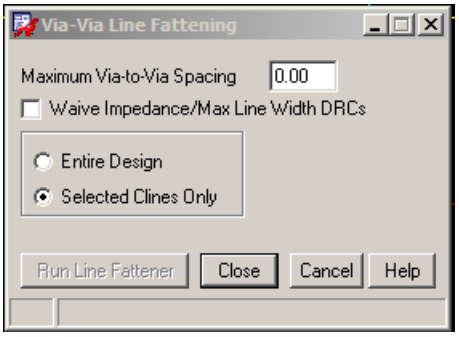
Color support is now available for Via labels. These graphical labels are used to provide visual feedback for the respective begin:end layers of a single or stacked series of microvias.

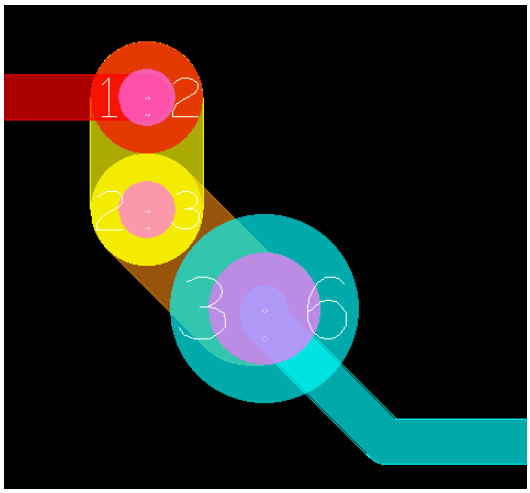
You can access the color controls in the *Color Dialog – Display* folder.



HDI Via-Via Line Fattening

In previous releases, if you wanted to increase the line width between two adjacent HDI vias, the application had to be run on the complete design. In this release, the feature has been enhanced to provide a new control option, using which, you can run the application on selected clines only.

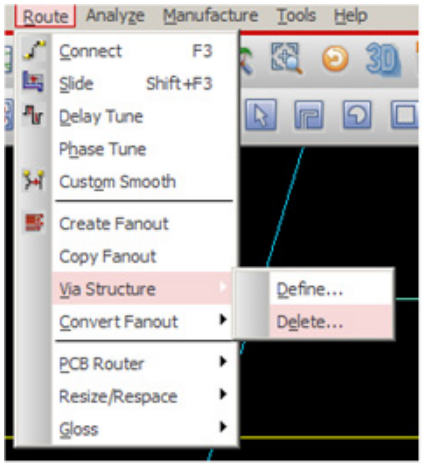




Delete Via Structures

Via structures are typically used in the breakout of devices requiring stacked or staggered microvias. The via structure library can be accessed from the *Create Fanout* application.

Starting this release, you can use the *Via Structure – Delete* command to delete unnecessary via structures from the design database.



Copy/Move Stacked Vias

The Copy and Move commands now handle stacked vias as a single entity.

Intelligent PDF Output

All versions of the PCB Editor are now connected into the PDF Publishing tool. This tool exports Allegro board data in a PDF document with intelligent data for components, nets, and test points. You can specify the graphical Class/subclass layers that can be viewed and the properties that are to be extracted in the PDF. The graphical data generation is defined through the artwork layer control files and the current color assigned to that layer in the design. Page size, gray scale, scaling, and other options are available to the user.

Allegro to PDF may also be run as a batch routine. To run PDF Publisher:

- Choose *File – Export – PDF.*
- Run the `pdf out` command.

Note: Artwork film records are required to be in place before extraction.

Licensing

You are required to have the Allegro PDF Publisher license as is used by Allegro Design Entry HDL, and at minimum a PDF reader. Cadence recommends Adobe 9.0 or higher.

Note: Cross Probing is not supported between Front- and Back-End PDF files.

Associative Dimensioning

The Allegro dimensioning capabilities have been enhanced so that when a dimension is created involving one or more design database objects, internally, the dimension remains associated with these objects. Subsequent editing operations, such as the moving of an object, can then appropriately and automatically update any dimensions that are associated with that object.

To access this functionality:

- Choose *Manufacturing – Dimension Environment*
- Run the *Dimension Edit* command
- Use the toolbar icon 

Note: Once in the Dimension Edit Environment, use the right-click menu to access all commands and parameter setup associated with dimensioning.

- When a database is up-revved a previous SPB release to 16.5 release, dimensions do not become associative. Dimension added in the previous releases remain

non-associative and essential static in place. They cannot be moved or edited but the PCB Designer may elect to delete and re-add the dimensions to leverage the new associative behavior.

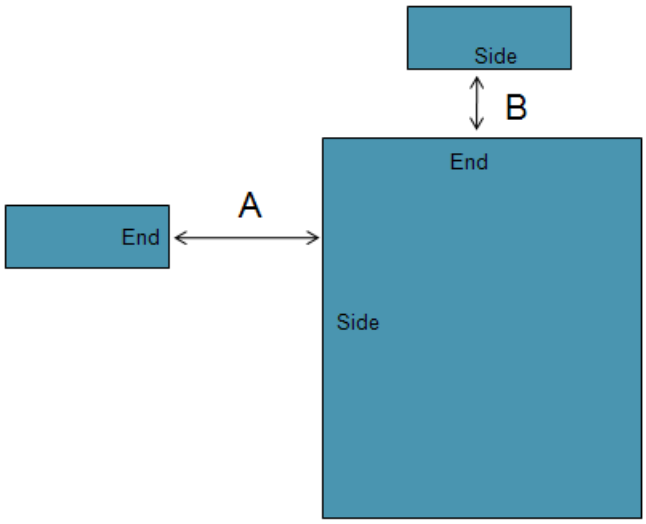
- When a 16.5 database is down-revved, the dimensions remain but the association is removed.
- The `delete dimensions` command associated with the dimension edit environment is used to delete associative dimensioning.
- Deleting an object, causes deletion of associated dimensions.
- To move dimension leader lines and text, use the `move text` or `edit leaders` commands associated with the dimension edit environment.
- After moving a component in the y-direction, the dimension text does not maintain its former y position. To maintain the former y location, use the `Lock dimensions` command. This command locks the text in place prior to moving the component.
- The `z-move` command is used to move dimension text to other subclasses, but there are some limitations. The available Class-Subclasses are:
  - Board Geometry
    - Dimension
    - Assembly Notes
    - Any user defined subclass
  - Drawing Format
    - Any user defined subclass
  - Manufacturing
    - Any user defined subclass
- In the parameter forms, Color blue represents:
    - Parameter form — changes apply to future dimensions that are added. They do not apply to existing dimensions.
    - Instance Parameter form — changes apply only to the dimension you select in the canvas.

Design for Manufacturing

- DFA Enhancements (Side-End and End-Side support)
- DFA Usability
- Minimum Metal to Metal Clearance DRC
- Duplicate Drill DRC
- Cross Section Chart
- Backdrill Enhancement (Any Layer to Any Layer)
- DRC Updates

DFA Enhancements (Side-End and End-Side support)

The DFA spreadsheet now supports a fourth DRC entry to accommodate requests for separate values for Side to End and End to Side. In the example below, A and B both represent a Side to End condition where different values need to be applied.



- The symbol considered the Reference Symbol is located in the column of the DFA spreadsheet.
- If *End to Side* value is not present, the DRC uses the *Side to End* value for both conditions, as was done in releases prior to 16.5 release.
- When comparing two identical symbols, only the Side to End value is used. End to Side is considered superfluous.

- When you down-rev the database to 16.3, the Side to End value is ignored by the DRC system.

DFA Usability

Interactively, behavior associated with moving a component to meet the minimum DFA clearance rule has been enhanced. This new behavior requires the DFA_PAUSE_LEVEL user preference value to be set to 3. When set, the active component will pause during movement in the attempt to meet the DFA rule.

Minimum Metal to Metal Clearance DRC

This is a new design-level check that has been added to ensure that minimum metal to metal clearance is met. This check has been added to flag spacing errors that occur when certain spacing modes are accidentally set to OFF, and for CAD<>CAM alignment.

It is best to run this check, near design completion. Otherwise, in most cases, it will produce redundant DRCs — assuming your entire spacing suite of modes is set to ON. Single clearance value entry is supported in the *Design Options* page. This checked is intended to work as a net to net check; same net behavior is not supported.

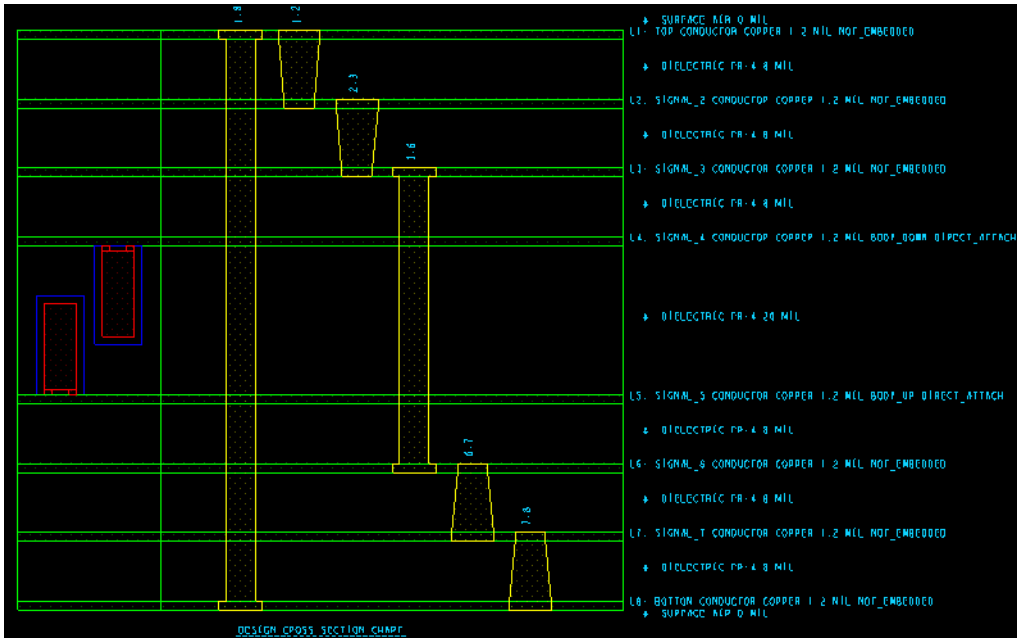
Duplicate Drill DRC

This is also a new design-level check that detects duplicate drill holes spanning the same layers. Duplicate drill holes may be based on the same or different pad stack definitions. Simple overlaps (non-identical drill locations) are excluded from this definition. Drill holes that share all the same layers are considered to be duplicate.

Cross Section Chart

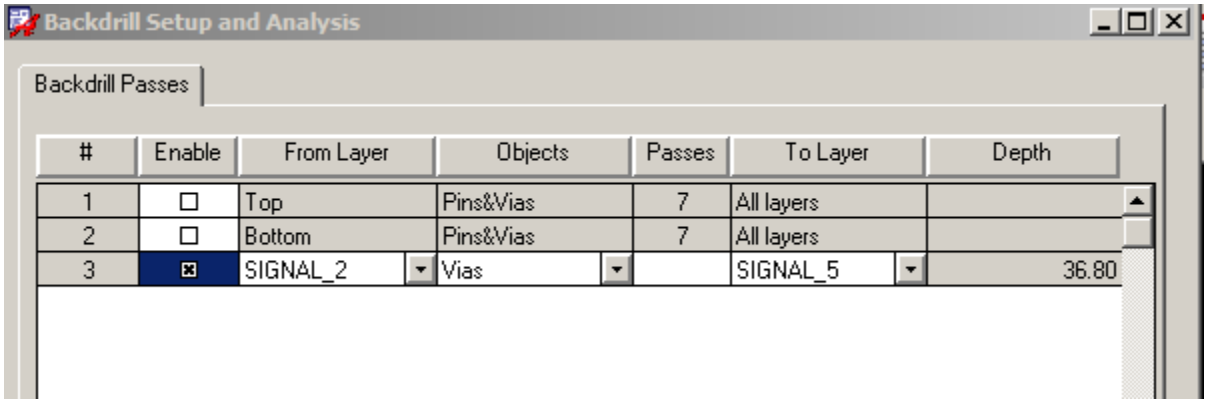
A detailed view of the cross section can now be generated. To access the command, either choose *Manufacture – Cross Section Chart*, or run the *xsection_chart* command.

Similar to the NC Legend, the chart is registered as a *group* object and will retain its current position upon recursive outputs.



Backdrill Enhancement (Any Layer to Any Layer)

Backdrilling capability in Allegro PCB Editor is enhanced to allow any layer to any layer configurations. Prior to SPB 16.5 release, backdrilling was restricted as it could start either from the top layer or from the bottom layer. This is a critical enhancements for composite construction techniques used with some HDI and sub-laminate designs.



DRC Updates

Max Neck Length DRC

Starting this release, the behavior of the Max Neck Length DRC is changed. Now the DRC flags an error if the cumulative length of necked sections exceeds the prescribed Max Neck Length value.

Prior to SPB 16.5 release, in a routed design, the Max Neck Length constraint was applied on a per-segment basis for CLINEs. Thus each segment was measured independently within a necked section and compared to the constraint value. As long as each individual segment was less than the maximum length, no violation was reported. However, in case of CLINE necks that span more than a single segment, there were situations when each individual segment was shorter than the length constraint; while the total length of the necked section exceeded the constrained length without report of violation. To address this scenario, the behavior of the Max Neck Length DRC is changed to constrain the cumulative length of necked sections to not exceed the prescribed Max Neck Length value.

ECAD-MCAD Flow

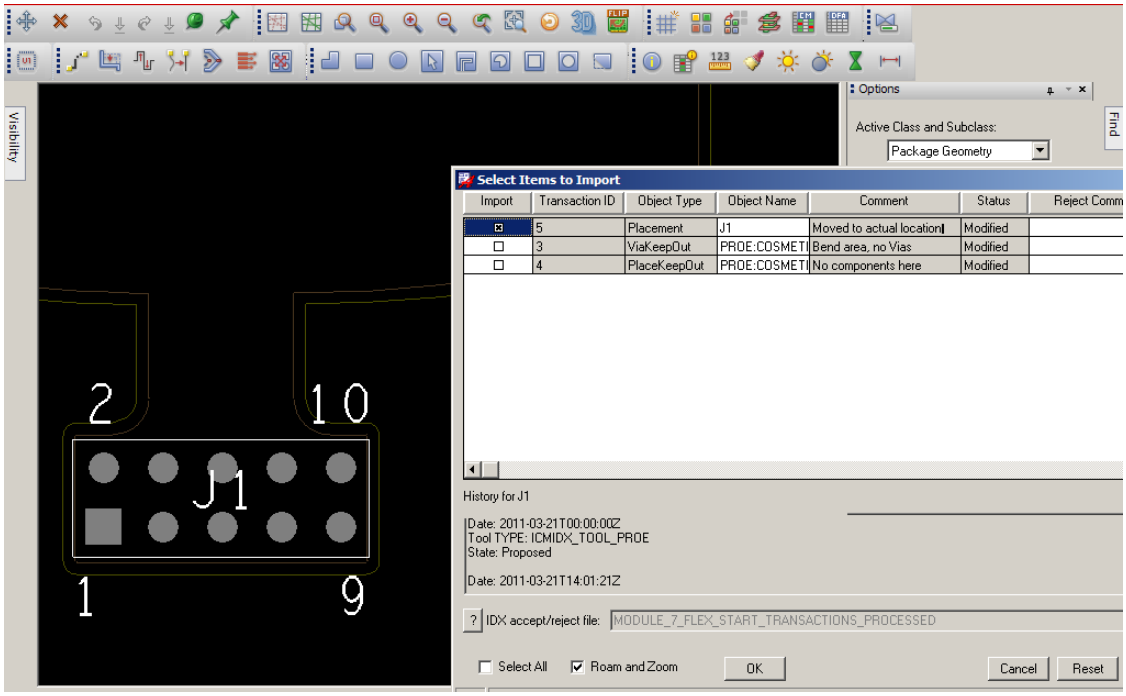
INCREMENTAL DATA EXCHANGE (IDX)

The exchange of electrical and mechanical CAD data has had many import/export formats based on IDF and DXF. Each format has maintained a set of standards accepted by the CAD industry. These formats have served well over the years, with one common underlying issue, the exchange of data is considered, "all or nothing". If a board outline, constraint areas, and component placement is used initially, all the same data is continually exchanged bi-directionally, even if just one object is modified. This exchange format is difficult to manage design impact and change tracking.

The EDMD schema (or IDX format as it is more commonly referred to), a new XML based data exchange format, was created to aid in the exchange of ECAD/MCAD data by introducing the concept of passing incremental changes. This implies that both the ECAD and MCAD tools begin at the same starting point, or baseline, and any change from the baseline line is considered an incremental modification of the data. The incremental data, and not the entire CAD interface data set, is then passed from one CAD tool to the other.

Additional capabilities in the EDMD schema enhance the ability of design collaboration. Comments, and accept/reject capabilities provide options to improve communication between the two design disciplines.

For example, after the design baselined, the PCB Designer moves a component whose location was defined in the baseline. In the new schema, the design exports this change, and through a GUI, adds a comment describing the reason for the modification. The Mechanical Design would preview the incremental data, accept the change and import the data, or reject the change, and reply with a comment explaining the reason for the change rejection, along with a possible new location. The PCB Designer previews the new proposal, accepts, rejects, and so on.



The EDMD schema is managed by ProSTEP iViP ECAD/MCAD Collaboration Project Group. (http://www.prostep.org). Cadence Design Systems is a member of this project group and continues to review and recommend updates and modifications to this standard to address technology and design process requirements.

Notes:

- The data exchanged in the IDX 2.0 format is the same as in the IDF 3.0 format. With the exception of panelization data, the data exchanged is identical between the two standards.
- Use of IDX format is recommended as it raises data exchange to a more collaborative environment. Once a baseline is established, only incremental changes are exchanged, where users can see a specific change, review the impact to the design the change would make, and either accept or reject that change. Whereas, the IDF format passes the entire data without providing users with a way of viewing the changes (also known as all or nothing).

- You cannot use both IDX 2.0 and IDF 3.0 for the same design. The data created for IDX and IDF contain ownership, data id and flows specific to each interface. If a design is started as IDF and IDX is launched, the user will be prompted with a prompt regarding the removal of all IDF properties and associations and visa-versa.
- While using IDX format you cannot start with an incremental file. A baseline must be defined before an incremental file can be imported.
- Accidental deletion of IDX file is not a problem because the IDX file is embedded within the Allegro database. Any proposed incremental IDX changes that are imported or exported are compared to the current baseline in the database. This baseline is updated for each proposed change that is accepted.
- You cannot manipulate the IDX file. The IDX data standard is a mix of STEP and XML formatted data with references to multiple areas in the file. Editing one item without editing all other references will result in an unusable or corrupt file producing bad results.

Database and Misc Enhancements

- Database Locking
- Multi-threading Support
- DBDOCTOR
- Downrev to 16.3
- DBSTAT
- Same Net Constraint Set update
- Symbol Editor
- Refresh Symbol
- Modules and Locked Property
- Techfile
- Design Status
- Color
- Artwork
- Thieving
- Create Detail

- Display Measure
- Shape Copy
- User Defined Mask Layers — Mirror support
- Place Replicate — Support for Single Symbol
- Placement Files
- Design Partitioning
- Polygon Select
- Undo/Redo Buffer
- Capture Canvas Image
- Zoom Button in Pick Dialog
- New Variables
- New Properties
- Modified Properties
- Deleted Properties
- Reports
- IDF Out
- Symbol Export
- Data Migration
- Script Migration
- Skill Enhancements

Database Locking

In pre-16.5 releases, multiple users could edit and update the same design without conflict notification. To prevent this situation an advisory lock feature has been introduced. In 16.5 release, when you open a design for editing, PCB Editor creates a lock file, `<design>.lck`. This lock file is maintained until Allegro exits, opens another design or writes a new design file. If a different program attempts to open this design, a warning message is thrown and users can then override or cancel their design open request. A similar message is presented when you attempt to overwrite a locked design.

You can disable the locking support by setting the `allegro_nolocking` environment variable. When this variable is set, programs do not create lock files but check for the presence of lock files before opening a design.

Multi-threading Support

DRC update now takes advantage of up to 16 computing units.

DBDOCTOR

Purge unused constraint set option added to the dialog. A high cset count can contribute to database performance issues. Cadence advises running the performance advisor to check for issues that contribute to performance degradation.

Downrev to 16.3

- Downrev to SPB16.3 is supported from the *File – Export* menu. As always, carefully consider the impact of downrev before commitment.
- Log file now supports a list of deleted properties

Subclass Characters

Character limit is increased to 31.

DBSTAT

`Dbstat -t` now reports the product tier used to save the database.

Same Net Constraint Set update

The by-layer DRC mode is now enabled by default on new designs.

Symbol Editor

- Package symbols can now be created with no placebound shape.
- Symbol editor can now change a pin from mechanical to connect by adding pin text to the PIN_NUMBER layer.

Refresh Symbol

Enhanced to provide an option to Reset Pin escapes.

Modules and Locked Property

When in the MDD editor, a LOCKED property can be added at the drawing level. When the MDD is loaded into a design, the resulting module inherits the locked property.

Techfile

- The techfile batch program has new options to allow filtering output to match the capability present in the Constraint Manager dialog.
- The techfile batch program now supports reading and writing dcf files.

  For more information, see `techfile -help` and the `-i` option.

Design Status

The Status dialog now supports Net Short DRC Status.

Color

- The color view drop-down in the Visibility tab now alphabetically sorts the user's .col files.
- Color view save now offers an option to save the flip state of the design.

Artwork

- The artwork dialog will now issue a warning and offer to create film records when the current film set does not contain all of the cross section entries.
- The artwork dialog has been enhanced to support adding a blank film record. To do this, use the *Add Manual* command available in the right-click menu.
- The default for new designs is RS274X and 2.5 units. Metric designs default to metric output.

Thieving

New options panel checkbox to keep thieving vias within the route keepin area.

Create Detail

Now supports placing a detail on any allowed layer.

Display Measure

Display measure window now includes the net name where appropriate.

Shape Copy

Shape instance parameters are now retained when performing a copy of a dynamic shape. This enhancement is also supported when using Z-Copy and Copy to Layers.

User Defined Mask Layers — Mirror support

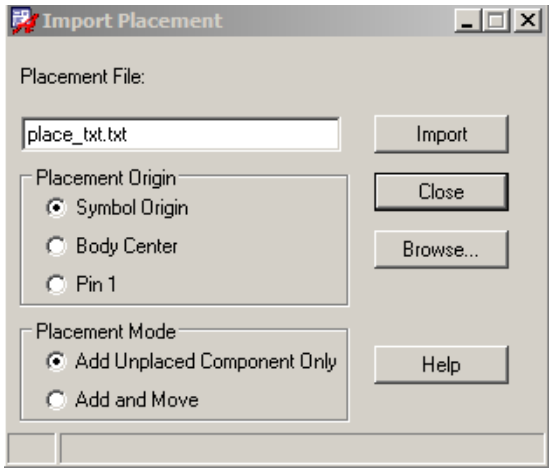
User defined mask layers now support the Allegro mirror _TOP/_BOTTOM standard. For example, a padstack used by a pin has a circle pad defined on a user mask layer GOLD_TOP. If the design also has a user mask layer GOLD_BOTTOM, when a mirror is performed on the symbol then the circle pad will appear on GOLD_BOTTOM.

Place Replicate — Support for Single Symbol

The two symbol restriction has been removed. This allows the user to replicate etch connected to a single symbol, such as a fanout pattern, and move these groups of elements as a single unit.

Placement Files

Placement import (plctxt) now offers an option to move placed components to the location, rotation and mirror values in the plctxt file. The default mode is not to alter placed components.



Design Partitioning

Place replicate now supported in the partition editors.

Polygon Select

Polygon select has been enhanced to automatically finish on double-click, as it would if *Done* were selected.

Undo/Redo Buffer

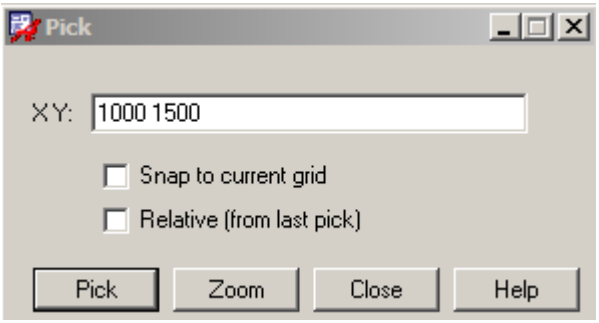
The commands export ipf, flipdesign, associativity off, associativity on, and del_viaarray no longer disable the undo/redo buffer.

Capture Canvas Image

The *Save As* dialog box, in the capture canvas image now defaults to the working directory.

Zoom Button in Pick Dialog

New Zoom button allows users, who work in application modes, access to the zoom center command.



New Variables

- `single_via_replace_default` – Allows user to specify single via replace as default mode when *Tools – Padstack Replace* is run. You can set this variable in the Interactive page of the User Preferences Editor dialog box.
- `text_nocompact` – Disables the Compact button in the text parameter dialog on a per-site basis.
- `options_no_enhanced_padentry` – Use as an initial setting of the *Enhanced Pad Entry* option associated with routing tools.
- `artwork_arc_round_error` – The artwork round warning messages can be made into an error message.
- `testprep_rpt_netnames` – testprep report option to print netnames on each row of report. The default behavior is to suppress the netname when it is the same as the previous row.
- `allegro_nolocking` – When this variable is set, programs will NOT create lock files but will check for the presence of lock files before opening a design.

New Properties

- EMBEDDED_PLACEMENT – enum property (values) Allowed on component definitions and component instances.
- EMBEDDED_SOFT – A boolean property. Allowed at design level.
- EMB_VIA_CONNECT_PADSTACK – A string property allowed at board level.

- EMBEDDED_VIA_KEEPOUT – A boolean property allowed on route keepouts.
- CDS_FSP_PIN_NAME – A string property allowed on pins (see FSP group).
- CDS_FSP_PIN_NUMBER – A string property allowed on pins.
- CDS_FSP_DP_PIN – A string property allowed on pins.
- CDS_FSP_IO_PIN_PAIR – A string property allowed on pins.
- CDS_FSP_DIFF_PIN_TYPE – A string property allowed on pins.
- CDS_FSP_BANK_NAME – A string property allowed on pins.
- CDS_FSP_GROUP_NAME – A string property allowed on pins.
- CDS_FSP_VOLTAGE – A string property allowed on pins.
- CDS_FSP_PIN_TYPE – A string property allowed on pins.
- CDS_FSP_PIN_STD – A string property allowed on pins.
- CDS_FSP_PIN_FUNC – A string property allowed on pins.
- CDS_FSP_CONNECT_INFO – A string property allowed on pins.

Modified Properties

- LOCKED – Now permitted at design-level. This allows adding to a mdd (module) database. When imported into a design resulting module will inherit the LOCKED attribute which means object editing within a module is not permitted. Same capability that is present with symbols.
- BACKDRILL_MAX_PTH_STUB – Now supported on vias and pins.
- CDS_FSP_NET – Renamed from FSP_NET and now allowed on pins (see FSP group).
- CDS_FSP_INSTANCE_NAME – Renamed from FSP_INSTANCE_NAME
- CDS_FSP_INSTANCE_ID – Renamed from FSP_INSTANCE_ID
- CDS_FSP_IS_FPGA – Renamed from FSP_IS_FPGA
- CDS_FSP_TERMINATION_TYPE – Renamed from FSP_TERMINATION_TYPE
- CDS_FSP_LIB_PART_MODEL – Renamed from FSP_LIB_PART_MODEL

Deleted Properties

- THERMAL_RELIEF – This property is now stored as a base attribute for performance reasons. Legacy access via Skill and extracta are provided.

Reports

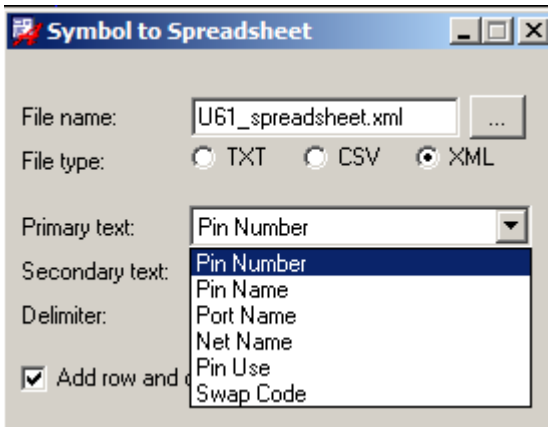
- Dangling via report now includes start/stop layers of dangling vias and antenna vias.
- Embedded Component (new)
- Embedded Cavities (new)
- Etch Detailed Length (new)
- Cross Section (new)

IDF Out

Added Package Keepin in the filter setup dialog as an exclude option.

Symbol Export

The *Symbol Export to Spreadsheet* feature of SiP now available in PCB Editor. Use this feature to output pin fields in `.txt`, `.csv` or `xml` formats. To access this command, choose *File – Export – Symbol Spreadsheet*.



Data Migration

- The Max Neck Width DRC is now a continuous cumulative check whereas older releases did it as a segment check. This may result in more DRCs in 16.5 designs. Cadence strongly feels that this is the correct way to do this check so no option is provided to run the check in its segment based mode.
- It you utilize embedded component design, you will first need to delete all your embedded components before you are allowed to downrev your design.
- There is no mechanism in place to convert your 16.3 dimensions to the new style associative dimensions.
- When embedded components are present, the `plctxt` output format utilizes a new format (rev 2). This cannot be read by earlier Allegro releases.
- It is no longer possible to directly downrev a design to release 16.01 from 16.5.

Script Migration

Pre-16.5 scripts performing dimensioning actions will not work in 16.5.

Skill Enhancements

As always you should check `<cdsroot>/share/pcb/examples/skill/DOC` for what new functions are available in this release. Noteworthy updates …

- Access to color patterns available
- Full access to Constraint Class tables
- Full access to grids and text blocks now available

RF PCB Enhancements

In this release several enhancements have been made in RF PCB to increase your productivity.

- Usability Enhancements
- IFF Interface Enhancements
  - Layer mapping for non-etch layers
  - Hierarchical component importing
  - RefDes Auto-synch
- Layout Enhancements
  - Breaking RF Components
  - Inserting RF Components
  - Converting RF Components
  - Shape to Component Enhancements
  - RF Push Enhancements

Usability Enhancements

Allegro PCB Editor provides a new application mode, RF Application Edit mode. This application mode provides quick and easy access to RF command specific to the selected object or group of objects. This application mode configures the tool for a specific task by populating the right mouse button pop-up menu with RF commands that operate on the currently selected RF object or group of RF objects. In addition, the menu also displays some generic RF commands (not specific to the object or objects selected) under a Quick Utilities sub-menu of the RMB.

IFF Interface Enhancements

The IFF interface import procedure now includes a number of enhancements.

Layer mapping for non-etch layers

In previous releases of RF PCB, the IFF import procedure allowed you to map only ETCH layers. However, now you can also map non-ETCH layers during import.

Hierarchical component importing

Also, the RF PCB IFF import procedure interprets elements within a hierarchical layout component in ADS, and generates the corresponding Allegro layout elements.

RefDes Auto-synch

As part of the import procedure, RF PCB now ensures that the schematic and layout files are synchronized by ensuring that the reference designators are assigned for each component imported into the schematic and layout files.

Layout Enhancements

This release includes a number of enhancements that help in the layout of RF components on the board. These include a number of enhancements to existing commands as well as a new command that allows you to break RF components on the board.

Breaking RF Components

Allegro PCB Editor includes a new rf_break command that allows you to break an RF component placed on your board.

You can break a component by percentage (applicable for all valid types of components), by length (applicable for LINE type components), by angle (applicable for CURVE type components), or by electrical length (applicable for MLIN, MCURVE, MCURVE2).

Inserting RF Components

The Add component and Scaled copy commands are now enhanced to allow you to insert an RF component between two RF components on the board.

Converting RF Components

If you are in the rf_change mode, you can now change the RF type of certain types of RF components:

- Line to Taper
- Taper to Line
- Line to Gap
- Gap to Line

- Taper to Gap
- Gap to Taper

Shape to Component Enhancements

In previous releases of RF PCB, you could convert a static shape to a component and save it for reuse by choosing RF-PCB – Convert – Shape to Component. However, now you can also select vias along with the shapes to convert. This will cause the vias to be included in the RF component after conversion.

RF Push Enhancements

The RF Push command is now enhanced to allow you to also push vias and user-defined vias.

What’s New for Older Releases

This section lists the What’s New for older releases of Allegro PCB Editor.

- Allegro PCB Editor: What's New in Release 16.3
- Allegro PCB Editor: What's New in Release 16.2
- Allegro PCB Editor: What's New in Release 16.01
- Allegro PCB Editor: What's New in Release 16.0