

Technical Paper #2: How to Back Annotate in ORCAD after re-sequencing is done in Allegro Layout.
© 2007 Baykal Technology, Inc.
Emre Uludemir, Founder

Table of Contents:	Page
Introduction:.....	2
Why do we need back annotation in schematics?:.....	2
What is a safe method for back annotation in ORCAD?:.....	2
How is re-sequencing done in Allegro?:.....	2
Example Allegro re-sequencing report:	4
How do we make a Was-is-file from Allegro re-sequencing file report (rename.log)?:	4
How do we back annotate in ORCAD?:.....	5
Possible error you might encounter during Back Annotation in ORCAD:	6
How to keep certain Reference Designators same through out the re-sequencing period?.....	6

Table of Figures:	Page
Figure 1: How to re-sequence Reference Designators in Allegro.	3
Figure 2: How to back annotate in ORCAD.....	5
Figure 3: Allegro Component Properties, default no property defined.	6
Figure 4: How to enter HARD_LOCATION property into your ORCAD schematics.....	7
Figure 5: How to pass HARD_LOCATION component property from ORCAD schematics to Allegro PCB.....	8
Figure 6: After importing HARD_LOCATION from schematics, we see that property exists now	9

Examples are given in ORCAD Schematics Capture ver 10.5, Allegro SPB 15.5

For additional questions please contact Emre Uludemir :
emre@baykal.com

Introduction:

This technical paper explains how to re-sequence the Allegro Database, how to prevent certain reference designators to be re-sequenced by adding a special property into ORCAD schematics database. How to safe back annotate your schematics, without disturbing any schematics properties (safe back annotation method), and file formats required in order to properly back annotate without errors.

Why do we need back annotation in schematics?:

For small boards it may not be critical, but when component sizes on the board goes beyond 100 especially after passing thousands, it becomes very difficult to locate components on the board. By having the PCB reference designators re-sequenced in a typical order, for example left to right first top side and then right to left on bottom side, it would be much easier to locate components in the lab or at the field servicing the board. The re-sequencing is done after all component placements are checked and frozen. PCB is then re-sequenced and a re-sequence report gets generated from the layout software such as Allegro. Then this information is imported back to ORCAD through a safe back annotation method which we discuss in this technical paper.

Also for Design For Manufacturability (DFM), it is much desired to have a board with incremental reference designators. This way for every type of reference designator, you can tell max number of components.

What is a safe method for back annotation in ORCAD?:

ORCAD has a very convenient Allegro interface for back annotation. But the dedicated import file format (*.swp) which is produced from Allegro Layout software could have altered properties, or new additional ones which is determined by the layout designer. By importing through this (swp) method, your schematics become vulnerable to un-controlled change. This way of importing re-sequenced board data from Allegro Layout Software, could change your ORCAD schematics properties, especially Net related precious properties if you have spent hours to have a complete schematics that reflects all proper Physical and Space type rules you have entered into your schematics. After importing huge file (.swp) , you can never be sure what is changed. It would be very painful to discover that some of your net properties in schematics is replaced by Allegro Designers modified properties, or could be erased or changed, you would never know unless you check everything one by one. But, we just want to update reference designators, that is it.

Well there is a safer way. Tell ORCAD that the re-sequencing is done in non-Allegro layout tool even though it is done in Allegro. Luckily, the report that produced in Allegro, *.rep can be manually modified to arrive at a Was-is file type as described in the next paragraphs.

How is re-sequencing done in Allegro?:

Below is an example Allegro Database, and steps to re-sequence the board after all placement on board is frozen and the board is almost ready for release, now it is time to re-sequence for DFM and easy part location.

To re-sequence the board in Allegro, from top menu:

Logic: Auto Rename RefDes: Rename

This selection above will bring you “Rename RefDes” dialog box on left side of the picture below. Then, click on “More” on the opened dialog box.

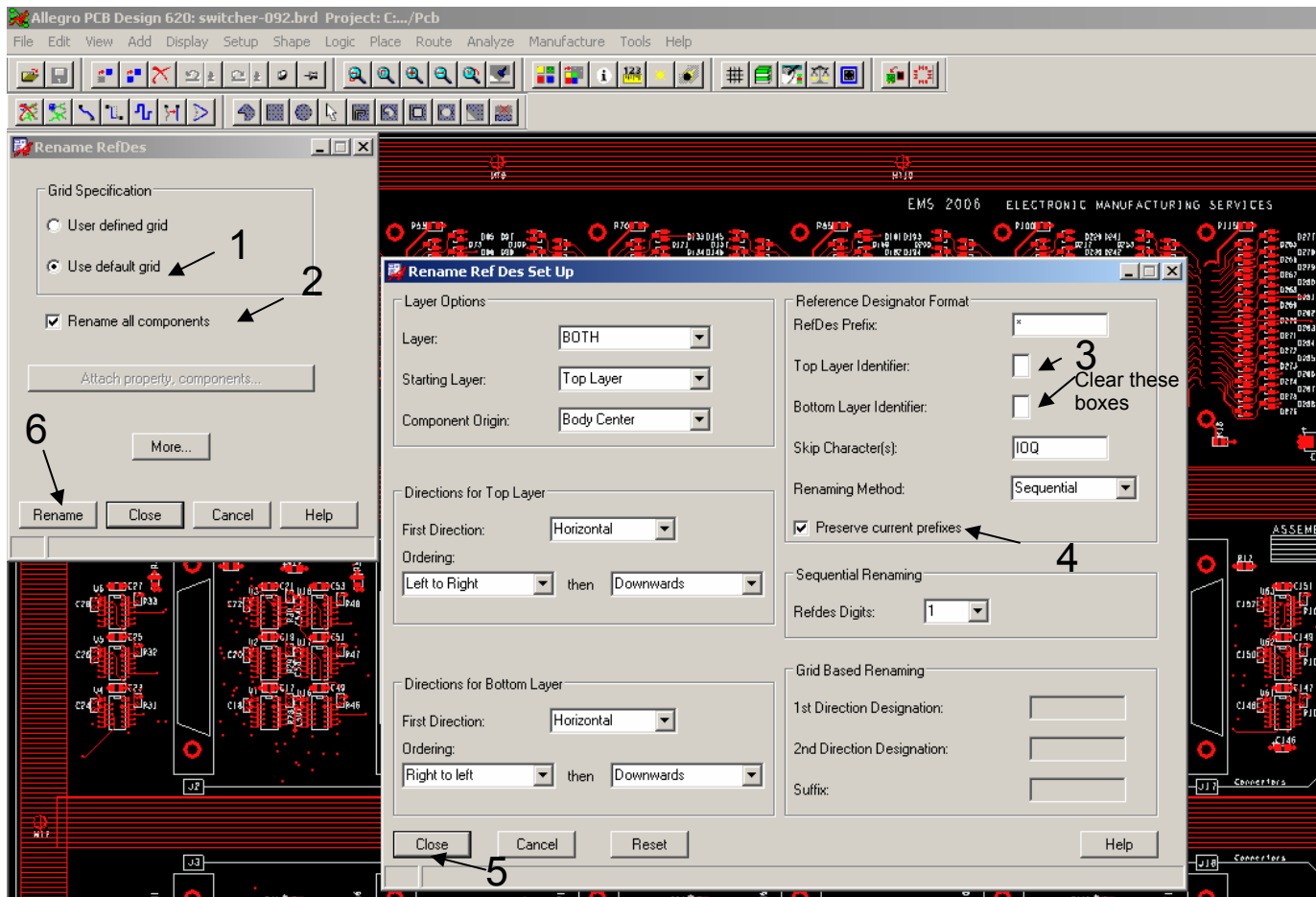


Figure 1: How to re-sequence Reference Designators in Allegro.

- (1) You can use default grid
- (2) Make sure “Rename all components” is selected
- (3) Clear boxes “Top, Bottom Layer Identifiers”, we want our Reference Designator Later un-touched.
- (4) Check, “Preserve current properties”
- (5) Now close “Rename Ref Des Set Up” dialog box, by clicking on the Close button.
- (6) Finally, click on “Rename” button on “Rename RefDes” dialog Box on left.

After renaming operation is completed in Allegro below is an example report on command screen in Allegro:

```
RENAMES COMPLETED = 660   REMAIN = 22.
RENAMES COMPLETED = 670   REMAIN = 12.
RENAMES COMPLETED = 680   REMAIN = 2.
Auto rename of Refdes COMPLETE.  688 components renamed.
Command >
```

Example Allegro re-sequencing report:

After re-sequencing is done in Allegro, it produces the report file called “rename.log”. This file is in plain text format. We will use this file to produce the was-is file which later we will use it for back annotation in the ORCAD schematics. Below is a sample rename.log file for an example.

```
(-----)
(  RENAME REFDES      )
(  Drawing      : BK-1289200-verB.brd )
(-----)
Renaming components on BOTH_SIDES on entire BOARD
  Extents: (-19900.0,-19900.0) (26100.0,16100.0)
Sequencing the Reference Designators SEQUENTIALLY
Row processing direction : to the RIGHT, from the top down.
Processing TOP of board, C340 has AUTO_RENAME property but is on BOTTOM, component ignored.
Processing TOP of board, C155 has AUTO_RENAME property but is on BOTTOM, component ignored.
OLD C1  NEW C1
OLD Q1  NEW Q1
OLD C2  NEW C2
OLD TP1 NEW TP1
OLD TP2 NEW TP2
OLD TP3 NEW TP3
OLD R1  NEW R1
OLD L1  NEW L1
OLD C4  NEW C3
OLD C5  NEW C4
OLD C6  NEW C5
OLD TP8 NEW TP4
OLD TP4 NEW TP5
OLD U1  NEW U1
```

(Note: Above section is what we need to produce was-is file)

Processing TOP of board, R172 has AUTO_RENAME property but is on BOTTOM, component ignored.

HARD_LOCATION property on J1, component ignored.

Processing TOP of board, RP67 has AUTO_RENAME property but is on BOTTOM, component ignored.

(Note: Above a HARD_LOCATION message , this prevents from that component to be re-sequenced)

How do we make a Was-is-file from Allegro re-sequencing file report (rename.log) ?:

Open “rename.log” file in a Text editor. Copy all the line starting with OLD xx NEW yy. Copy these sections into a new text file. Once you go through the report file, and you made sure all lines are copied, (you can also cut and paste which would be easier to trace if you missed any lines), save this new file as “was-is-file.txt”. Now you have copied all replacement reports from report file to the new was-is file. All you have to do now is to search and replace “OLD” with nothing and replace “NEW” with nothing. Basically, erase “OLD” and “NEW” prefixes, we do not need them. The file can be any file extension, but essentially it is a text file indicating each component reference update in a separate line. Beginning with old component reference designator and “SPACE” and the new reference designator.

Example “was-is-file.txt” file:

```
Q1  Q1
C2  C2
TP1 TP1
C4  C3
U3000 U4
.
.
```

Explanation:

Q1 reference designator is not changed after re-sequencing in Allegro.
C2 reference designator is not changed after re-sequencing in Allegro.
TP1 reference designator is not changed after re-sequencing in Allegro
C4 became C3 after re-sequencing in Allegro.
U3000 became U4 after re-sequencing in Allegro.

How do we back annotate in ORCAD?:

From Project window, select (highlight) your_design.dsn.

- (1) From buttons at top (or from menu) click on Back-annotation.
- (2) Backannotate dialog box appears, here at top, select “Layout” tab (Non-allegro back annotation)
- (3) Browse to you was is file location.
- (4)

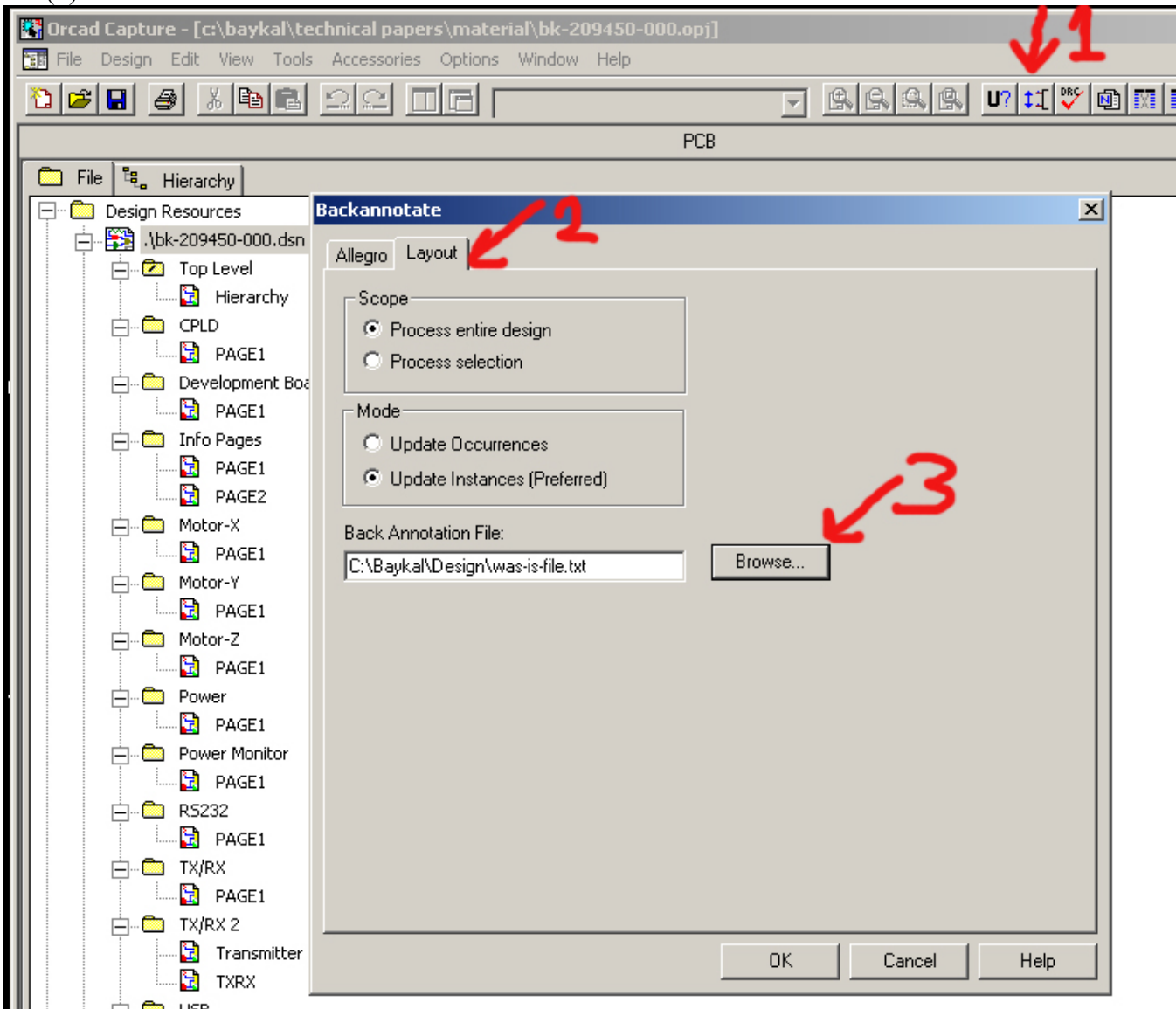


Figure 2: How to back annotate in ORCAD

After back annotation go to Session log and make sure that the back annotation is completed with success like the example session log below. Also make sure to run DRC check after back annotation just incase.

* Performing back annotation.

Back annotation complete.

Possible error you might encounter during Back Annotation in ORCAD:

File format is wrong? Was is file was not formatted properly, received this error in ORCAD:

```
*****
*
* Performing back annotation.
*
*****
ERROR [GAT0031] (Line 1) Invalid line in swap file. Possibly a misspelled keyword. OLD C1 NEW C1
Back annotation complete.
```

The reason for back annotation error is that, “was-is-file.txt” does not have the correct format. Was is file does not have proper format, remove “OLD”, “NEW”:

```
OLD Q1 NEW Q1
OLD C2 NEW C2
OLD TP1 NEW TP1
OLD TP2 NEW TP2
OLD TP3 NEW TP3
OLD R1 NEW R1
OLD L1 NEW L1
OLD C4 NEW C3
OLD C5 NEW C4
```

This fix of removal of “OLD”, “NEW” prefix fixes it.

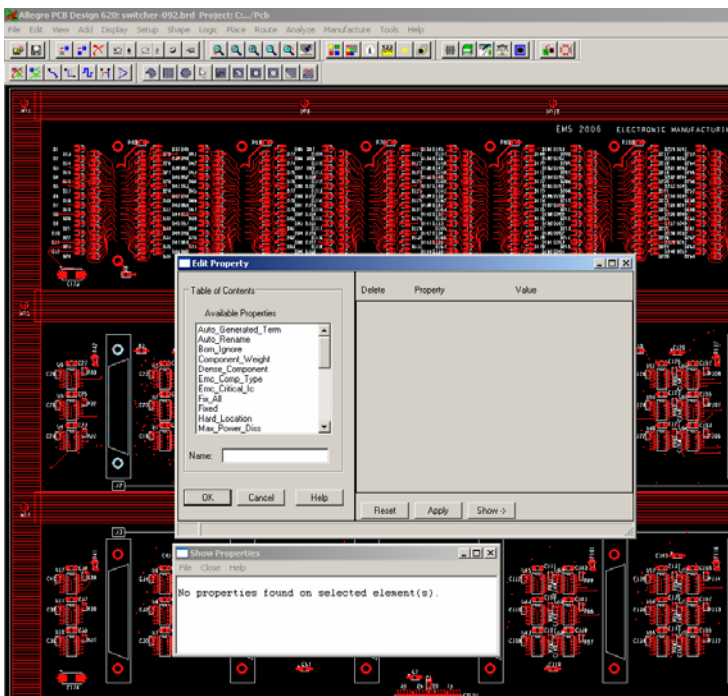
Just have this in each line:

Search and replace all “OLD” with “” (Nothing)

Search and replace all “NEW” with “” (Nothing)

How to keep certain Reference Designators same through out the re-sequencing period?

First let’s take a look at the Component Instance property in Allegro which affects the particular component’s auto re-sequencing state. Below is a sample design which we will use for auto re-sequencing.



If HARD_LOCATION property is defined in PCB, that component will retain the same reference designator after re-sequencing is done. In some design we might like to have some components retaining reference designators, such as CompactPCI connectors (J1, J2,...J4) or face plate related connectors or LED references to match certain mechanical drawings.

On Figure 3 on left, we do not see the special property HARD_LOCATION defined for the highlighted component, in this case a connector. If we re-sequence this board, the reference designator for this connector will be replaced by the re-sequenced one. In this example, we prevent all connector reference designators from being replaced, by defining HARD_LOCATION property for these components.

Figure 3: Allegro Component Properties, default no property defined.

Now let's us modify our ORCAD schematics, go to particular ORCAD schematics page, select the components you wish to have "HARD_LOCATION" property so that they would retain their reference designators after re-sequencing in Allegro. You can select as many components as you wish and then right click, then say "Edit Properties". This will bring the ORCAD property editor for the components that you just selected. Below is an example. Then make sure, you have the "Filter by: Cadence-Allegro" in the section left to the Help button. This will bring the properties that we can pass to Allegro.

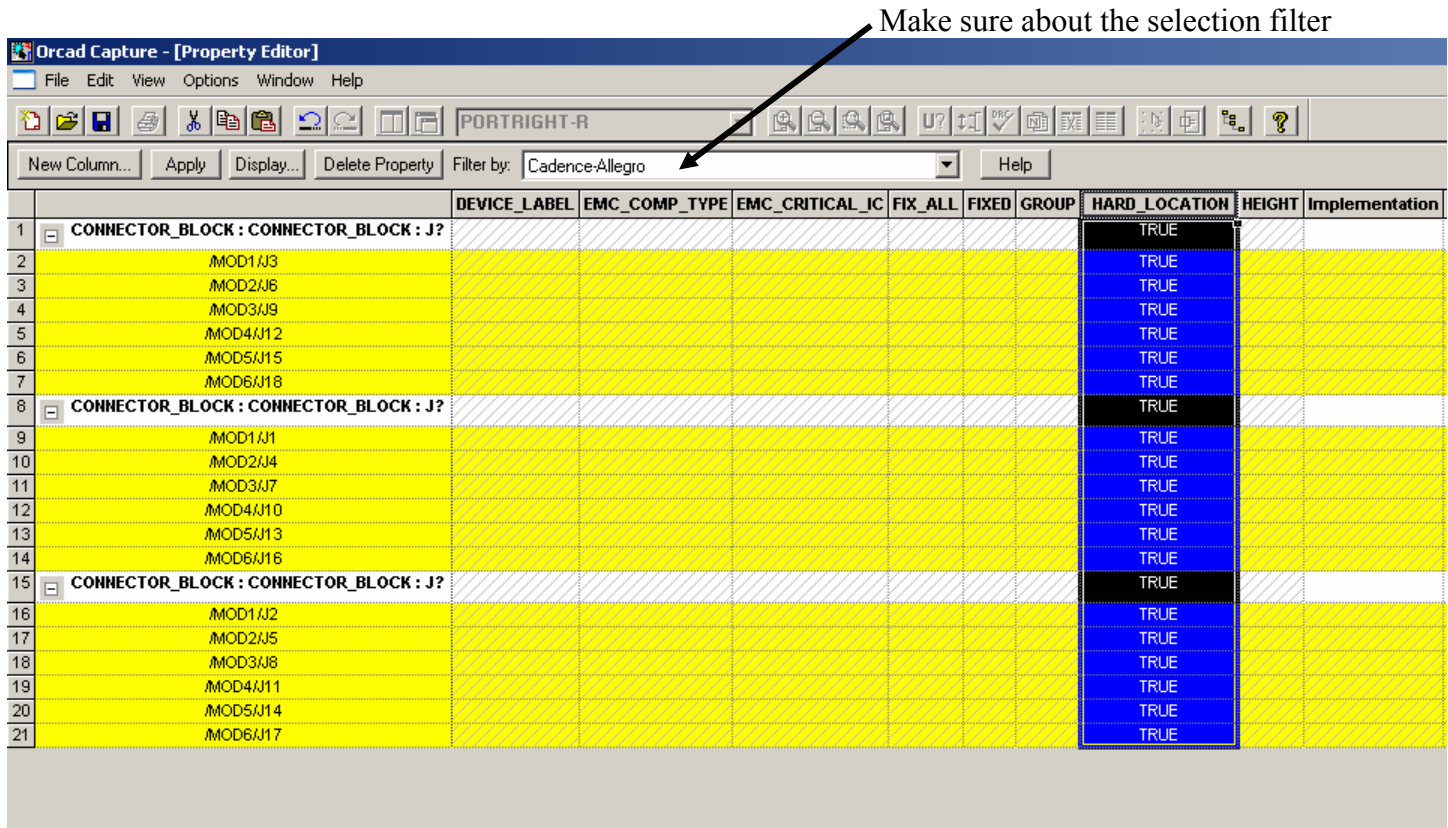


Figure 4: How to enter HARD_LOCATION property into your ORCAD schematics

Click on HARD_LOCATION field (Column) this will highlight whole column. Then move your mouse right over the HARD_LOCATION label at the top of the highlighted column. Right click as the mouse arrow points in the box for the HARD_LOCATION label. Now this will bring a small selection, go for "Edit", and then type TRUE. This will later all HARD_LOCATION field for all the components in one entry, saving you time. Otherwise you can also click on each empty area and type "HARD_LOCATION".

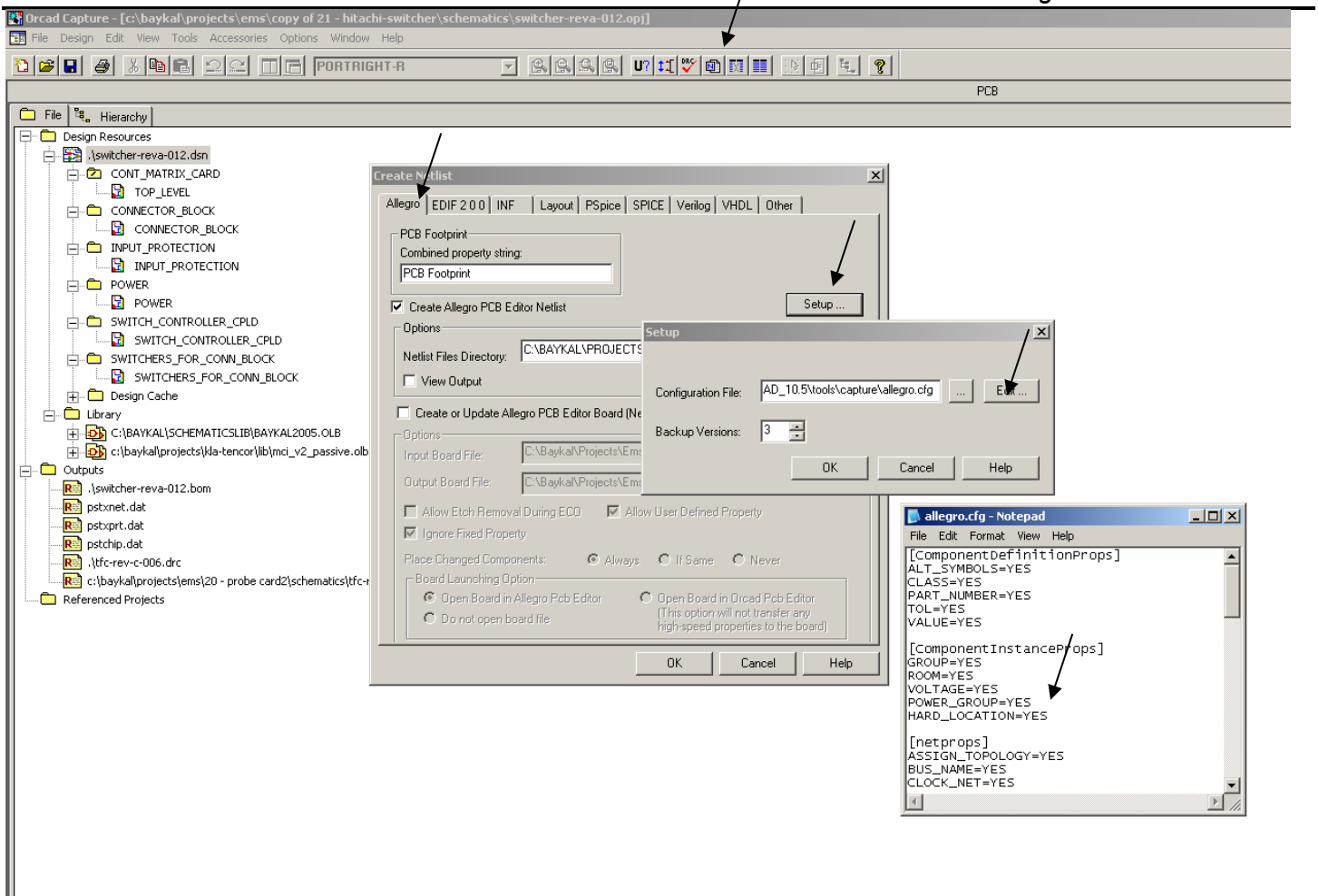


Figure 5: How to pass HARD_LOCATION component property from ORCAD schematics to Allegro PCB.

For the defined property to safely pass to Allegro we need to modify the allegro.cfg text file. You can see this file opened in Figure 2, bottom right. To do this in your ORCAD schematics:

Create Netlist

Allegro Tab

Check: Create Allegro PCB Editor Netlist

Hit: Setup, this will take you to Allegro.cfg text file.

Modify Allegro.cfg file, section "[ComponentInstanceProps]", as below:

[ComponentInstanceProps]

GROUP=YES

ROOM=YES

VOLTAGE=YES

POWER_GROUP=YES

HARD_LOCATION=YES (Edit and put this in)

Now generate new netlist and import it to Allegro. If you followed all the steps up to here, below in the particular component properties, you should see **HARD_LOCATION** defined. Value of **HARD_LOCATION** may not be set to “TRUE” as we indicated in our ORCAD schematics, but it will work fine, no manual modification to the **HARD_LOCATION** property is required.

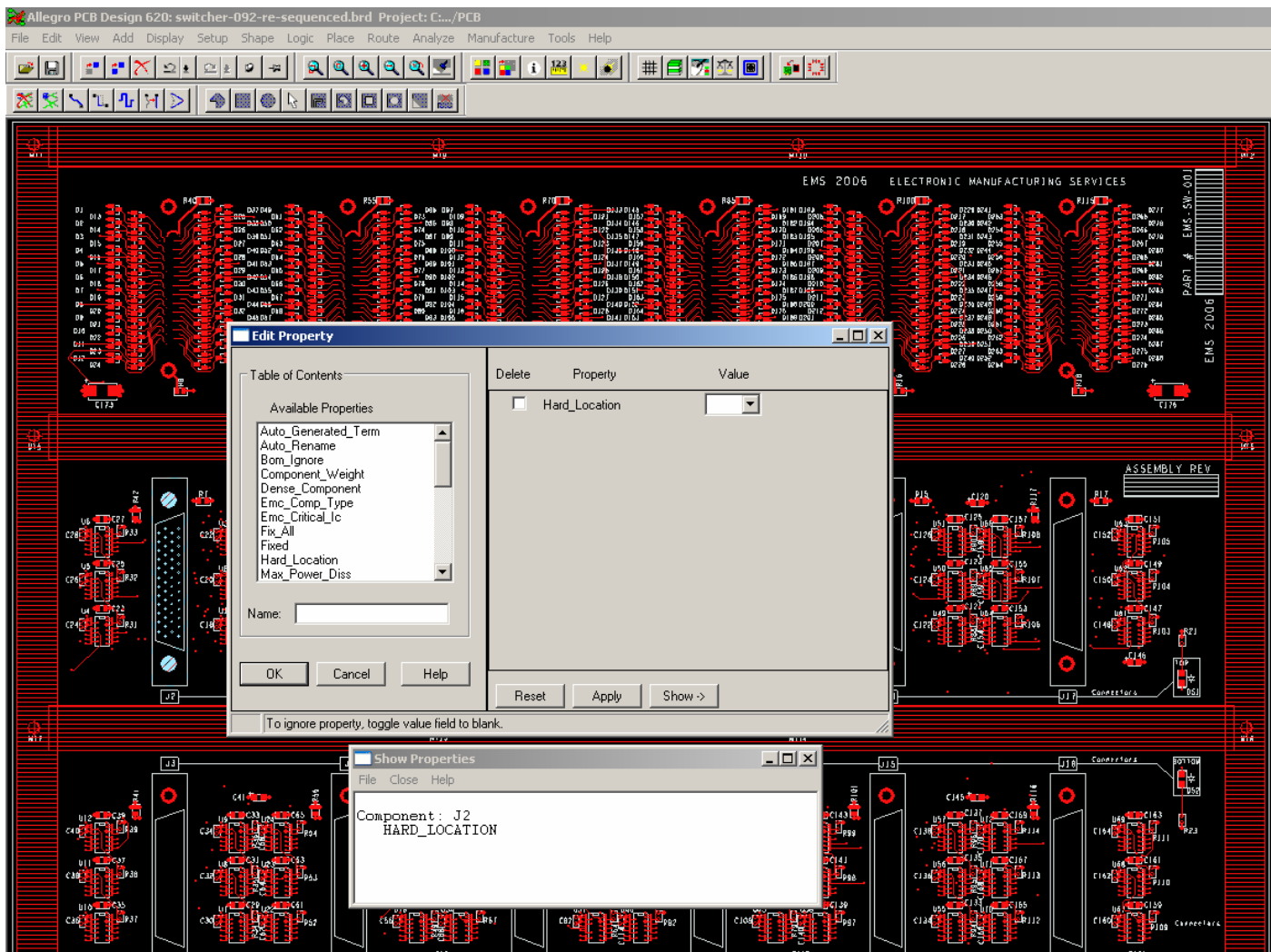


Figure 6: After importing **HARD_LOCATION** from schematics, we see that property exists now