# MPM3510A

## 36V/1.2A Module Synchronous Step-Down Converter with Integrated Inductor

The Future of Analog IC Technology

## DESCRIPTION

The MPM3510A is a synchronous, rectified, step-down converter with built-in power MOSFETs, inductor, and two capacitors. It offers a compact solution with only 4 external components to achieve a 1.2A continuous output current with excellent load and line regulation over a wide input supply range. The MPM3510A operates in a 1.15MHz switching frequency, which provides fast load transient response.

Full protection features include over-current protection (OCP) and thermal shutdown (TSD).

The MPM3510A eliminates design and manufacturing risks while dramatically improving time-to-market.

The MPM3510A is available in a space-saving QFN-19 (3mmx5mmx1.6mm) package.

## FEATURES

- Complete Switch Mode Power Supply
- 4.5V to 36V Wide Operating Input Range
- 1.2A Continuous Load Current
- 80mΩ/50mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- Fixed 1.15MHz Switching Frequency
- 800kHz to 2MHz Frequency Sync
- Power-Save Mode for Light Load
- Power Good Indicator
- OCP with Valley-Current Detection and Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in a QFN-19 (3mmx5mmx1.6mm) Package
- Total Solution Size 6.7mmx6.3mm

## APPLICATIONS

- Industrial Controls
- Automotive
- Medical and Imaging Equipment
- Telecom Applications
- LDO Replacement
- Space and Resource-Limited Applications
- Distributed Power Systems

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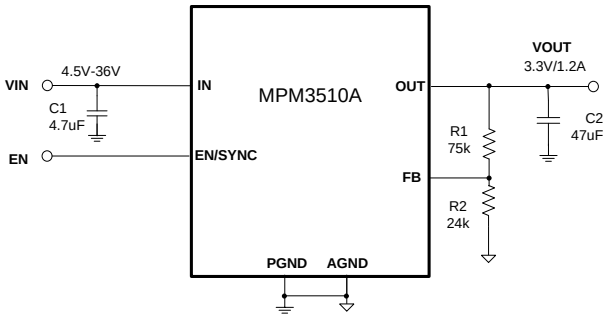
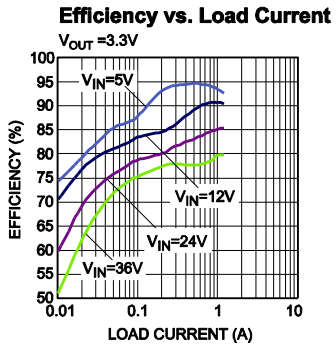
## TYPICAL APPLICATION





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## ORDERING INFORMATION

| Part Number* | Package | Top Marking |
|---|---|---|
| MPM3510AGQV | QFN-19 (3mmx5mmx1.6mm) | *See Below* |

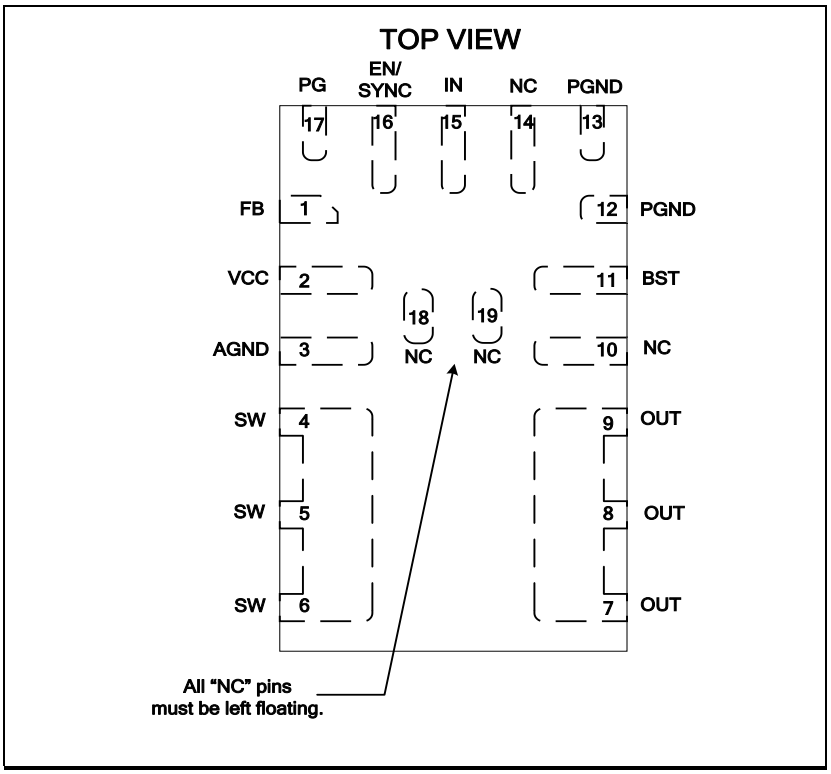
* For Tape & Reel, add suffix –Z (eg. MPM3510AGQV –Z)

## TOP MARKING

MPYW
3510
ALLL
M

MP: MPS prefix
Y: Year code
W: Week code
3510A: First four digits of the part number
LLL: Lot number
M: Module

## PACKAGE REFERENCE





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## ABSOLUTE MAXIMUM RATINGS (1)

$V_{IN}$, $V_{OUT}$ ..... -0.3V to 40V
$V_{SW}$ .....
-0.3V (-5V for <10ns) to $V_{IN}$+0.3V (43V for <10ns)
$V_{BST}$ ..... $V_{SW}$+6V
All other pins.....-0.3V to 6V (2)
Continuous power dissipation ($T_A$ = +25°C) (3)
.....2.7W
Junction temperature.....150°C
Lead temperature .....260°C
Storage temperature.....-65°C to 150°C

## *Recommended Operating Conditions* (4)

Supply voltage ($V_{IN}$) ..... 4.5V to 36V
Output voltage ($V_{OUT}$).....0.81V to $V_{IN}$*$D_{Max}$
Operating junction temp. ($T_J$). ..-40°C to +125°C

## *Thermal Resistance* (5) $\theta_{JA}$ $\theta_{JC}$

| | | |
|---|---|---|
| QFN-19 (3mmx5mmx1.6mm) | 46 | 10 °C/W |

**NOTES:**

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) For additional details on EN's ABS MAX rating, please refer to the "Enable/SYNC" section on page 12.
3) The maximum power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX)-$T_A$)/$\theta_{JA}$. Exceeding the maximum allowable power dissipation will produce an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.


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## ELECTRICAL CHARACTERISTICS

**$V_{IN}$ = 24V, $T_J$ = -40°C to +125°C(6), unless otherwise noted. Typical values are at $T_J$ = +25°C.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Supply current (shutdown) | $I_{IN}$ | $V_{EN}$ = 0V | | | 8 | μA |
| Supply current (quiescent) | $I_q$ | $V_{FB}$ = 1V | | 0.58 | 0.8 | mA |
| HS switch-on resistance | $HS_{RDS-ON}$ | $V_{BST-SW}$ = 5V | | 80 | 155 | mΩ |
| LS switch-on resistance | $LS_{RDS-ON}$ | $V_{CC}$ = 5V | | 50 | 105 | mΩ |
| Inductor DC resistance | $L_{DCR}$ | | | 75 | | mΩ |
| Switch leakage | $SW_{LKG}$ | $V_{EN}$ = 0V, $V_{SW}$ = 24V | | | 1 | μA |
| High-side peak current limit | $I_{PEAK_LIMIT}$ | 20% duty cycle | 3 | 4.3 | | A |
| Low-side valley current limit | $I_{VALLEY_LIMIT}$ | Vout short to GND | | 1.5 | | A |
| Oscillator frequency | $f_{SW}$ | $V_{FB}$ = 700mV | 800 | 1150 | 1500 | kHz |
| Maximum duty cycle | $D_{MAX}$ | $V_{FB}$ = 700mV | 89 | 92 | | % |
| Minimum on time(7) | $T_{ON_MIN}$ | | | 50 | | ns |
| Feedback voltage | $V_{FB}$ | $T_J$ = 25°C | 798 | 810 | 822 | mV |
| | | $T_J$ = -40°C to +125°C | 790 | | 830 | mV |
| Feedback current | $I_{FB}$ | $V_{FB}$ = 850mV | | 10 | 100 | nA |
| EN rising threshold | $V_{EN_RISING}$ | | 1.1 | 1.45 | 1.8 | V |
| EN falling threshold | $V_{EN_FALLING}$ | | 0.95 | 1.3 | 1.65 | V |
| EN input current | $I_{EN}$ | $V_{EN}$ = 2V | | 4 | 7 | μA |
| EN turn-off delay(7) | $EN_{Td-off}$ | | | 3 | | μs |
| SYNC frequency range | $f_{SYNC}$ | | 800 | | 2000 | kHz |
| VIN under-voltage lockout threshold—rising | $INUV_{Vth}$ | | 3.75 | 4.05 | 4.35 | V |
| VIN under-voltage lockout threshold—hysteresis | $INUV_{HYS}$ | | | 400 | | mV |
| PG rising threshold | $PG_{Vth-Hi}$ | | 84% | 87.5% | 91% | $V_{FB}$ |
| PG falling threshold | $PG_{Vth-Lo}$ | | 79% | 82.5% | 86% | $V_{FB}$ |
| PG rising delay | $PG_{Td_Rising}$ | | 30 | 90 | 160 | μs |
| PG falling delay | $PG_{Td_Falling}$ | | 25 | 55 | 95 | μs |
| PG sink current capability | $V_{PG}$ | Sink 4mA | | | 0.4 | V |
| PG leakage current | $I_{PG-LEAK}$ | | | | 100 | nA |
| VCC regulator | $V_{CC}$ | | 4.6 | 4.9 | 5.2 | V |
| VCC load regulation | | $I_{CC}$ = 5mA | | 1.5 | 4 | % |
| Soft-start time | $t_{SS}$ | $V_{OUT}$ from 10% to 90% | 0.5 | 1.45 | 2.5 | ms |
| Thermal shutdown (7) | | | | 165 | | °C |
| Thermal hysteresis (7) | | | | 20 | | °C |

**NOTES:**

6) Not tested in production and guaranteed by over-temperature correlation.

7) Derived from characterization test. Not tested in production.


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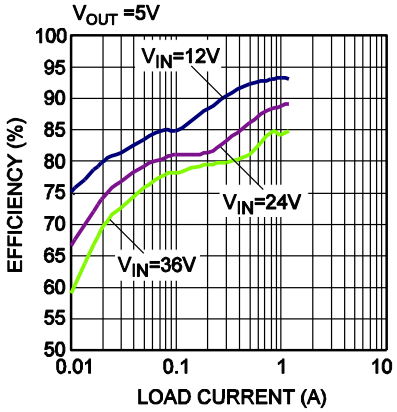
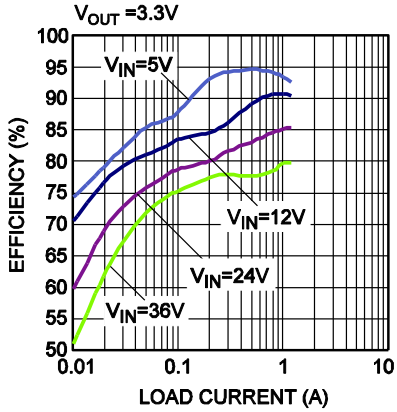
# TYPICAL PERFORMANCE CHARACTERISTICS

**Typical performance characteristic waveforms are produced from the evaluation board. $V_{IN}$ = 24V, $V_{OUT}$ = 3.3V, $T_A$ = 25°C, unless otherwise noted.**

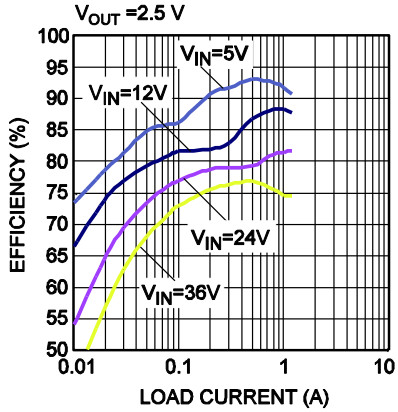
**Efficiency vs. Load Current**



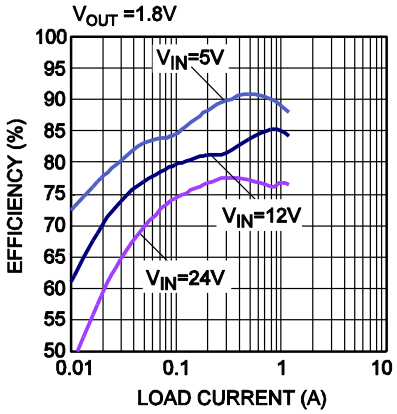

**Efficiency vs. Load Current**



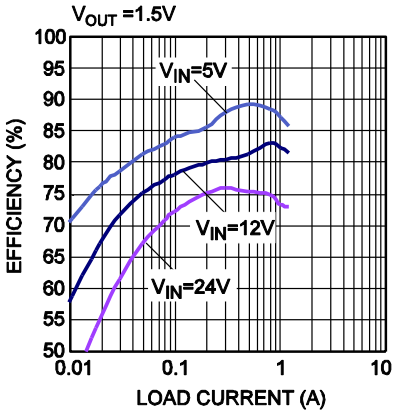

**Efficiency vs. Load Current**



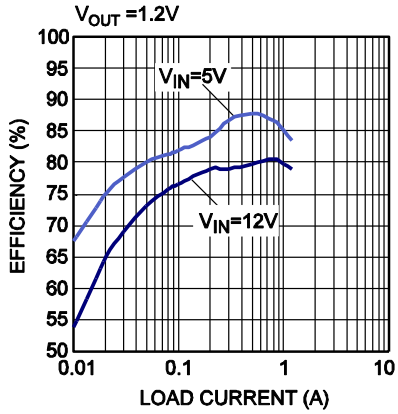

**Efficiency vs. Load Current**



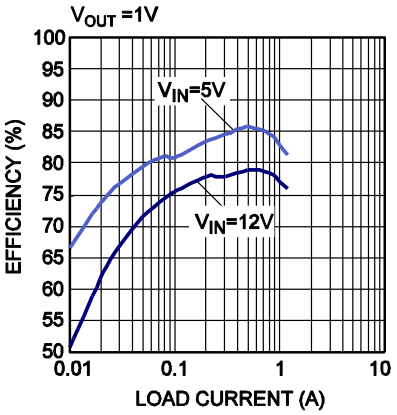

**Efficiency vs. Load Current**



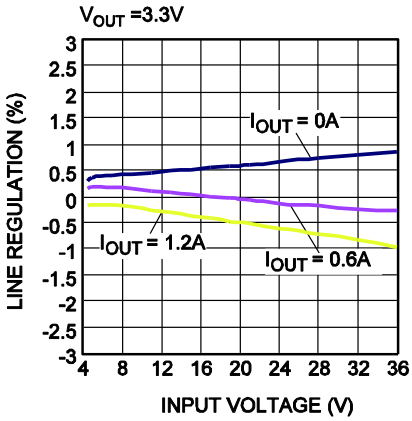

**Efficiency vs. Load Current**



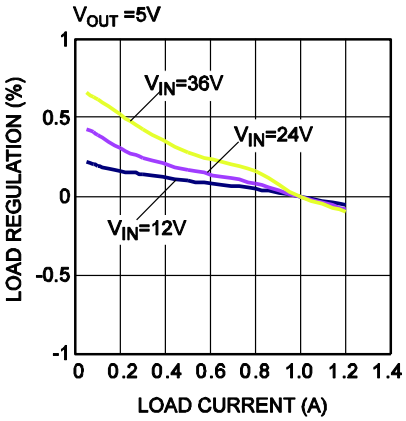

**Efficiency vs. Load Current**




**Line Regulation**




**Load Regulation**





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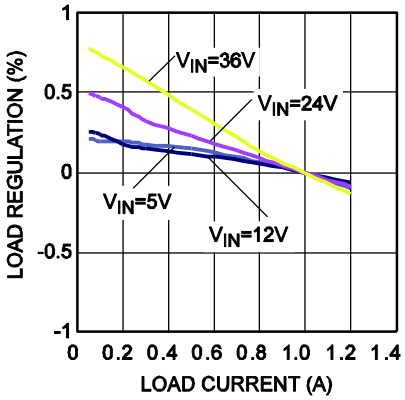
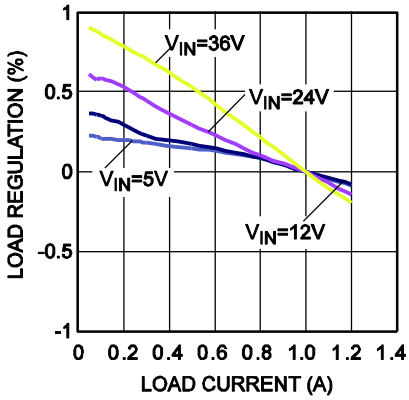
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**Typical performance characteristic waveforms are produced from the evaluation board.**
**$V_{IN}$ = 24V, $V_{OUT}$ = 3.3V, $T_A$ = 25°C, unless otherwise noted.**

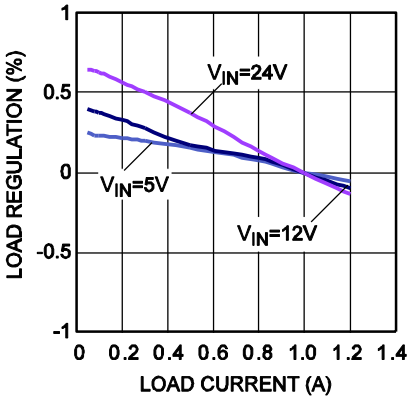
**Load Regulation**
$V_{OUT}$ =3.3V



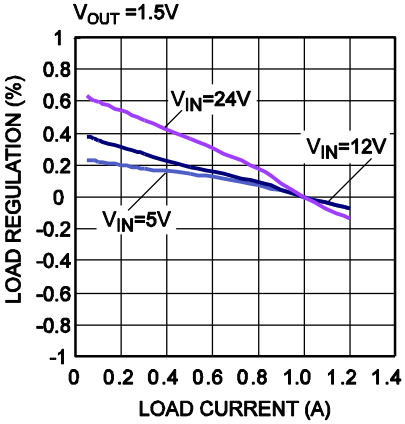

**Load Regulation**
$V_{OUT}$ =2.5V



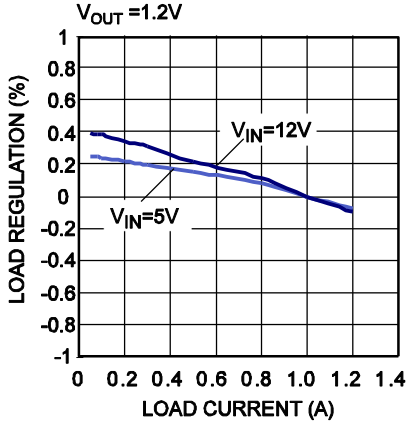

**Load Regulation**
$V_{OUT}$ =1.8V



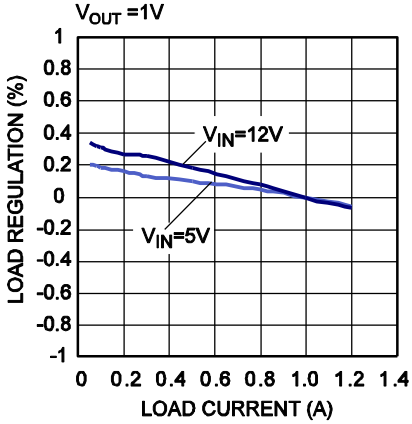

**Load Regulation**
$V_{OUT}$ =1.5V



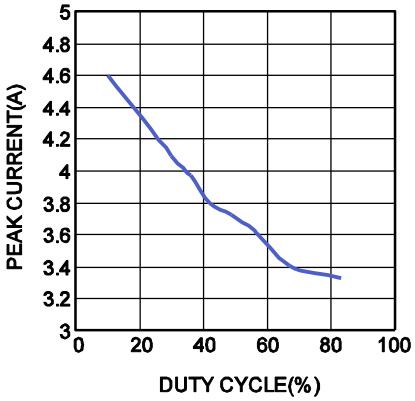

**Load Regulation**
$V_{OUT}$ =1.2V



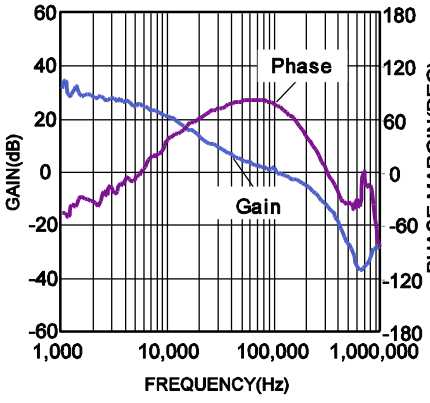

**Load Regulation**
$V_{OUT}$ =1V



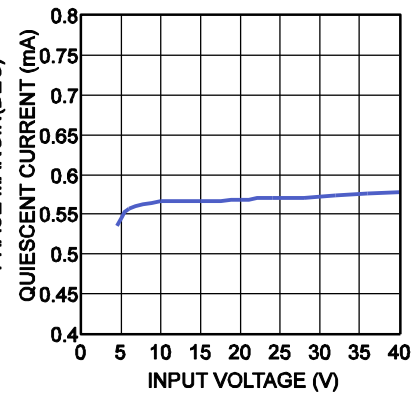

**Peak Current vs. Duty Cycle**




**Bode Plot**
$I_{OUT}$ =1.2A




**Quiescent Current vs. Input Voltage**





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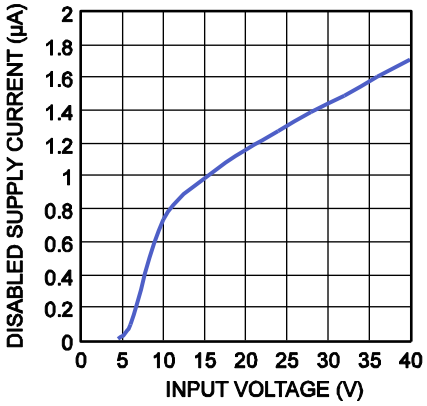
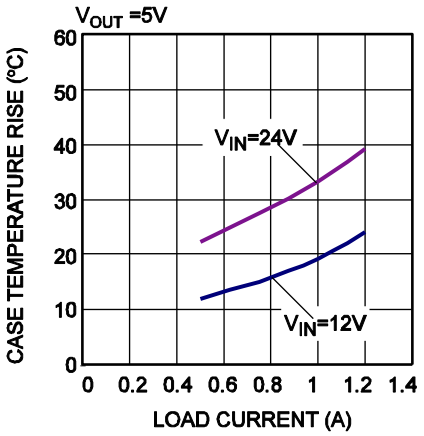
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**Typical performance characteristic waveforms are produced from the evaluation board.**
**$V_{IN}$ = 24V, $V_{OUT}$ = 3.3V, $T_A$ = 25°C, unless otherwise noted.**

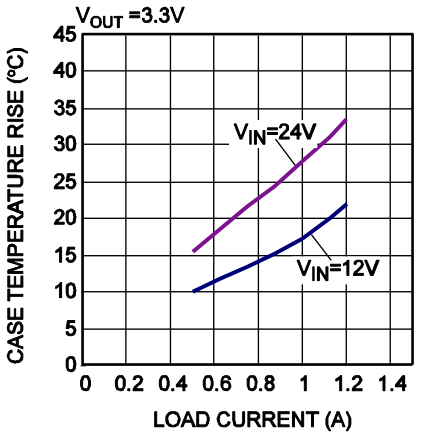
**Disabled Supply Current vs. Input Voltage**



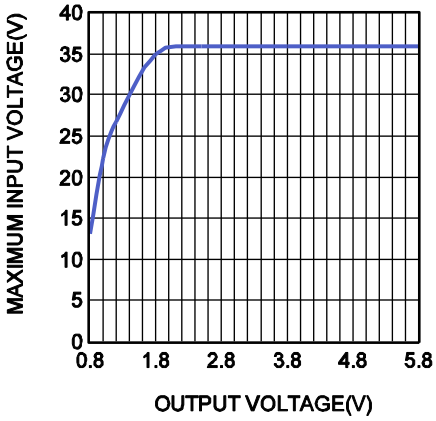

**Case Temperature Rise vs. Output Current**




**Case Temperature Rise vs. Output Current**




**Maximum $V_{IN}$ vs. Output Volatge**





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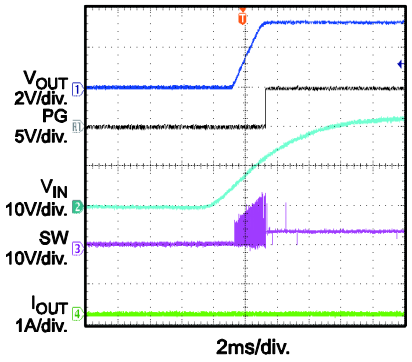
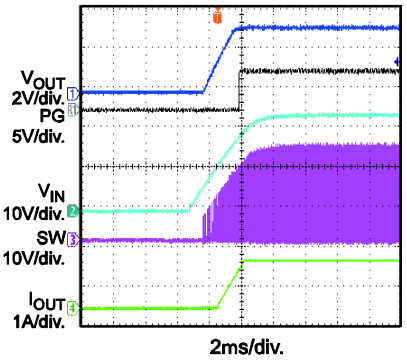
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**Typical performance characteristic waveforms are produced from the evaluation board.**
**$V_{IN}$ = 24V, $V_{OUT}$ = 3.3V, $T_A$ = 25°C, unless otherwise noted.**

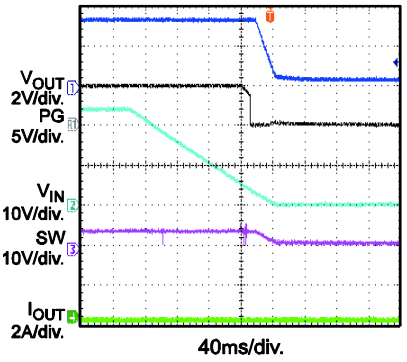
**Start-Up through Input Voltage**
$I_{OUT}$=0A



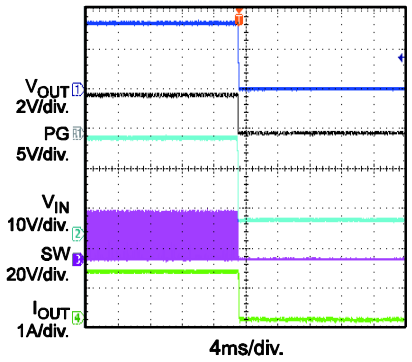

**Start-Up through Input Voltage**
$I_{OUT}$=1.2A



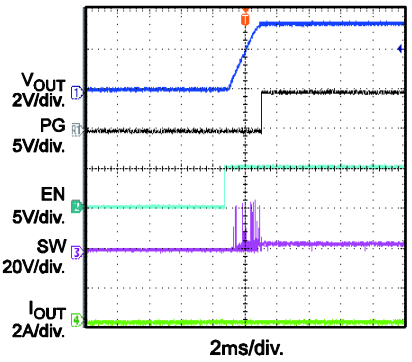

**Shutdown through Input Voltage**
$I_{OUT}$ = 0A



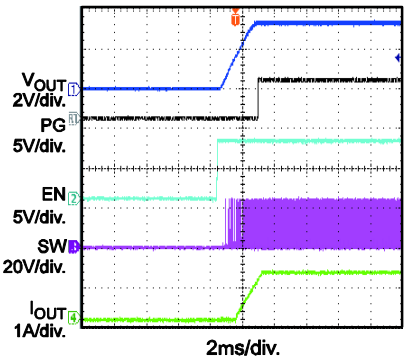

**Shutdown through Input Voltage**
$I_{OUT}$=1.2A



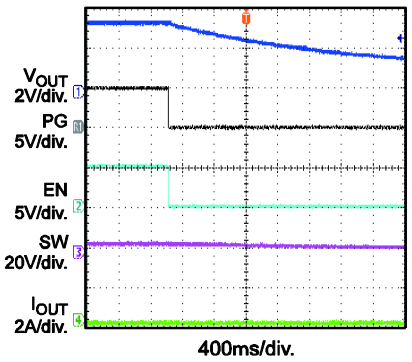

**Start-Up through Enable**
$I_{OUT}$ = 0A



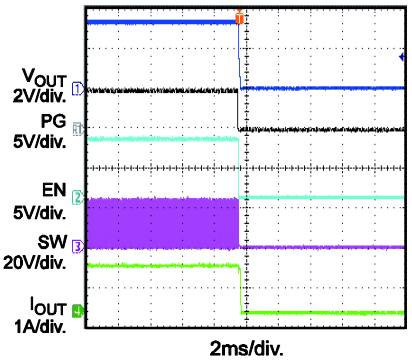

**Start-Up through Enable**
$I_{OUT}$=1.2A



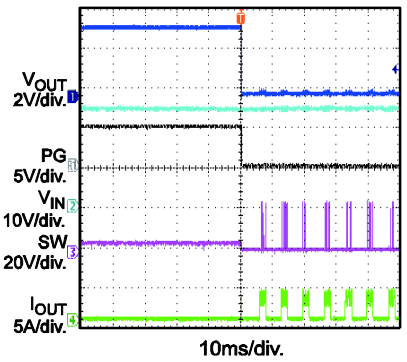

**Shutdown through Enable**
$I_{OUT}$ = 0A




**Shutdown through Enable**
$I_{OUT}$ = 1.2A




**SCP Entry**
$I_{OUT}$ = 0A





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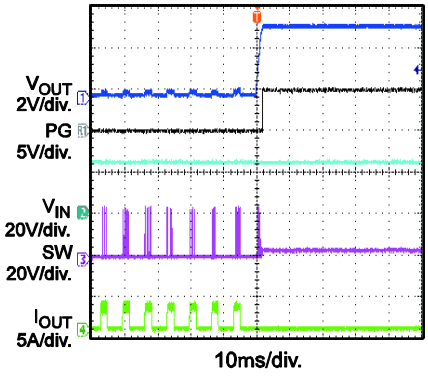
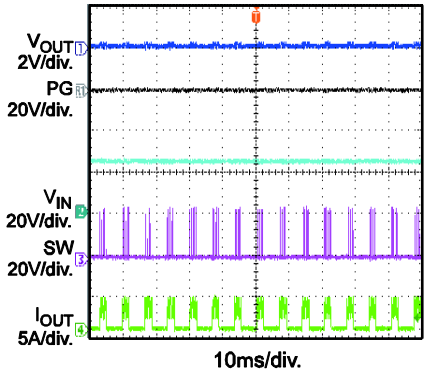
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**Typical performance characteristic waveforms are produced from the evaluation board.**
**$V_{IN}$ = 24V, $V_{OUT}$ = 3.3V, $T_A$ = 25°C, unless otherwise noted.**

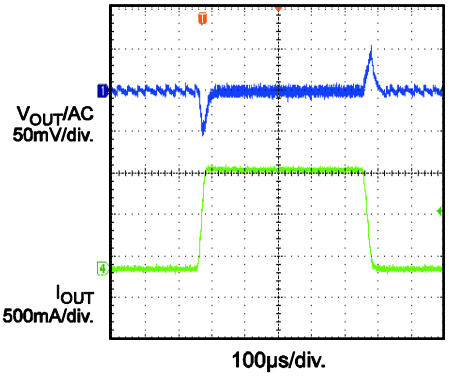
**SCP Recovery**
$I_{OUT}$ = 0A



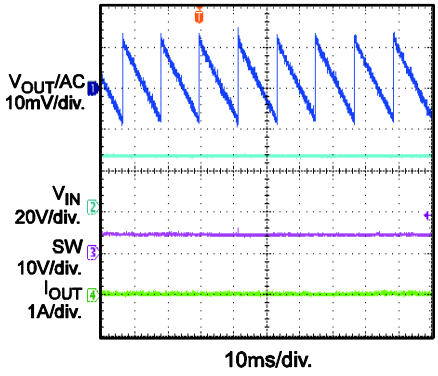

**SCP Steady State**



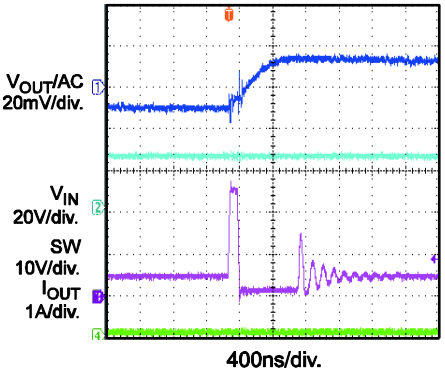

**Load Transient**
$I_{OUT}$ = 0A-1.2A



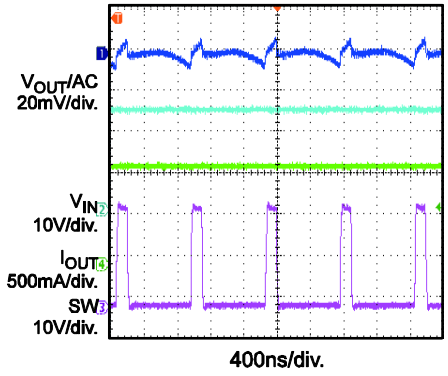

**Output Ripple**
$I_{OUT}$ = 0A




**Output Ripple**
$I_{OUT}$ = 0A




**Output Ripple**
$I_{OUT}$ = 1.2A





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## PIN FUNCTIONS

| Package Pin # | Name | Description |
|---|---|---|
| 1 | FB | **Feedback.** Connect FB to the tap of an external resistor divider from the output to AGND to set the output voltage. To prevent current-limit runaway during a short-circuit fault, the frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 400mV. Place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces. |
| 2 | VCC | **Internal 5V LDO output.** The module integrates a LDO output capacitor, so there is no need to add an external capacitor. |
| 3 | AGND | **Analog ground.** AGND is the reference ground of the logic circuit. AGND is connected internally to PGND. |
| 4, 5, 6 | SW | **Switch output.** No connection is needed for the SW pins, but a large copper plane is recommended on pins 4, 5, and 6 to improve heat sink. |
| 7, 8, 9 | OUT | **Power output.** Connect the load to OUT. An output capacitor is needed. |
| 10, 14, 18, 19, | NC | **No connection.** Do NOT connect. NC must be left floating. |
| 11 | BST | **Bootstrap.** A bootstrap capacitor is integrated internally, so external connections are not needed. |
| 12, 13 | PGND | **Power ground.** PGND is the reference ground of the power device. PCB layout requires extra care (see recommended “PCB Layout Guidelines” on page 16). For best results, connect to PGND with copper and vias. |
| 15 | IN | **Supply voltage.** IN supplies the power for the internal MOSFET and regulator. The MPM3510A operates from a +4.5V to +36V input rail. IN requires a low ESR and low inductance capacitor to decouple the input rail. Place the input capacitor very close to IN and connect it with wide PCB traces and multiple vias. |
| 16 | EN/SYNC | **Enable/synchronize.** EN=high to enable the module. Float EN or connect it to ground to disable the converter. Apply an external clock to EN to change the switching frequency. |
| 17 | PG | **Power good indicator.** PG is an open-drain structure. |


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# FUNCTIONAL BLOCK DIAGRAM

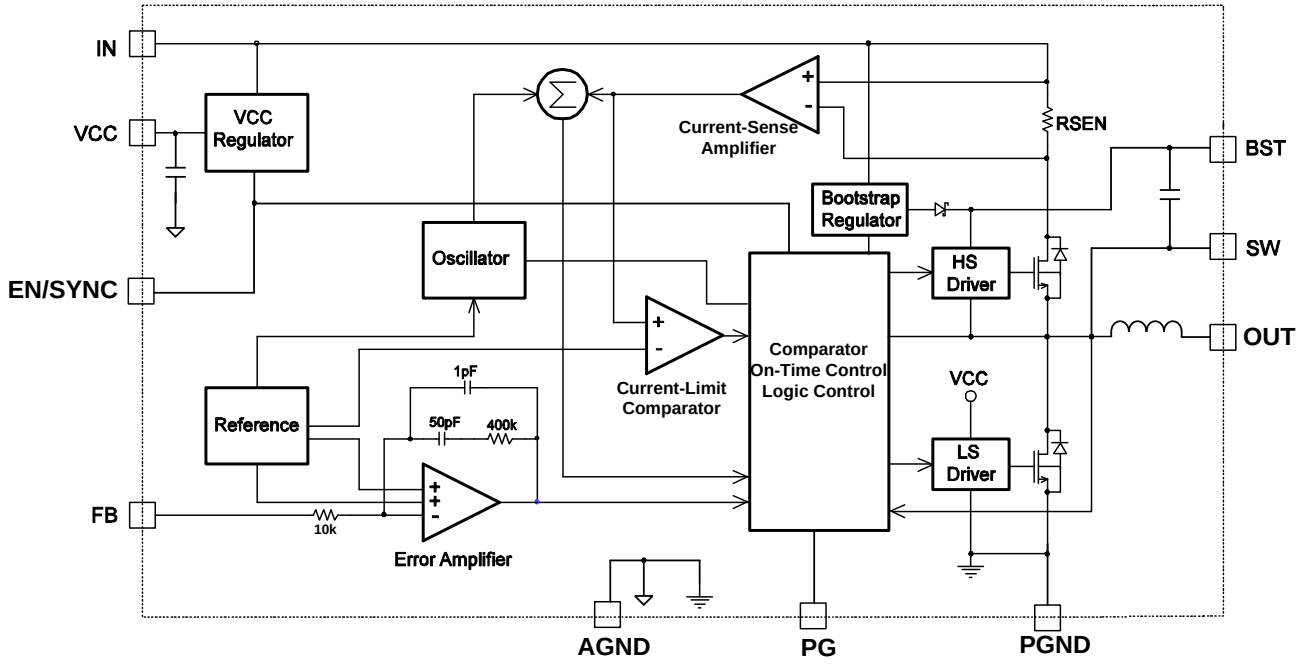


**Figure 1: Functional Block Diagram**


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## OPERATION

The MPM3510A is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs, inductor, and two capacitors. It offers a very compact solution that achieves a 1.2A continuous output current with excellent load and line regulation over a 4.5V to 36V input supply range.

The MPM3510A operates in a fixed-frequency, peak-current–control mode to regulate the output voltage. An internal clock initiates a PWM cycle. The integrated high-side power MOSFET (HS-FET) turns on and remains on until the current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle starts. If the current in the HS-FET does not reach the value set by the COMP value within 92% of one PWM period, the HS-FET is forced off.

### Internal Regulator

A 5V internal regulator powers most of the internal circuitries. This regulator takes $V_{IN}$ and operates in the full $V_{IN}$ range. When $V_{IN}$ exceeds 5V, the output of the regulator is in full regulation. When $V_{IN}$ is less than 5V, the output decreases. The part integrates an internal decoupling capacitor, so there is no need to add an external VCC output capacitor.

### AAM Operation

The MPM3510A has advanced asynchronous modulation (AAM) power-save mode for light load (see Figure 2). AAM voltage ($V_{AAM}$) is fixed internally. The internal 250mV AAM voltage sets the transition point from AAM to PWM. Under a heavy-load condition, the $V_{COMP}$ is higher than $V_{AAM}$. When the clock goes high, the HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by the COMP voltage. The internal clock re-sets every time $V_{COMP}$ is higher than $V_{AAM}$.

Under a light-load condition, the value of $V_{COMP}$ is low. When $V_{COMP}$ is less than $V_{AAM}$ and $V_{FB}$ is less than $V_{REF}$, $V_{COMP}$ ramps up until it exceeds $V_{AAM}$. During this time, the internal clock is blocked. This will make the MPM3510A skip pulses for pulse frequency modulation (PFM) mode, achieving the light-load power save.

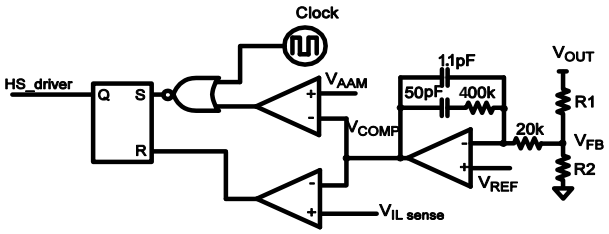


**Figure 2: Simplified AAM Control Logic**

### Error Amplifier (EA)

The error amplifier compares the FB voltage to the internal 0.81V reference ($V_{REF}$) and outputs a current proportional to the difference between the two. This output current then charges or discharges the internal compensation network to form the COMP voltage, which controls the power MOSFET current. The optimized, internal compensation network minimizes the external component count and simplifies the control loop design.

### Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MPM3510A UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 4.05V while its falling threshold is 3.65V.

### ENABLE/SYNC

EN is a control pin that turns the regulator on and off. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. An internal 1MΩ resistor from EN to GND allows EN to be floated to shut down the chip.

EN is clamped internally using a 6.5V series-Zener-diode (see Figure 3). Connecting the EN input through a pull-up resistor to the voltage on $V_{IN}$ limits the EN input current to less than 100μA.

For example, with 12V connected to $V_{in}$, $R_{PULLUP} \geq (12V - 6.5V) \div 100\mu A = 55k\Omega$.

Connecting EN directly to a voltage source without a pull-up resistor requires limiting the amplitude of the voltage source to ≤6V to prevent damage to the Zener diode.


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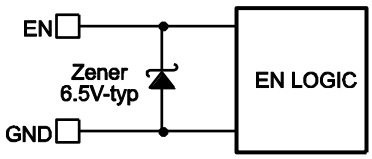


**Figure 3: 6.5V Zener Diode Connection**

Connect an external clock with a range of 800kHz to 2MHz to synchronize the internal clock rising edge to the external clock rising edge. The pulse width of the external clock signal should be less than 700ns.

### Internal Soft Start (SS)

The soft start prevents the converter output voltage from overshooting during start-up. When the chip starts, the internal circuitry generates a soft-start voltage (SS) that ramps up from 0V to 5V. When SS is lower than $V_{REF}$, the error amplifier uses SS as the reference. When SS is higher than $V_{REF}$, the error amplifier uses $V_{REF}$ as the reference. The SS time is set internally to 1.3ms.

### Over-Current Protection (OCP) and Hiccup

The MPM3510A has cycle-by-cycle peak current limit protection and valley-current detection protection. The inductor current is monitored during the HS-FET on state. If the inductor current exceeds the current-limit value set by the COMP high clamp voltage, the HS-FET turns off immediately. Then the low-side MOSFET (LS-FET) turns on to discharge the energy, and the inductor current decreases. The HS-FET remains off unless the inductor valley current is lower than a certain current threshold (the valley-current limit), even though the internal CLK pulses high. If the inductor current doesn't drop below the valley-current limit when the internal CLK pulses high, the HS-FET will miss the CLK, and the switching frequency will decrease to half the nominal value. Both the peak and valley current limits assist in keeping the inductor current from running away during an over-load or short-circuit condition.

If the output voltage drops below the under-voltage (UV) threshold (50% below the reference), the MPM3510A enters hiccup mode to re-start the part periodically (simultaneously the peak current limit is kicked) .

This protection mode is useful when the output is dead shorted to ground and greatly reduces the average short-circuit current to alleviate thermal issues and protect the regulator. The MPM3510A exits hiccup mode once the over-current condition is removed.

### Thermal Shutdown (TSD)

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the die temperatures exceed 165°C, the device stops switching. When the temperature drops below its lower threshold (145°C, typically), the power supply resumes operation.

### Floating Driver and Bootstrap Charging

An internal bootstrap capacitor powers the floating power MOSFET driver. A dedicated internal regulator (see Figure 4) charges and regulates the bootstrap capacitor voltage to ~5V. When the voltage between the BST and SW nodes drops below regulation, a PMOS pass transistor connected from $V_{IN}$ to BST turns on. The charging current path is from $V_{IN}$ to BST, and then to SW. The external circuit should provide enough voltage headroom to facilitate charging. As long as $V_{IN}$ is significantly higher than SW, the bootstrap capacitor remains charged. When the HS-FET is on ($V_{IN}$≈$V_{SW}$), the bootstrap capacitor cannot charge. When the LS-FET is on, $V_{IN}$–$V_{SW}$ reaches its maximum value for fast charging. When there is no inductor current ($V_{SW}$=$V_{OUT}$), the difference between $V_{IN}$ and $V_{OUT}$ charges the bootstrap capacitor. The floating driver has its own UVLO protection with a rising threshold of 2.2V and a hysteresis of 150mV.

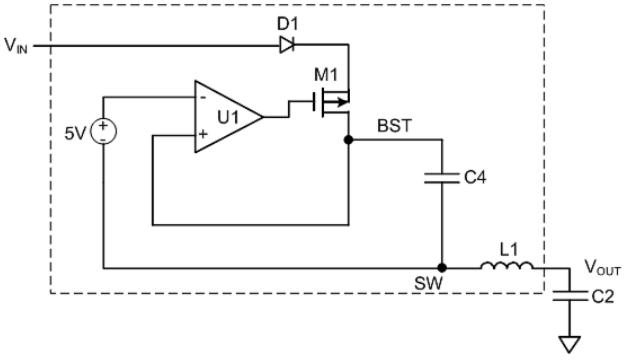


**Figure 4: Internal Bootstrap Charging Circuit**


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### Start-Up and Shutdown

If $V_{IN}$ exceeds its thresholds, the chip starts up. The reference block starts first, generating stable reference voltage and currents; then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: $V_{IN}$ low, EN low, and thermal shutdown. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.


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# APPLICATION INFORMATION

### Setting the Output Voltage

The external resistor divider sets the output voltage (see the “Typical Application” on page 1). Also, the feedback resistor (R1) sets the feedback loop bandwidth with the internal compensation capacitor (see the “Typical Application” on page 1). Choose R1 around 75kΩ when $V_{OUT} \geq 1V$. R2 is then given using Equation (1):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.81V} - 1} \quad (1)$$

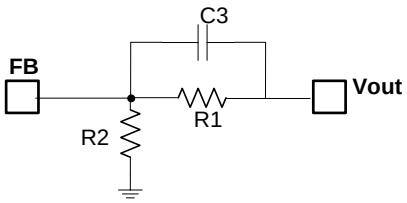


**Figure 5: Feedback Network**

See Table 1 and Figure 5 for the feedback network and a list of the recommended resistor values for common output voltages.

**Table 1: Resistor Selection for Common Output Voltages**

| $V_{OUT}$ (V) | R1 (kΩ) | R2 (kΩ) | C3(pF) |
|---|---|---|---|
| 1.0 | 75 | 300 | 33 |
| 1.2 | 75 | 150 | 33 |
| 1.5 | 75 | 91 | 22 |
| 1.8 | 75 | 62 | 22 |
| 2.5 | 75 | 36 | 22 |
| 3.3 | 75 | 24 | 22 |
| 5 | 75 | 14.3 | 22 |

### Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore, it requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Use ceramic capacitors with X5R or X7R dielectrics for best results because of their low ESR and small temperature coefficients. For most applications, use a 4.7µF capacitor.

Since C1 absorbs the input switching current, it requires an adequate ripple-current rating. The RMS current in the input capacitor can be estimated with Equation (2) and Equation (3):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (2)$$

The worse case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (3)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide sufficient charge in order to prevent excessive voltage ripple at the input. The input voltage ripple caused by capacitance can be estimated with Equation (4):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (4)$$

### Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (5):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (5)$$

Where $L_1$ is the inductor value and $R_{ESR}$ is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple. For


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simplification, the output voltage ripple can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (7)$$

The characteristics of the output capacitor affect the stability of the regulation system. The MPM3510A can be optimized for a wide range of capacitance and ESR values.

### External Bootstrap Diode

An external bootstrap diode can enhance the efficiency of the regulator given the following conditions:

- $V_{OUT}$ is 5V or 3.3V;
- the duty cycle is high: $D=\frac{V_{OUT}}{V_{IN}}$ >65%

In these cases, add an external BST diode from VCC to BST (see Figure 6).

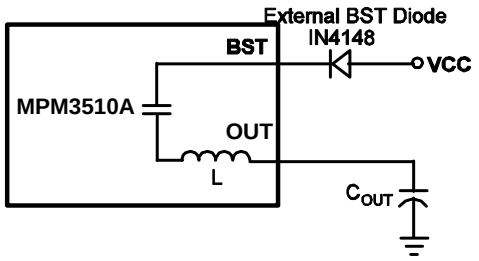



**Figure 6: Optional External Bootstrap Diode to Enhance Efficiency**

The recommended external BST diode is IN4148.

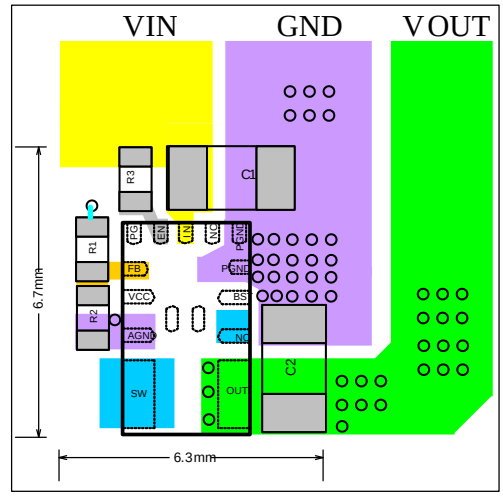
### PCB Layout Guidelines [8]

Efficient PCB layout is critical to achieve stable operation, especially for input capacitor placement. For best results, refer to Figure 7 and follow the guidelines below:

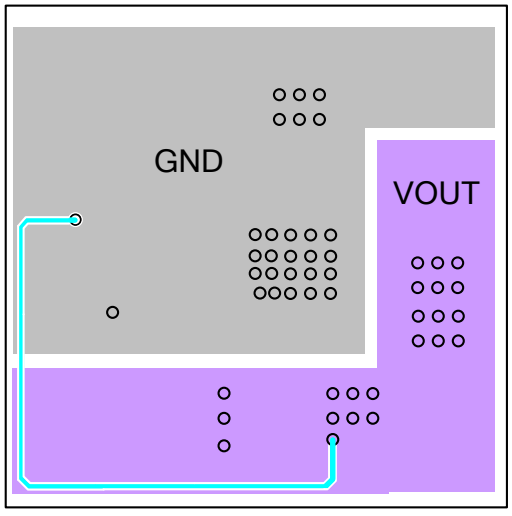
1. Use a large ground plane to connect directly to PGND. If the bottom layer is ground plane, add vias near PGND.
2. Ensure the high-current paths at GND and IN have short, direct, and wide traces.
3. Place the ceramic input capacitor close to IN and PGND. Keep the connection of the input capacitor and IN as short and wide as possible.
4. Place the external feedback resistors next to FB.
5. Keep the feedback network away from the switching node.

**NOTE:**

8) The recommended layout is based on Figure 8 and the "Typical Application Circuits" on page 18.




**Top Layer**




**Bottom Layer**

**Figure 7: Recommended PCB Layout**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## Design Example

Table 2 below is a design example following the application guidelines for the specifications below:

**Table 2: Design Example**

| | |
|---|---|
| **$V_{IN}$** | 24V |
| **$V_{OUT}$** | 3.3V |
| **Io** | 1.2A |

The detailed application schematic is shown in Figure 8. The typical performance and circuit waveforms have been shown in the “Typical Performance Characteristics” section. For additional device applications, please refer to the related evaluation board datasheets.


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## TYPICAL APPLICATION CIRCUITS

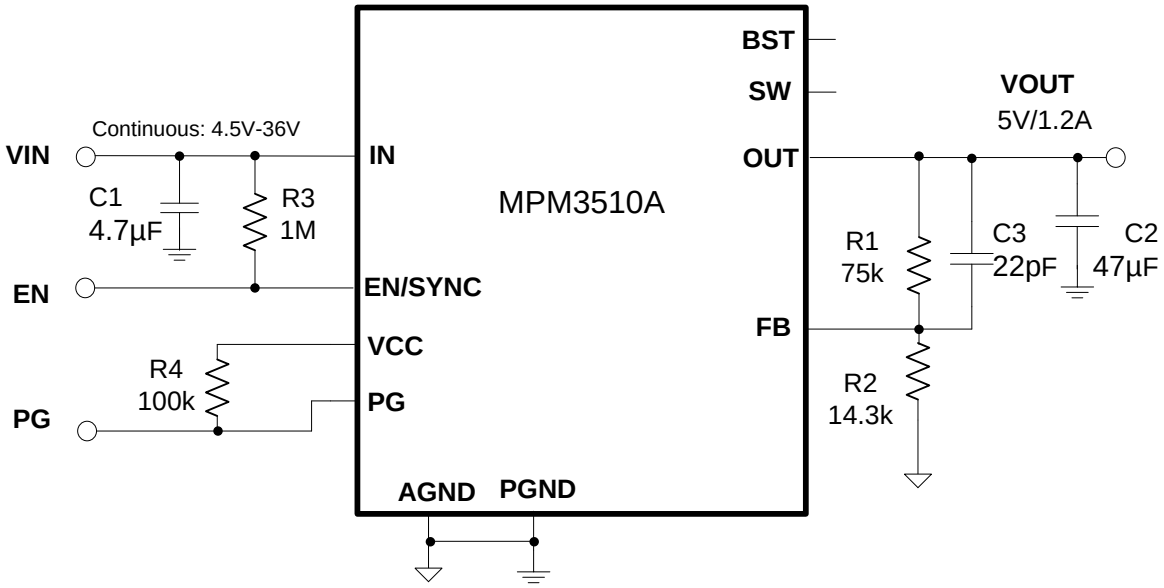


**Figure 7: $V_{OUT}$ = 5V, $I_{OUT}$ = 1.2A**

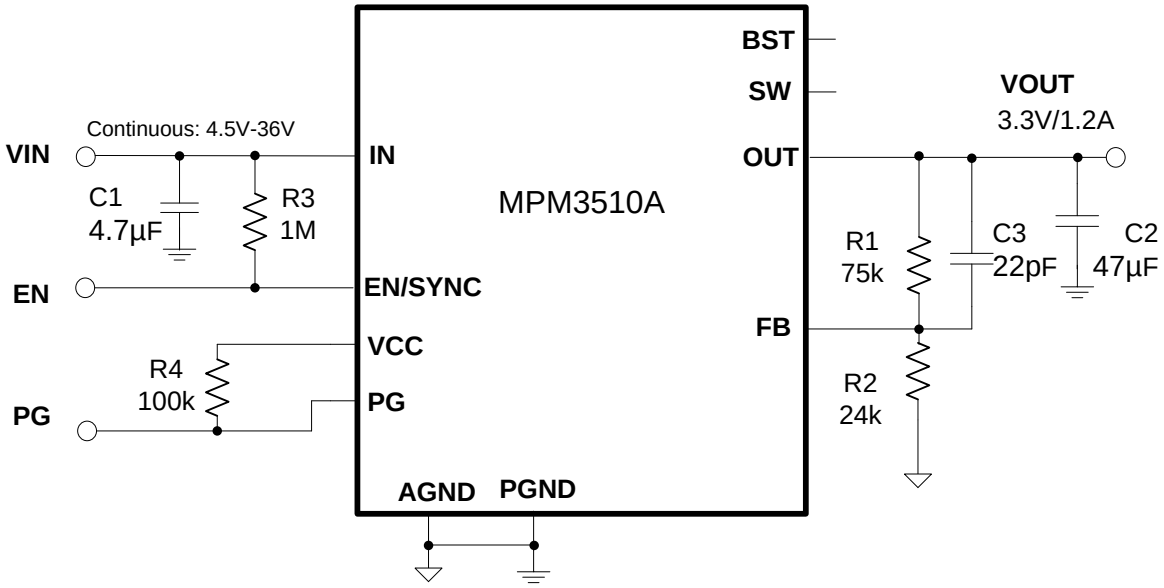


**Figure 8: $V_{OUT}$ = 3.3V, $I_{OUT}$ = 1.2A**


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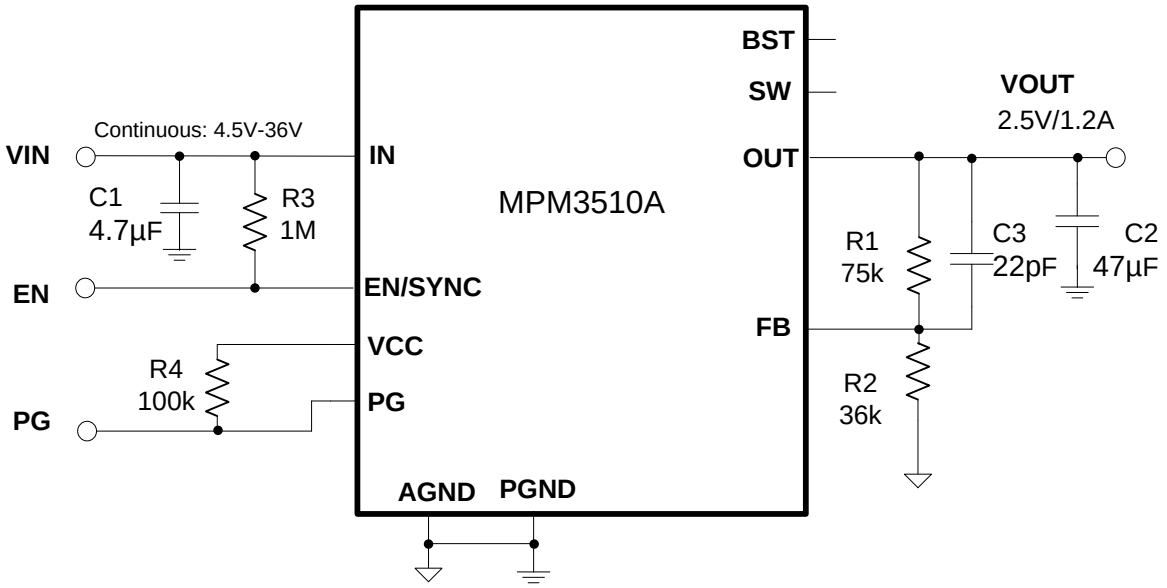


**Figure 9: $V_{OUT}$ = 2.5V, $I_{OUT}$ = 1.2A**

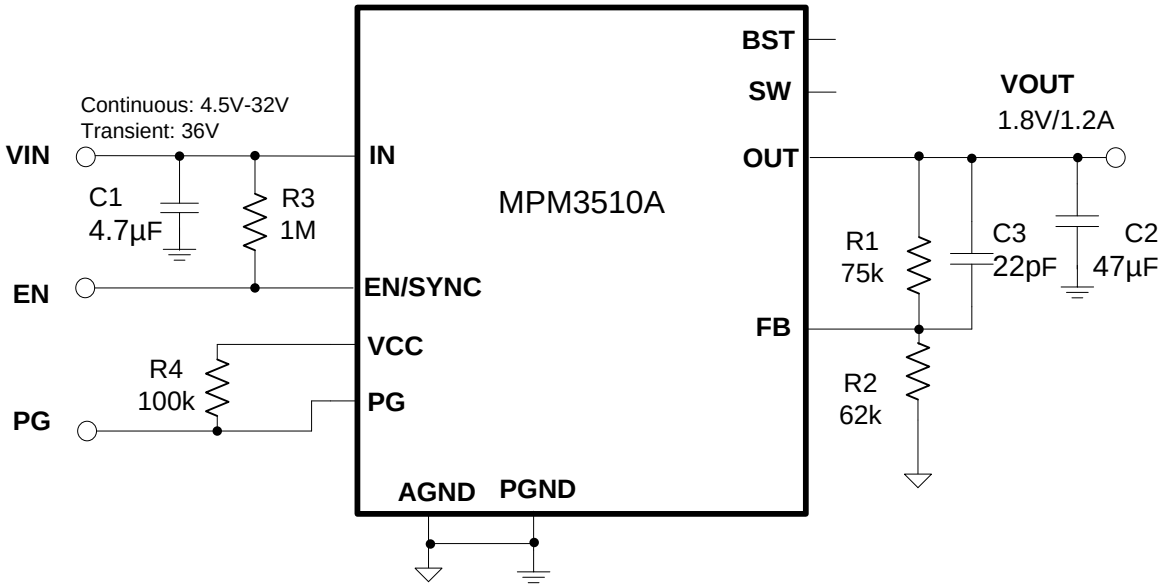


**Figure 10: $V_{OUT}$ = 1.8V, $I_{OUT}$ = 1.2A**


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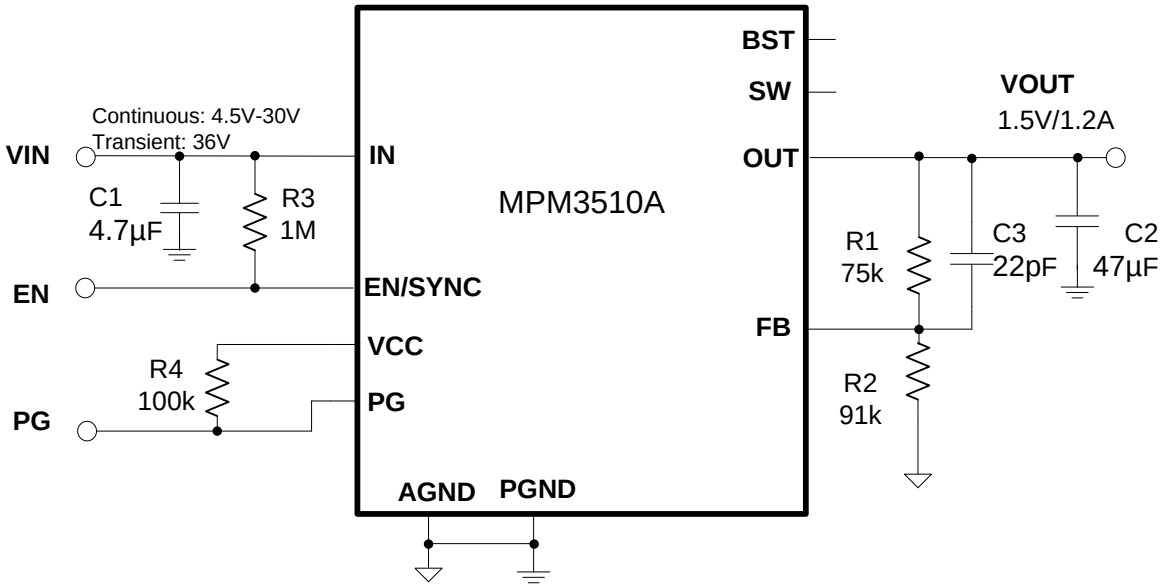


**Figure 11: $V_{OUT}$ = 1.5V, $I_{OUT}$ = 1.2A**

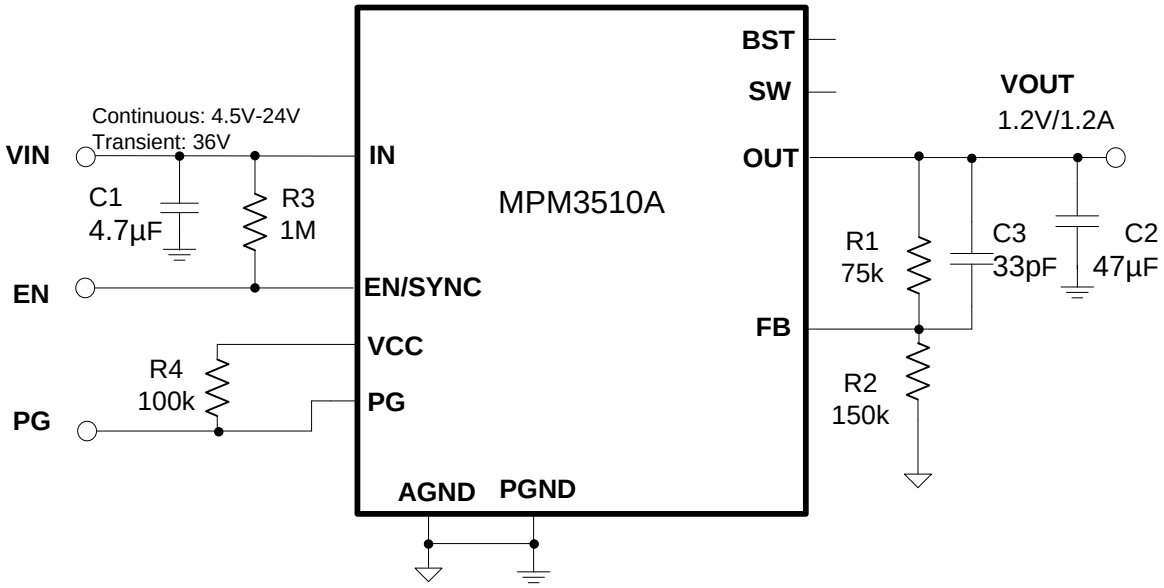


**Figure 12: $V_{OUT}$ = 1.2V, $I_{OUT}$ = 1.2A**


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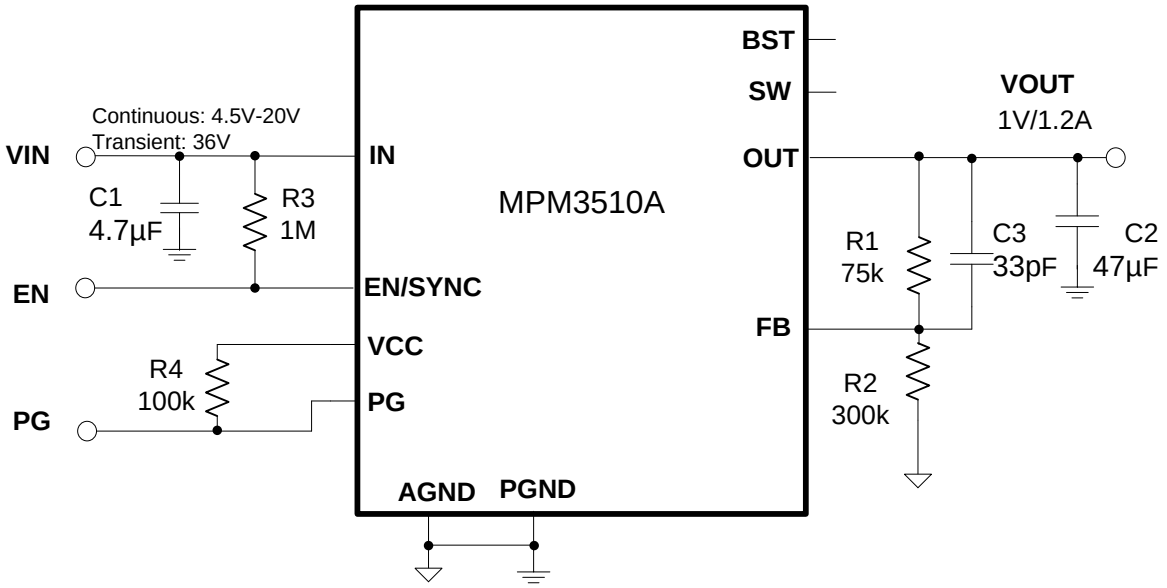


**Figure 13: $V_{OUT}$ = 1V, $I_{OUT}$ = 1.2A**


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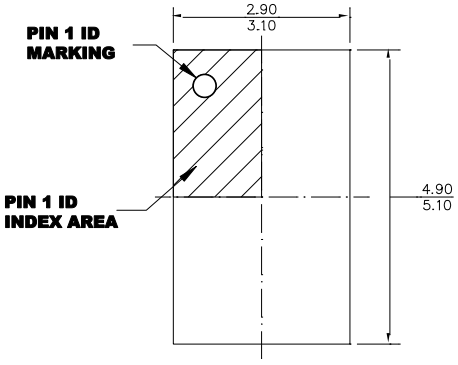
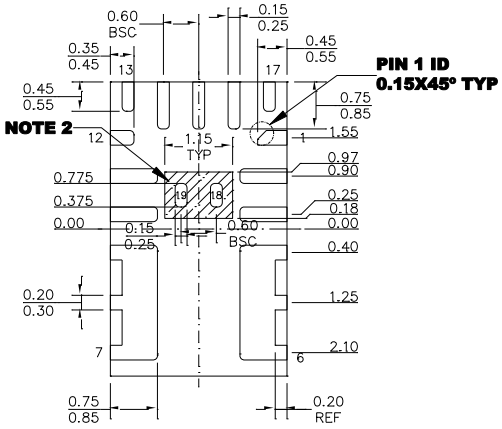
# PACKAGE INFORMATION

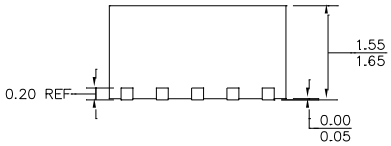
## QFN-19 (3mm x 5mm x 1.6mm)



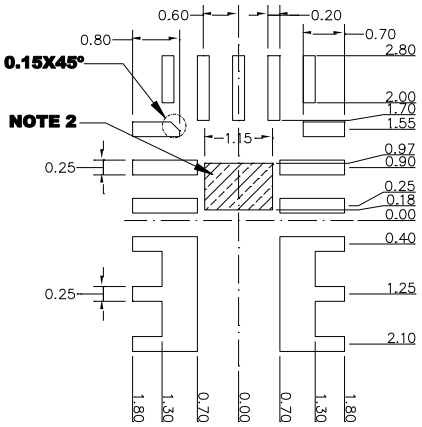

**TOP VIEW**




**BOTTOM VIEW**




**SIDE VIEW**




**RECOMMENDED LAND PATTERN**

**NOTE:**

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) SHADED AREA IS THE KEEP-OUT ZONE. ANY PCB METAL TRACE AND VIA ARE NOT ALLOWED TO CONNECT TO THIS AREA ELECTRICALLY OR MECHANICALLY.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.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## Revision History

| Revision # | Revision date | Description | Pages Updated |
|---|---|---|---|
| 1.1 | 2021/01/06 | update the OUT pin ABS<br>$V_{IN,}$….-0.3V to 40V update to $V_{IN}$ $V_{OUT}$ …. -30V to 40V | page3 |

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